ExpressLane PEX 8605-AA/AB
4-Lane, 4-Port PCI Express Gen 2 Switch
Data Book

Version 1.4

March 2014

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Revision History

Version	Date	Description of Changes
1.0	November, 2011	Production release, Silicon Revision AA.
1.1	January, 2012	Production update, Silicon Revision AA. Updated power numbers in Chapter 13, "Electrical Specifications." Updated available RDKs in Table A-1. Applied miscellaneous corrections and enhancements throughout the data book.
1.2	March, 2012	Production update, Silicon Revision AA. Corrected function of pins A26 and B19 to be VAUX_IO. Previous versions of this data book incorrectly labeled these pins as VDD_IO. **Designs that power VAUX_IO and VDD_IO supplies separately are impacted by this change. Designs that connect VAUX_IO and VDD_IO supplies together are not affected.** Applied miscellaneous corrections and enhancements throughout the data book.
1.3	November, 2012	Production release, Silicon Revision AB. Production update, Silicon Revision AA. Added support for the Exposed Pad TQFP package type (Silicon Revision AB only). Changed the Center Pad's signal name to "Ground (VSS)" Corrected pin locations in Figure 3-2. Added I^2C pin header information to Section 3.4.5. Changed "SMBus Slave Address" to "SMBus Device Address." Updated the EE_DI description. Cleaned up PM D-state references. Removed ordering information for Silicon Revision AA. Applied miscellaneous corrections and enhancements throughout the data book.
1.4	March, 2014	Production update, Silicon Revisions AA and AB. Corrected second page of Figure 14-2, dimension "e".

Copyright Information

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Preface

The information in this data book is subject to change without notice. This PLX data book to be updated periodically as new information is made available.

Audience

This data book provides functional details of PLX Technology's ExpressLane PEX 8605-AA/AB 4-Lane, 4-Port PCI Express Gen 2 Switch, for hardware designers and software/firmware engineers. The information provided pertains to both Silicon Revisions (AA and AB), unless specified otherwise.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc., www.plxtech.com

  The PLX PEX 8605 Toolbox includes this data book and other supporting documentation, *such as* errata, and design and application notes.
- The Institute of Electrical and Electronics Engineers, Inc. (IEEE), www.ieee.org
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
- Intel Corporation, www.intel.com
  - *PHY Interface for the PCI Express Architecture, Version 2.00*
- NXP Semiconductors, ics.nxp.com
  - *The I2C-Bus Specification, Version 2.1*
- PCI Special Interest Group (PCI-SIG), www.pcisig.com
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Bus Power Management Interface Specification, Revision 1.2*
  - *PCI Code and ID Assignment Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
  - *PCI Express Base Specification, Revision 1.1*
  - *PCI Express Base Specification, Revision 2.0*
  - *PCI Express Base Specification, Revision 2.0 Errata*
  - *PCI Express Base Specification, Revision 2.1*
  - *PCI Express Card Electromechanical Specification, Revision 2.0*
  - *PCI Express Mini Card Electromechanical Specification, Revision 1.1*
  - *PCI Express Architecture PCI Express Jitter and BER White Paper, Revision 1.0*
- Personal Computer Memory Card International Association (PCMCIA), www.pcmcia.org
  - *ExpressCard Standard Release 1.0*
- PXI System Alliance (PXI), www.pxisa.org
  - *PXI-5 PXI Express Hardware Specification, Revision 1.0*
- SBS Implementers Forum, smbus.org
  - *System Management Bus (SMBus) Specification, Version 2.0*

Note: *In this data book, shortened titles are associated with the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI Power Mgmt. r1.2	*PCI Bus Power Management Interface Specification, Revision 1.2*
PCI-to-PCI Bridge r1.2	*PCI to PCI Bridge Architecture Specification, Revision 1.2*
PCI Express Base r1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express Base r1.1	*PCI Express Base Specification, Revision 1.1*
PCI Express Base r2.0	*PCI Express Base Specification, Revision 2.0*
PCI Express Base r2.1	*PCI Express Base Specification, Revision 2.1*
PCI ExpressCard CEM r2.0	*PCI Express Card Electromechanical Specification, Revision 2.0*
PCI ExpressCard Mini CEM r1.1	*PCI Express Mini Card Electromechanical Specification, Revision 1.1*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*
IEEE Standard 1149.6-2003	*IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
I^2C Bus v2.1 *I2C Bus v2.1*[a]	*The I^2C-Bus Specification, Version 2.1*
SMBus v2.0	*System Management Bus (SMBus) Specification, Version 2.0*

a. Due to formatting limitations, the specification name may appear without the superscripted "2" in its title.

Terms and Abbreviations

The following tables list common terms and abbreviations used in this data book. Most terms and abbreviations defined in the *PCI Express Base r2.1* are generally not included in this table.

Terms and Abbreviations	Definitions
8b/10b	Data-encoding scheme used on data transferred across a Link that is operating at either Gen 1 or Gen 2 Link speed (2.5 or 5.0 GT/s, respectively).
ACK	Acknowledge Control Packet. A Control packet used by a destination to acknowledge Data packet receipt. A signal that acknowledges signal receipt.
ARI	Alternative Routing-ID Interpretation.
ARP	Address Resolution Protocol.
BAR	Base Address register.
BER	Bit error rate.
BIST	Built-In Self Test.
Clock cycle	One period of the PCI Express interface clock.
CRC	Cyclic Redundancy Check.
CSR	Configuration Space register.
DLL	Data Link Layer.
DMA	Direct Memory Access.
Downstream Device	Device that is connected to a downstream Port.
Downstream Port	Port that is used to communicate with a device below it in the system hierarchy. A switch can have one or more downstream Ports.
ECC	Error-Correcting Code.
EIES	Electrical Idle Exit Sequence.
EIOS	Electrical Idle Ordered-Set.
Electrical Idle	Transmitter is in a High-Impedance state (+ and - are both at common mode voltage).
EP	Endpoint.
FC	Flow Control.
Field	Multiple register bits that are combined for a single function.
FTS	Fast Training Sequence.
Gbps	Gigabits per second.
Gen 1	*PCI Express Base r1.1* and below. Link transfer rate of 2.5 GT/s.
Gen 2	*PCI Express Base r2.0* and *PCI Express Base r2.1*. Link transfer rate of 5.0 GT/s.
GPIO	General-Purpose Input/Output.
GPU	Graphics Processing Unit.
GT/s	Giga-Transfers per second.
HCSL	High-Speed Current Steering Logic.
HCSLOUT	HCSL Output clocks.
INCH	Ingress Credit Handler.
InitFC	Initialization Flow Control.

Terms and Abbreviations	Definitions
JTAG	Joint Test Action Group.
Lane	Bidirectional pair of differential PCI Express I/O signals.
LC	Inductor Capacitor.
LCRC	Link Cyclic Redundancy Check.
Link	Active connection between two Ports or devices.
Local	Reference to PCI Express attributes (*such as* credits) that belong to the PCI Express Link logic.
LTSSM	Link Training and Status State Machine.
LVDS	Low-Voltage Differential Signaling.
LVPECL	Low-Voltage Positive Emitter-Coupled Logic.
MPS	Maximum Payload Size.
NACK	Negative Acknowledge. Used in the SMBus-related content.
NAK	Negative Acknowledge.
N_FTS	Number (quantity) of Fast Training Sequences field in Training Sets.
NOP	No Operation.
OS	Ordered-Set.
P2P	Peer-to-Peer or PCI-to-PCI (as identified at point of use).
Packet	Bundle of data organized in a group for transmission. Packets typically contain control information, data, and error detection/correction bits.
PEC	Packet Error Code.
PEX	PCI Express.
PHY	Physical Layer.
PIPE	PHY Interface for PCI Express architecture.
PLL	Phase-Locked Loop.
PM	Power Management.
PME	Power Management Event.
PN	Port Number.
Port	Interface to a group of SerDes and supporting logic that is capable of creating a Link, for communication with another Port.
Port ID	Number, assigned in hardware, that associates a SerDes with a Port.
P-P	PCI-to-PCI.
PRBS	Pseudo-Random Bit Sequence.
QoS	Quality of Service.
RAS	Reliability, Availability, and Serviceability.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
Rx	Receiver.

Terms and Abbreviations	Definitions
SATA	Serial Advanced Technology Attachment. Computer bus interface used for connecting Host Bus adapters to mass storage devices, *such as* hard disk and optical drives.
SerDes	Serializer/De-Serializer. A high-speed differential-signaling parallel-to-serial and serial-to-parallel conversion logic attached to Lane pads.
SN	SerDes Number.
SPI	Serial Peripheral Interface.
SSC	Spread-Spectrum Clock.
Sticky Bits	Register bits in which the current values are unchanged by a Hot Reset, Link Down event or a Secondary Bus Reset, while the PEX 8605 is powered. Sticky bits are reset to default values by a Fundamental Reset. HwInit, ROS, RW1CS, and RWS CSR types. (Refer to Table 11-5, "Register Types, Grouped by User Accessibility," for CSR type definitions.)
Sticky State	Condition that causes a state machine to be stuck in a particular state, unable to make forward progress.
TC	Traffic Class.
TCB	Training Control Bits field in Training Sets.
TL	Transaction Layer.
TLC	Transaction Layer Control. The module performing PCI Express Transaction Layer functions.
TLP	Transaction Layer Packet. PCI Express packet formation and organization.
Transfer	One or more Bus transactions to move information between a software client and its function.
TS1	Type 1 Training Sequence Ordered-Set.
TS2	Type 2 Training Sequence Ordered-Set.
Tx	Transceiver.
UDID	Unique Device Identifier.
UI	Unit Interval – 400 ps at 2.5 GT/s, 200 ps at 5.0 GT/s.
Upstream Device	Device that is connected to Port 0.
Upstream Port	Port 0, used to communicate with a device above it in the system hierarchy. Electrically closest to the Host. Receives downstream data traffic.
UTP	User Test Pattern.
VC	Virtual Channel. The PEX 8605 supports one Virtual Channel, VC0.
Vector	Address and data.
WRR	Weighted Round-Robin scheduling.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
PEX_XXXn[*x*] PEX_XXXp[*x*]	When the signal name appears in all CAPS, with the primary Port description listed first, field [*x*] indicates the number associated with the signal pins/pads assigned to a specific SerDes module/Lane. The lowercase "n" (negative) or "p" (positive) suffix indicates the differential pair of signals, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a "#" appended to the term (*for example*, PEX_PERST#).
`Program/code samples`	`Monospace font` (*`program or code samples`*) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
Command/Status	Register names.
Parity Error Detected	Register parameter [bit or field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].
Number multipliers	k = 1,000 (10^3) is generally used with frequency response. K = 1,024 (2^{10}) is used for Memory size references. KB = 1,024 bytes. M = meg. = 1,000,000 when referring to frequency (decimal notation) = 1,048,576 when referring to Memory sizes (binary notation)
255d	d = Suffix that identifies decimal values.
1Fh	h = Suffix that identifies hex values. Each prefix term is equivalent to a 4-bit binary value (Nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 nor 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to "B" (*for example*, 4B = 4 bytes).
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord or DW	Double-Word (32 bits) is the primary register size in these devices.
QWord	Quad-Word (64 bits).
Reserved	Do not modify ***reserved*** register bits and fields. Unless specified otherwise, these bits read as 0 and must be written as 0.
word	16 bits.

Contents

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Registers

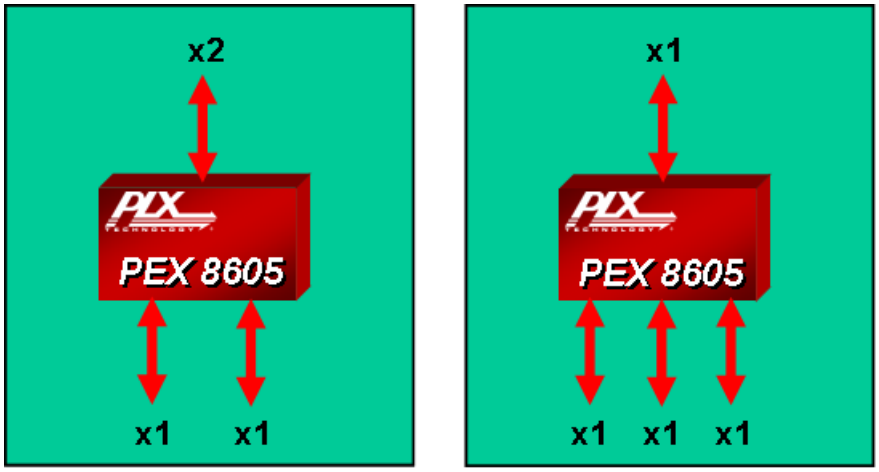
Chapter 1 Introduction

1.1 Overview

This data book describes PLX Technology's ExpressLane™ PEX 8605, a fully non-blocking, low-latency, low-cost, and low-power 4-Lane, 4-Port PCI Express Gen 2 switch. Conforming to the *PCI Express Base r2.1*, the PEX 8605 enables users to add high-bandwidth I/O to consumer products, including set-top boxes, home gateways, as well as servers, storage systems, and communications platforms. The PEX 8605's flexible hardware configuration and software programmability allows the switch to be tailored for a variety of application requirements.

.Figure 1-1 illustrates the possible PEX 8605 Port configurations, using varying Link widths.

Figure 1-1. Port Configurations



1.2 Features

The PEX 8605 supports the following features:

- 4-Port PCI Express switch
  - 4 Lanes with integrated on-chip SerDes
  - Low-power SerDes (under 90 mW per Lane)
  - Fully Non-Blocking Switch architecture
  - Port configuration
    - 4 independent Ports
    - Choice of Link width (quantity of Lanes) per unique Link/Port (x1, x2)
    - Configurable with serial EEPROM or I^2C
- Three pairs of buffered, 100-MHz HCSL output clocks, one pair for each of its downstream PCI Express Ports
- High Performance
  - Full line rate on all Ports
  - Cut-Thru packet latency of less than 250 ns between symmetric (x1 to x1)
  - Maximum Payload Size – 256 bytes
- Quality of Service (QoS) support
  - All Ports support one, full-featured Virtual Channel (VC0)
  - All Ports support eight Traffic Class (TC[7:0]) mapping, independently of the other Ports
  - Weighted Round-Robin (WRR) Port arbitration
- Reliability, Availability, Serviceability (RAS) features
  - Electromechanical Interlock supported with Power Enable output
  - Baseline and Advanced Error Reporting capability
  - JTAG AC/DC boundary scan
- INTA# (PEX_INTA#) and FATAL ERROR (FATAL_ERR#) (Conventional PCI SERR# equivalent) pin support
- 4 General-Purpose Input/Output (GPIO) pins, which can be used for Link Status LEDs, GPIOs, and/or Interrupt inputs
- Other PCI Express Capabilities
  - Transaction Layer Packet (TLP) Digest support for Poison bit
  - Lane reversal (Port 0 only, when Port 0 is configured with a x2 Link width)
  - Polarity reversal
  - Conventional PCI-compatible Link Power Management states
    - L0, L0s, L1, L2, and L2/L3 Ready
    - L3 (with Vaux supported)
  - Conventional PCI-compatible Device Power Management states
    - D0, D1, D2, and D3hot
    - D3cold (with Vaux supported)
  - Active State Power Management (ASPM)
  - Dynamic Link speed (2.5 or 5.0 GT/s) negotiation
  - Dynamic Link width negotiation

- Out-of-Band Initialization options
  - Serial EEPROM
  - I^2C and SMBus (7-bit Slave address with 100 Kbps)
- Serial EEPROM interface for initializing Configuration registers
- Testability – JTAG support
- 12-MHz oscillator with internal Phase-Locked Loop (PLL) multiplier
- 1.0V and 2.5V operating voltages
- Lead-Free and RoHS (Reduction of Hazardous Substances)-compliant
- Available in two different packages:
  - 10 x 10 mm^2, 136-pin Dual-Row Advanced Quad Flat No-lead (aQFN) package
  - 14 x 14 mm^2, 128-pin Exposed Pad Thin Quad Flat Pack (TQFP) package (Silicon Revision AB only)
- Typical power – 930 mW
- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
  - *PCI Code and ID Assignment Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2 (PCI-to-PCI Bridge r1.2)*
  - *PCI Express Base Specification, Revision 1.1 (PCI Express Base r1.1)*
  - *PCI Express Base Specification, Revision 2.0 (PCI Express Base r2.0)*
  - *PCI Express Base Specification, Revision 2.0 Errata*
  - *PCI Express Base Specification, Revision 2.1 (PCI Express Base r2.1)*
  - *PCI Express Card Electromechanical Specification, Revision 2.0 (PCI ExpressCard CEM r2.0)*
  - *PCI Express Mini Card Electromechanical Specification, Revision 1.1 (PCI ExpressCard Mini CEM r1.1)*
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Standard 1149.1-1990)*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*
  - *The I^2C-Bus Specification, Version 2.1 (I^2C Bus v2.1)*
  - *System Management Bus (SMBus) Specification, Version 2.0 (SMBus v2.0)*

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Chapter 2 Features and Applications

2.1 Flexible and Feature-Rich 4-Lane, 4-Port Switch

2.1.1 Highly Flexible Port Configurations

The PLX ExpressLane PEX 8605 PCI Express Gen 2 Switch offers a maximum of 4 Ports. Link widths can be individually configured for each Port, through auto-negotiation, hardware strapping, an optional serial EEPROM, and/or the I^2C Slave interface. Link widths can be individually configured as any power-of-two, from x1 to x2.

The PEX 8605 supports a limited, but flexible, quantity of Port configurations. *For example*, the PEX 8605 can be used in a fan-out application, with Port 0 as the upstream Port (fixed), and the remaining available Lanes divided among up to three downstream Ports.

2.1.2 Non-Blocking Crossbar Switch Architecture

The Non-Blocking Crossbar Switch architecture is an on-chip interconnect switching fabric, which is built upon the existing PLX Switch Fabric Architecture technology. In addition to addressing simultaneous multiple flows, the Crossbar Switch architecture incorporates functions required to support an efficient PCI Express switch fabric, including:

- Deadlock avoidance
- Priority preemption
- PCI Express Ordering rules
- Packet fair queuing
- Oldest first scheduling

The Crossbar Switch interconnect physical topology is that of a packet-based Crossbar Switch fabric (internal fabric). The Crossbar Switch protocol is sufficiently flexible and robust to support a variety of embedded system requirements. The Crossbar Switch architecture basic features include:

- Multiple concurrent Data transfers
- Global ordering within the PEX 8605
- Three types of transactions - Posted, Non-Posted, and Completion (P, NP, and Cpl, respectively) – meet PCI and PCI Express Ordering and Deadlock Avoidance rules
- Optional weighting of source Ports, to support Source Port arbitration

2.1.3 Low Packet Latency and High Performance

The PEX 8605 architecture supports packet **Cut-Thru with a maximum latency of 250 ns** for Link widths of x1 to x1. This, combined with large Packet memory, flexible common buffer/FC credit pool, and Non-Blocking Internal Switch architecture, provides full line rate on all Ports for performance-hungry applications, *such as* servers and switch fabrics. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the PEX 8605 supports a Packet Payload size of up to 256 bytes.

2.1.3.1 Data Payloads

The Data Payloads are variable length with a maximum of 256 bytes, as defined by the **Device Control** register *Maximum Payload Size* field (All Ports, offset 70h[7:5]; available sizes are 128 and 256 bytes). Read Requests ***do not*** include a Data Payload.

2.1.3.2 Cut-Thru Mode

Cut-Thru mode can reduce latency, especially for longer packets, because the entire packet does not need to be stored before being forwarded. Instead, after the Header is decoded, the packet can be immediately forwarded. The PEX 8605 is designed to cut through TLPs, to and from every Port. By default, all Ports are enabled for Cut-Thru. Cut-Thru mode can be disabled for all Ports, by Clearing the **Debug Control** register *Cut-Thru Enable* bit (Port 0, offset 1DCh[21]).

Notice: ***One of the drawbacks to using Cut-Thru mode is that the TLP is not known to be good until the last byte. If the TLP proves to be bad, the Cut-Thru packet must be discarded. If the TLP has already been forwarded to another device, that TLP will be framed with an EDB (End Data Bad), as opposed to the standard END.***

Note: *The **Debug Control** register Cut-Thru Enable bit affects the entire switch. If Cut-Thru is enabled, all Ports use Cut-Thru. If Cut-Thru is **not** enabled, no Ports use Cut-Thru.*

2.1.4 Virtual Channel and Traffic Classes

The PEX 8605 supports one Virtual Channel (VC0) and eight Traffic Classes (TC[7:0]). VC0 and TC0 are required by the *PCI Express Base r2.1*, and configured at device start-up.

2.1.5 Data Integrity

To enable designs that require **guaranteed error-free packets**, the PEX 8605 provides **Poison** bit support, and **Error-Correcting Code** (ECC) protection on the internal data paths and memory (RAM). ECC maintains packet integrity through the PEX 8605, by providing automatic correction of any 1-bit errors. These features are optional in the *PCI Express Base r2.1*; however, PLX provides them across its entire ExpressLane PCI Express Gen 1 and Gen 2 switch product lines.

2.1.6 Configuration Flexibility

The PEX 8605 provides several ways to configure its operations. *For example*, the PEX 8605 can be configured through Strapping pins, Host software, an optional serial EEPROM, and/or the I^2C Slave interface. Additionally, the I^2C Slave interface allows for easy debug during the Development phase, performance monitoring during the Operation phase, and driver and/or software upgrade.

2.1.7 Interoperability

The PEX 8605 is designed to be fully compliant with the *PCI Express Base r2.1*, and is backward-compatible to the *PCI Express Base r1.1* and *PCI Express Base r1.0a*. Additionally, the switch supports **auto-negotiation**, **Lane reversal** (Port 0 only, when Port 0 is configured with a x2 Link width), and **polarity reversal**, for maximum board design and board layout flexibility. Furthermore, the PEX 8605 is designed to be interoperable with many popular motherboards and server boards with PCI Express connections, and PCI Express endpoints (Ethernet, RAID Controllers), as well as PLX's family of PCI Express switches and bridges. All PLX ExpressLane devices undergo thorough interoperability testing at PLX's **Interoperability Lab** and compliance testing at the **PCI-SIG Compliance Workshop**, to ensure compatibility with PCI Express devices in the market.

2.1.8 Low Power with Granular SerDes Control

The PEX 8605 provides **low-power** capability that is fully compliant with the *PCI Express Base r2.1* and *PCI Power Mgmt. r1.2* Power Management (PM) specifications. Unused SerDes can be disabled, to further reduce power consumption.

The PEX 8605 supports **SerDes output software control**, to allow power and signal strength optimization within a system. The SerDes block also supports **Loopback modes** and **Advanced Error Reporting**, which enables efficient system debug and management.

2.1.9 Dynamic Lane Reversal

The PEX 8605 supports dynamic Lane reversal during the Link training process on Port 0 only, when Port 0 is configured with a x2 Link width.

Lane reversal capability allows flexibility in determining board routing, so that PCI Express components can be connected without having to criss-cross wires. If the wiring of Lanes to a device is reversed (on both Transmitters and Receivers), only one of the two connected devices must support Lane reversal.

Either of the outside Lanes (Transmitter and Receiver pairs) of the PEX 8605 programmed Link width must be identified as being Lane 0. During Link training, both devices on the Link negotiate the Lane numbering. During the Link Training and Status State Machine (LTSSM)'s *Configuration* state, the upstream device sends TS1 Ordered-Sets, in which each connected Lane is identified by a consecutive Lane Number, starting with Lane 0 corresponding to the physical Lane Number associated with Port 0.

Port 0 reverses its Lane Numbers and attempts to re-train when any of the following conditions occur:

- No Receiver is detected on preferred Lane 0
- No valid Training Sets are received on preferred Lane 0 during the LTSSM's *Polling* state
- TS1 with a non-zero Lane Number Port 0 is received on Lane 0

To confirm successful Lane Number negotiation, both devices exchange TS2 Ordered-Sets with identical Lane Numbers on each connected Lane.

2.1.10 Fully Compliant Power Management

The PEX 8605 supports Link (L0, L0s, L1, L2, L2/L3 Ready, and L3) and Device (D0 and D3hot) Power Management (PM) states, in compliance with the *PCI Express Base r2.1* and *PCI Power Mgmt. r1.2* PM specifications.

For further details, refer to Chapter 10, "Power Management."

2.1.11 General-Purpose Input/Output Signals

The PEX 8605 includes four General-Purpose Input/Output (GPIO) pins and associated registers, that can be programmed to function as GPIO or Link Status (Lane Good) indicators. Default functionality is LANE_GOOD[3:0]#; however, serial EEPROM, I^2C/SMBus, and/or software can program the GPIO registers to define functionality for each I/O.

For details, refer to the LANE_GOOD[3:0]# signal description in Chapter 3, "Signal Pin Descriptions," and to Section 8.5, "General-Purpose Input/Output."

2.2 Applications

The PEX 8605, with its flexible configurations, allows user-specific tuning to a variety of **Host-centric, as well as peer-to-peer, applications**.

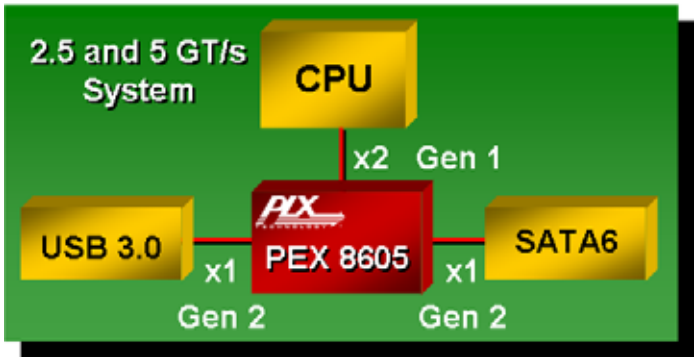
2.2.1 Host-Centric Fan-Out

The PEX 8605, with its versatile symmetric or asymmetric Lane configuration capability, allows user-specific tuning to a variety of Host-centric applications.

Figure 2-1 illustrates a typical **fan-out** design in which the processor provides a PCI Express Link that must be fanned into a larger quantity of smaller Ports for a variety of I/O functions, each with different bandwidth requirements.

In the example illustrated in Figure 2-1, the PEX 8605 has a 2-Lane Port 0, and two downstream Ports. The downstream Ports provide x1 PCI Express connectivity to the endpoints. With its maximum of four Ports, the PEX 8605 can provide fan-out connectivity to up to three PCI Express devices.

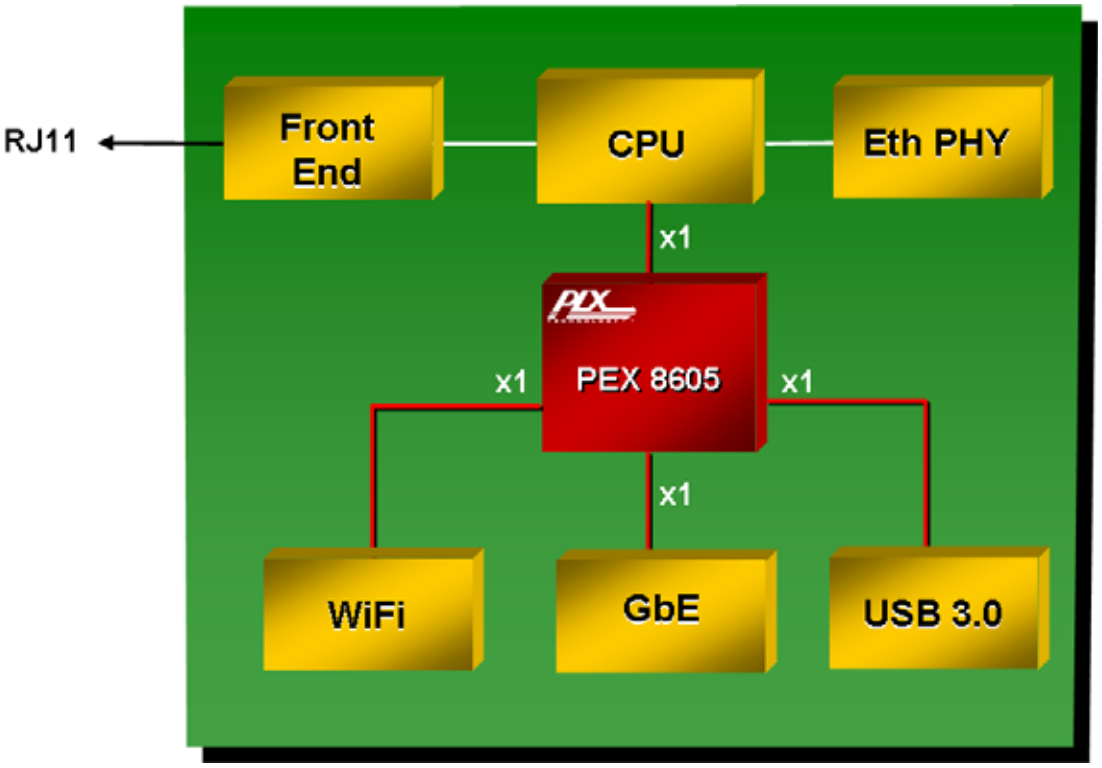
Figure 2-1. Host-Centric Fan-Out



2.2.2 Set-Top Box

With its small footprint, the PEX 8605 is ideal for consumer applications. Figure 2-2 shows an example for a set-top box. The four PEX 8605 Ports provide connectivity between the processor and up to three peripherals (each by way of a x1 connection). This usage model provides connectivity within a set-top box between the control processor and various endpoints. The PEX 8605 can also connect to legacy devices, using a PLX PCI Express-to-PCI bridge, *such as* the PEX 8112.

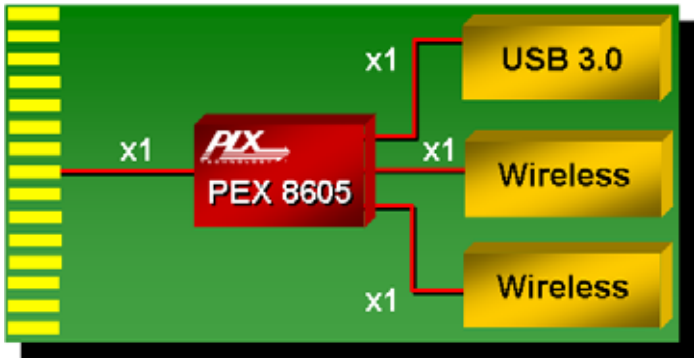
Figure 2-2. Set-Top Box



2.2.3 Mobile Wireless Adapter

The PEX 8605 can be used in applications where low power consumption is of importance, as is the case in mobile applications. An example of a wireless adapter is illustrated in Figure 2-3.

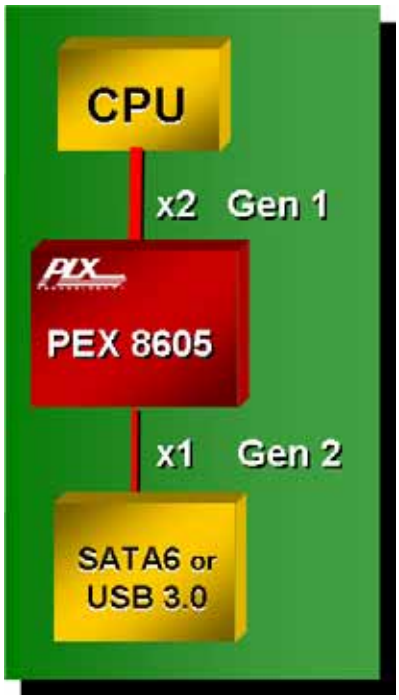
Figure 2-3. Mobile Wireless Adapter



2.2.4 Bandwidth Bridge (Bandwidth Normalization)

There are four PCI Express Lanes available in the PEX 8605. Each one can represent an individual Port, or alternatively two can be joined to form a x2 Link Port (Port 0 only). A x2 Link Port can provide double the bandwidth of a x1 Link, when all Lanes are operating at the same data rates (all at 2.5 or 5.0 GT/s). In some instances, the need to match the bandwidth between devices running at different data rates (2.5 versus 5.0 GT/s) is required to sustain the performance of the faster device. Figure 2-4 provides an example where the PEX 8605 is configured as x2x1x1. In this example, the x2 Link is running at the lower data rate (2.5 GT/s), while a single x1 Link is running at the higher data rate (5.0 GT/s). In this usage model, the PEX 8605 acts as a bridge between Gen 1 and Gen 2 devices, allowing the faster device to operate at its full-bandwidth capabilities.

Figure 2-4. Gen 1 to Gen 2 Bandwidth Bridge



2.3 Software Usage Model

From the system model viewpoint, each PCI Express Port is a virtual PCI-to-PCI bridge, with its own set of PCI Express Configuration registers. Port 0 is fixed as the upstream Port. The BIOS or Host can configure the other Ports, by way of Port 0, using Conventional PCI enumeration.

2.3.1 System Configuration

The virtual PCI-to-PCI bridges within the PEX 8605 are compliant to the PCI and PCI Express system models. The Configuration Space registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by Type 0 and Type 1 Configuration Requests, through the virtual primary bus interface (matching Bus Number, Device Number, and Function Number).

2.3.2 Interrupt Sources and Events

The PEX 8605 supports the INT*x* Interrupt Message type (compatible with *PCI r3.0* Interrupt signals) or Message Signaled Interrupts (MSI), when enabled. The PEX 8605 generates Interrupts/Messages for the following:

- Hot Plug or Power Management events
- GPIO-generated events
- Baseline and Advanced Error Reporting

Interrupts forwarded from downstream Ports and internally generated interrupts are re-mapped and collapsed at Port 0.

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Chapter 3 Signal Pin Descriptions

3.1 Introduction

This chapter provides descriptions of the 136 PEX 8605 signal pins and center Ground pad, which include the signal name, type, location, and a brief description. A map of the PEX 8605's physical pin locations is also provided.

3.2 Pin Description Abbreviations

The following abbreviations are used in the signal pin tables provided in this chapter.

Table 3-1. Pin Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
A	Analog Input signal
APWR	2.5 to 3.3V Power for SerDes Analog circuits
CMLCLKn[a]	Differential low-voltage, high-speed, CML negative Clock inputs
CMLCLKp	Differential low-voltage, high-speed, CML positive Clock inputs
CMLRn	Differential low-voltage, high-speed, CML negative Receiver inputs
CMLRp	Differential low-voltage, high-speed, CML positive Receiver inputs
CMLTn	Differential low-voltage, high-speed, CML negative Transmitter outputs
CMLTp	Differential low-voltage, high-speed, CML positive Transmitter outputs
CPWR	1.0V Power for low-voltage Core circuits
DPWR	1.0V Power for SerDes Digital circuits
GND	Common Ground for all circuits
HCSLOUT	High-Speed Current Steering Logic (HCSL) Output clocks
I	Input
I/O	Bidirectional (Input or Output)
I/OPWR	2.5 to 3.3V Power for Input and Output interfaces
N/C	No Connect, these signals must not be connected to board electrical paths
O	Output
OD	Open Drain output
PLLPWR	1.0V Power pins for Phase-Locked Loop (PLL) circuits
PD	Weak internal pull-down resistor
PU	Weak internal pull-up resistor
SerDes	Serializer/De-Serializer differential low-voltage, high-speed, I/O signal pairs (negative and positive)
STRAP	Input signals used for PEX 8605 configuration, operational mode Setting, and ***Factory Test***; these signals generally are not toggled at runtime

a. For REFCLK input, CML source is recommended; however, LVDS source is supported.

3.3 Internal Pull-Up/Pull-Down Resistors

The PEX 8605 contains I/O buffers that have weak internal pull-up or pull-down resistors, indicated in this chapter by PU or PD, respectively, in the signal pin tables (**Type** column). If a signal with this notation is used and no board trace is connected to the pin, the internal resistor is usually sufficient to keep the signal from toggling. However, if a signal with this notation is not used, but is connected to a board trace and is not used nor driven by an external source at all times, the internal resistors might not be sufficiently strong, to hold the signal in the Inactive state. In cases such as these, it is recommended that the signal be pulled or tied High to VDD_IO or Low to Ground, as appropriate, through a 3KΩ to 10KΩ resistor.

Table 3-2 lists the internal pull-up and pull-down resistor values.

Table 3-2. Internal Resistor Values

Internal Resistor	Minimum	Typical	Maximum	Units
PU	33.6K	50K	69.3K	Ω
PD	33.5K	50K	69.4K	Ω

3.4 Signal Pin Descriptions

Note: *If there is more than one pin per signal name that includes a numbered range, the locations are listed in the same sequence in which the range is listed, starting at the top row, from left to right. For example, PEX_PERn2 is located at B47, PEX_PERn1 is located at B10, and so forth.*

If there is more than one pin per signal name that does not include a numbered range (such as VDD_IO), the locations are listed in ascending alphanumeric order.

The PEX 8605 signals are divided into the following groups:

- PCI Express Signals
- Serial EEPROM Signals
- Strapping Signals
- JTAG Interface Signals
- I2C/SMBus Slave Interface Signals
- Device-Specific Signals
- No Connect Signals
- Power and Ground Signals

3.4.1 PCI Express Signals

Table 3-3 defines the PCI Express SerDes and Control signals.

Table 3-3. PCI Express Signals – 27 Pins

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
PEX_PERn[3:0]	CMLRn	A61, B47, B10, A6	121, 108, 19, 7	**Negative Half of PCI Express Receiver Differential Signal Pairs (4 Pins)**
PEX_PERp[3:0]	CMLRp	A62, A55, A11, A5	122, 109, 18, 6	**Positive Half of PCI Express Receiver Differential Signal Pairs (4 Pins)**
PEX_PERST#	I PU	B15	32	**PCI Express Reset** When asserted, causes a full-device (Fundamental) reset. Must be asserted for 100 ms after power and clocks are stable. When operating in systems that do not implement the D3cold state, PEX_PERST# should be driven together with PWRON_RST# input. (Refer to Chapter 5, "Reset and Initialization," for details.)
PEX_PETn[3:0]	CMLTn	A59, A52, A14, A8	117, 104, 23, 11	**Negative Half of PCI Express Transmitter Differential Signal Pairs (4 Pins)**
PEX_PETp[3:0]	CMLTp	A60, A53, B11, B6	118, 105, 22, 10	**Positive Half of PCI Express Transmitter Differential Signal Pairs (4 Pins)**
PEX_REFCLKn	CMLCLKn	B24	52	**Negative Half of 100-MHz PCI Express Reference Clock Input Signal Pair** PEX_REFCLKn/p do not require AC coupling capacitors, when driven from an HCSL source. Use with other Clock driver types (such as LVDS or Low-Voltage Positive Emitter-Coupled Logic (LVPECL)) has not been characterized.
PEX_REFCLKp	CMLCLKp	A27	51	**Positive Half of 100-MHz PCI Express Reference Clock Input Signal Pair** PEX_REFCLKn/p do not require AC coupling capacitors, when driven from an HCSL source. Use with other Clock driver types (such as LVDS or LVPECL) has not been characterized.
PEX_REFCLK_OUT_BIAS	A	B22	48	**Optional Bias Voltage Input** Can be left unconnected for typical applications. Suggest routing this pin to a test point.

Table 3-3. PCI Express Signals – 27 Pins *(Cont.)*

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
PEX_REFCLK_OUTn3 PEX_REFCLK_OUTn2 PEX_REFCLK_OUTn1	HCSLOUT	A21 A23 B21	39 43 46	**Negative Half of 100-MHz PCI Express Reference Clock Output for Pairs 3, 2, and 1 (3 Pins)** Reference Clock outputs are enabled, by default, and can be disabled by Clearing their **Clock Enable** register *REFCLK x Enable* bit (Port 0, offset 1D8h[10:8]). ***Note:*** *Termination resistor networks are not required for REFCLK output pairs.*
PEX_REFCLK_OUTp3 PEX_REFCLK_OUTp2 PEX_REFCLK_OUTp1	HCSLOUT	A20 A22 A24	38 41 45	**Positive Half of 100-MHz PCI Express Reference Clock Output for Pairs 3, 2, and 1 (3 Pins)** Reference Clock outputs are enabled, by default, and can be disabled by Clearing their **Clock Enable** register *REFCLK x Enable* bit (Port 0, offset 1D8h[10:8]). ***Note:*** *Termination resistor networks are not required for REFCLK output pairs.*
PEX_REFCLK_OUT_RREF	A	B23	50	**External Reference Resistor** Connect to Ground through a 2.00KΩ, 1% resistor. Place the resistor close to this pin.

3.4.2 Serial EEPROM Signals

The PEX 8605 includes four signals for interfacing to a serial EEPROM, defined in Table 3-4. For information regarding serial EEPROM use, refer to Chapter 6, "Serial EEPROM Controller."

Table 3-4. Serial EEPROM Signals – 4 Pins

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
EE_CS#	I/O as O PU	B32	73	**Active-Low Serial EEPROM Chip Select Output**
EE_DI	O	A36	71	**PEX 8605 Output to Serial EEPROM Data Input** Used for writing Serial data when programming the serial EEPROM. When an external serial EEPROM is implemented, EE_DI requires an external pull-up resistor (4.7KΩ to 10KΩ). While this I/O cell has an internal pull-up, it is not sufficiently strong to guarantee fast rise time of the signal. EE_DI can be left unconnected if a serial EEPROM is not implemented.
EE_DO	I/O as I PU	B33	75	**PEX 8605 Input from Serial EEPROM Data Output** Inputs data from the serial EEPROM during Read operations. Should be pulled High to VDD_IO.
EE_SK	I/O as O PU	A38	74	**Serial EEPROM Clock Frequency Output** Programmable, by way of the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, offset 268h[2:0]), to the following: • 1 MHz (default) • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz

3.4.3 Strapping Signals

The PEX 8605 Strapping inputs, defined in Table 3-5, Set the configuration of Link width and various setup and test modes. These inputs must be pulled or tied High to VDD_IO or Low to Ground, or left unconnected, as indicated in the table.

After a Fundamental Reset, the **Link Capability** (All Ports, offset 74h), and **Debug Control** and **Port Configuration** registers (Port 0, offsets 1DCh and 574h, respectively) capture pin status. Strapping input Configuration data can be changed, by writing new data to these registers from the serial EEPROM. I^2C/SMBus can also change Strapping input Configuration data; however, it should first Set the Port's **Port Control** register *Disable Port x* bit (Port 0, offset 234h[19:16]), to prevent linkup and Host enumeration. Then, when I^2C programming is complete, I^2C/SMBus should lastly Clear Port 0's *Disable Port x* bit, to enable linkup and allow subsequent Host enumeration.

Table 3-5. Strapping Signals – 15 Pins

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
STRAP_DEBUG_SEL#	I PU	C4	30	***Factory Test Only*** STRAP_DEBUG_SEL# can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied High to VDD_IO.
STRAP_FAST_ BRINGUP#	I PU	A40	78	***Factory Test Only*** STRAP_FAST_BRINGUP# can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied High to VDD_IO.
STRAP_LEGACY	I PU	C13	97	***Factory Test Only*** STRAP_LEGACY can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied High to VDD_IO.
STRAP_PLL_ BYPASS#	I PU	C12	96	***Factory Test Only*** STRAP_PLL_BYPASS# can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied High to VDD_IO.
STRAP_PORTCFG	I PD	B37	83	**Port Configuration Select** Defines the PEX 8605 Port configuration. The STRAP_PORTCFG value is reflected in the initial **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0]) value. This configuration Setting can subsequently be overwritten by serial EEPROM load. (Refer to Chapter 6, "Serial EEPROM Controller," for details.) L = x1x1x1x1 (Lane 0 is Port 0, upstream) H = x2x1x1 (Lanes [1-0] combine to form Port 0, upstream)
STRAP_PROBE_ MODE#	I PU	C3	27	***Factory Test Only*** STRAP_PROBE_MODE# can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied High to VDD_IO.

Table 3-5. Strapping Signals – 15 Pins *(Cont.)*

<table>
<tr><th>Signal Name</th><th>Type</th><th>Dual-Row aQFN Location</th><th>Exposed Pad TQFP Location</th><th>Description</th></tr>
<tr><td>STRAP_RC_MODE</td><td>I
PD</td><td>B35</td><td>79</td><td>Factory Test Only
STRAP_RC_MODE can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied Low to Ground.</td></tr>
<tr><td>STRAP_SERDES_ MODE_EN#</td><td>I
PU</td><td>A39</td><td>76</td><td>Factory Test Only
STRAP_SERDES_MODE_EN# can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied High to VDD_IO.</td></tr>
<tr><td>STRAP_SMBUS_EN#</td><td>I
PU</td><td>B28</td><td>62</td><td>System Management Bus Enable
Selects the I²C or SMBus protocol, and defines the default SMBus Configuration register SMBus Enable bit (Port 0, offset 2ACh[0]) value, as listed below.
<table><tr><th>STRAP_SMBUS_EN# Input State</th><th>Offset 2ACh[0] Value</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>When pulled or tied Low to Ground, enables SMBus Slave protocol on the I2C_SCL and I2C_SDA 2-wire bus. ARP is enabled if I2C_ADDR2 is Low when sampled at the time PEX_PERST# input de-asserts.
When pulled or tied High to VDD_IO, enables I²C Slave protocol on the I2C_SCL and I2C_SDA 2-wire bus.</td></tr>
<tr><td>STRAP_SSC_ CENTER#</td><td>I
PU</td><td>C11</td><td>93</td><td>Factory Test Only
STRAP_SSC_CENTER# can be left unconnected in standard applications. If this input is connected to a board circuit trace, it must be externally pulled or tied High to VDD_IO.</td></tr>
</table>

Table 3-5. Strapping Signals – 15 Pins *(Cont.)*

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
STRAP_TEST MODE[3:0]	[3, 1]: I PU [2, 0]: I PD	C10, C9, C8, C7	67, 64, 63, 60	***Factory Test Only* (4 Pins)** STRAP_TESTMODE[3:0] can be left unconnected in standard applications. If these pins are connected to external board traces, they must be strapped as HLHL, as follows: • STRAP_TESTMODE[3, 1] must be pulled or tied High to VDD_IO • STRAP_TESTMODE[2, 0] must be pulled or tied Low to Ground
STRAP_UPCFG_ TIMER_EN#	I PU	A28	53	**Link Upconfigure Timer Enable** STRAP_UPCFG_TIMER_EN# maps to the **Debug Control** register *STRAP_UPCFG_TIMER_EN# Pin State* bit (Port 0, offset 1DCh[4]). This input and its corresponding register bit must ***not*** be toggled at runtime. When STRAP_UPCFG_TIMER_EN# is pulled or tied High, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the 5.0 GT/s (Gen 2) data rate and Autonomous Change. When STRAP_UPCFG_TIMER_EN# is pulled or tied Low, if this Link training sequence fails during the *Configuration* state, the next time the LTSSM exits the *Detect* state, TS Ordered-Sets advertise only the 2.5 GT/s (Gen 1) data rate and no Autonomous Change support. If Link training continues to fail when the LTSSM is in the *Configuration* state, the LTSSM continues to alternate between Gen 1 and Gen 2 advertisement every time it exits the *Detect* state. ***Note:*** *This feature should only be enabled if a non-compliant device will not linkup when these Data Rate Identifier bits are Set.*

3.4.4 JTAG Interface Signals

The PEX 8605 includes five signals for performing Joint Test Action Group (JTAG) boundary scan, defined in Table 3-6. The JTAG interface is described in Section 12.7, "JTAG Interface."

Table 3-6. JTAG Interface Signals – 5 Pins

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
JTAG_TCK	I PU	A48	94	**JTAG Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 20 MHz.
JTAG_TDI	I PU	A47	91	**JTAG Test Data Input** Serial input to the JTAG TAP Controller, for test instructions and data.
JTAG_TDO	O	B29	65	**JTAG Test Data Output** Serial output from the JTAG TAP Controller test instructions and data.
JTAG_TMS	I PU	B42	95	**JTAG Test Mode Select** Input decoded by the JTAG TAP Controller, to control test operations.
JTAG_TRST#	I PU	A34	66	**JTAG Test Reset** Active-Low input used to reset the Test Access Port. When JTAG functionality is not used, the JTAG_TRST# input should be driven Low, or pulled Low to VSS (Ground) through a 1.5KΩ resistor, to place the JTAG TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's **Instruction** register to contain the *IDCODE* instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.

3.4.5 I²C/SMBus Slave Interface Signals

Table 3-7 defines the five I²C/SMBus Slave interface signals. The I²C/SMBus Slave interface provides access to the PEX 8605 registers. Most registers that can be programmed by serial EEPROM (including registers that are Read Only to PCI Express), can be also programmed by I²C/SMBus. However, I²C/SMBus cannot replace the serial EEPROM programming of some registers, *such as* SerDes- and Hot Plug-related registers that (generally) must be configured prior to automatic link training, immediately following Reset. I²C/SMBus can also be used to program the serial EEPROM.

The I²C/SMBus Slave interface used with PLX software is a powerful debugging tool that enables register access, regardless of whether the PCI Express Link is Up. Figure 3-1 illustrates the suggested Header pin layout on 0.1-inch centers, for direct connection to the Total Phase Aardvark I²C-USB converter (as used with PLX Rapid Development Kits (RDKs)).

For further details, refer to Chapter 7, "I2C/SMBus Slave Interface Operation."

Figure 3-1. Suggested I²C Header Pin Layout on 0.1-Inch Centers

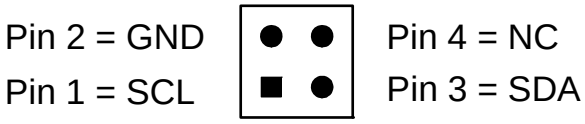


Table 3-7. I2C/SMBus Slave Interface Signals – 5 Pins

<table>
<tr><th>Signal Name</th><th>Type</th><th>Dual-Row aQFN Location</th><th>Exposed Pad TQFP Location</th><th>Description</th></tr>
<tr><td>I2C_ADDR [2:0]</td><td>I
PU</td><td>A41, B36, A42</td><td>80, 81, 82</td><td>
I2C Slave/SMBus Device Address Bits 2 through 0 Inputs (3 Pins)

Used to define the three least significant bits of the PEX 8605 7-bit I2C Slave/SMBus Device Address, which is reflected in both the I2C Configuration register Slave Address and SMBus Configuration register SMBus Device Address fields (Port 0, offsets 294h[2:0] and 2ACh[7:1], respectively). If I2C or SMBus configuration is used, the I2C_ADDR[2:0] inputs should be strapped to a unique address, to avoid an address conflict with any other I2C/SMBus devices (on the same I2C Bus/SMBus segment).

The following table lists the pin and register bit values associated with the I2C Slave and SMBus Device addresses.
<table>
<tr><th>I2C_ADDR [2:0] Values</th><th>Offset 294h[2:0] Value</th><th>Offset 294h[6:3] Value</th><th>I2C Slave Address</th><th>SMBus Device Address</th></tr>
<tr><td>000</td><td>000b</td><td rowspan="8">1011b</td><td>1011_000b</td><td>ARP</td></tr>
<tr><td>001</td><td>001b</td><td>1011_001b</td><td>ARP</td></tr>
<tr><td>010</td><td>010b</td><td>1011_010b</td><td>ARP</td></tr>
<tr><td>011</td><td>011b</td><td>1011_011b</td><td>ARP</td></tr>
<tr><td>100</td><td>100b</td><td>1011_100b</td><td>1011_100b</td></tr>
<tr><td>101</td><td>101b</td><td>1011_101b</td><td>1011_101b</td></tr>
<tr><td>110</td><td>110b</td><td>1011_110b</td><td>1011_110b</td></tr>
<tr><td>111</td><td>111b</td><td>1011_111b</td><td>1011_111b</td></tr>
</table>
Continued…
</td></tr>
</table>

Table 3-7. I²C/SMBus Slave Interface Signals – 5 Pins *(Cont.)*

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
I2C_ADDR [2:0]	I PU	A41, B36, A42	80, 81, 82	**I2C Slave/SMBus Device Address Bits 2 through 0 Inputs (3 Pins) *(Cont.)*** If the STRAP_SMBUS_EN# input (of which its inverse value defines the default value of the **SMBus Configuration** register *SMBus Enable* bit (Port 0, offset 2ACh[0])) is Low, to enable SMBus protocol as default, the I2C_ADDR2 input defines the same default value for two register bits – bit 2 of the Slave address (Port 0, offset 294h[2]), and the **SMBus Configuration** register *ARP Disable* bit (Port 0, offset 2ACh[8]). Specifically, if the STRAP_SMBUS_EN# input is Low (to enable SMBus protocol as default): • If the I2C_ADDR2 input is Low, to enable Address Resolution Protocol (ARP) as default, the *ARP Disable* bit default value is 0, and bit 2 of the **I2C Configuration** register *Slave Address* field defaults to a value of 0. In this configuration, the upper five bits of the 7-bit Slave address default to value 10110b. • If the I2C_ADDR2 input is High, to disable ARP as default, the *ARP Disable* bit default value is 1, and bit 2 of the **I2C Configuration** register *Slave Address* field defaults to a value of 1. In this configuration, the upper five bits of the 7-bit Slave address default to value 10111b. The internal pull-up resistors cause the I2C_ADDR[2:0] inputs to default to HHH (111b). If the I²C/SMBus Slave address must be changed to a different value, add pull-down resistors, to force the appropriate I2C_ADDR[2:0] inputs to a logic Low state, and the Address bits that are to be logic High can be pulled High, or optionally, can remain unconnected. However, if the I2C_ADDR[2:0] inputs that are logic High are connected to circuit traces, external pull-up resistors are recommended, because the internal pull-up resistors might not be sufficiently strong, to hold the input(s) High.
I2C_SCL	OD	A45	87	**I²C/SMBus Serial Clock Line** I²C/SMBus Clock line. Data on the I²C Bus can be transferred at rates of up to 100 kbit/s (Standard mode). **I2C_SCL requires an external pull-up resistor.** ***Note:*** *The PEX 8605 I²C/SMBus Slave Interface can stretch the Low period of the I²C/SMBus clock while a simultaneous in-band Request that also targets PEX 8605 registers is being processed.*
I2C_SDA	OD	B39	88	**I²C/SMBus Serial Data I/O** Transmits and receives I²C/SMBus data during I²C/SMBus accesses to PEX 8605 registers. **I2C_SDA requires an external pull-up resistor.**

3.4.6 Device-Specific Signals

Table 3-8 defines the Device-Specific signals – signals that are unique to the PEX 8605.

Table 3-8. Device-Specific Signals – 15 Pins

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
FATAL_ERR#	O	B40	90	**Fatal Error Output** Asserted Low when a Fatal error is detected in the PEX 8605 and the following conditions exist (all the same conditions that are required to send a Fatal Error Message to the Host). For *PCI Express Base r2.1* errors: • Specific error is defined as *Fatal* in the **Uncorrectable Error Severity** register (All Ports, offset FC0h), and • Reporting of the specific error condition is enabled (not masked) by the **Uncorrectable Error Mask** register's (All Ports, offset FBCh) corresponding *Interrupt Mask* bit, and • **Device Control** register *Fatal Error Reporting Enable* bit (All Ports, offset 70h[2]) –or– **PCI Command** register *SERR# Enable* bit (All Ports, offset 04h[8]) is Set Device-Specific (RAM ECC) errors can be reported as a PCI Express Uncorrectable Error, and/or by interrupt (INT*x*, MSI, or PEX_INTA#) signaling by the FATAL_ERR# output: • Uncorrectable Internal error in the **Uncorrectable Error Status** register *Uncorrectable Internal Error Status* bit (Port 0, offset FB8h[22]) is defined as *Fatal* in the **Uncorrectable Error Severity** register *Uncorrectable Internal Error Severity* bit (Port 0, offset FC0h[22]), and • Reporting of Uncorrectable Internal errors is enabled (not masked) by the **Uncorrectable Error Mask** register *Uncorrectable Internal Error Mask* bit (Port 0, offset FBCh[22]), and • **Device Control** register *Fatal Error Reporting Enable* bit (All Ports, offset 70h[2]) –or– **PCI Command** register *SERR# Enable* bit (All Ports, offset 04h[8]) is Set The **Device Status** register *Fatal Error Detected* bit (All Ports, offset 70h[18]) is Set, and the specific error is flagged in the **Uncorrectable Error Status** register (All Ports, offset FB8h). **If FATAL_ERR# output is not used, this signal can remain unconnected.**

Table 3-8. Device-Specific Signals – 15 Pins *(Cont.)*

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
HP_PRSNT#	I/O as I PU	B25	55	**Hot Plug PRSNT# Input** Active-Low slot control logic input that connects to the PCI Express slot's PRSNT# signal, which is typically grounded. A change in the HP_PRSNT# input state is latched in the **Slot Status** register *Presence Detect Changed* bit (Downstream Ports, offset 80h[19]), and the state change can assert an interrupt to notify the Host of a board's presence in the slot. When the following conditions exist: • HP_PRSNT# is not masked (**Slot Control** register *Presence Detect Changed Enable* bit (Downstream Ports, offset 80h[3], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set an interrupt (MSI, INT*x* Message, and/or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated. ***Note:*** *HP_PRSNT# is internally de-bounced, but must remain stable for at least 10 ms.*
LANE_GOOD[3:0]#	I/O PU	B16, B55, A16, A19	35, 125, 28, 36	**Active-Low PCI Express Lane Status Indicator Outputs for Lanes [3-0] (Default) or General-Purpose I/O (4 Pins)** Default function for these pins is LANE_GOOD[3:0]#, as determined by the **Debug Control** register *LANE_GOODx#/GPIOx Pin Function Select* bit (Port 0, offset 1DCh[22] is Set). The LANE_GOOD[3:0]# signals reflect Link status for each PCI Express Lane, and can directly drive the common-anode LED module. LANE_GOOD[3:0]# LED behavior is as follows: • **Solid Off** – Lane is disabled • **Solid On** – Lane is enabled, 5.0 GT/s • **0.5 seconds On, 0.5 seconds Off** – Lane is enabled, 2.5 GT/s, reduced Lanes are up (latter applies only to Port 0, when its Link width is x2) Alternately, the LANE_GOOD[3:0]# pins can be programmed as General-Purpose I/O (GPIO) signals that provide input, output, and/or pulse-width-modulated (PWM) output functions for specific applications. (Refer to Section 8.5, "General-Purpose Input/ Output," and Section 12.8, "Lane Good Status LEDs," for further details.)

Table 3-8. Device-Specific Signals – 15 Pins *(Cont.)*

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
MFG_AMC	I PD	C5	31	***Factory Test Only*** Do not connect this pin to board electrical paths.
MFG_TAPEN	I PD	C6	34	***Factory Test Only*** Do not connect this pin to board electrical paths.
MFG_TMC1	I PD	C15	126	***Factory Test Only*** Do not connect this pin to board electrical paths.
MFG_TMC2	I PD	C16	1	***Factory Test Only*** Do not connect this pin to board electrical paths.
PEX_INTA#	OD	B34	77	**Interrupt Output** PEX_INTA# Interrupt output is enabled if: • INT*x* Messages are enabled (**PCI Command** register *Interrupt Disable* bit (All Ports, offset 04h[10]) is Cleared), and MSIs are disabled (**MSI Control** register *MSI Enable* bit (All Ports, offset 48h[16]) is Cleared) • PEX_INTA# output is enabled (**ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for x Interrupt* bit(s) (All Ports, offset 1C8h[6 and/or 4]) are Set) The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources: • Conventional PCI INT*x* Message generation • Native MSI transaction generation • Device-Specific PEX_INTA# assertion PEX_INTA# assertion (Low) indicates that one or more of the following events and/or errors (if not masked) were detected: • Power Management events • Hot Plug events • General-Purpose Input Interrupt events (Refer to Section 8.4, "PEX_INTA# Interrupts," for details.) **If used, PEX_INTA# requires an external pull-up to VDD_IO.**
PROCMON	O	C14	100	***Factory Test Only*** Do not connect this pin to board electrical paths.

Table 3-8. Device-Specific Signals – 15 Pins *(Cont.)*

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
PWRON_RST#	I PU	B14	29	**Power-On Reset** When asserted Low, causes a reset of the Wake/Beacon Detect circuitry in a sleeping system (D3hot). When operating in systems in which remote Wakeup, using WAKE# or beacon signaling from the D3cold state, must be forwarded, PWRON_RST# must be held High when the PEX 8605 is in the D3cold state. (Refer to Section 10.3.1.4, "D3cold Device Power Management State," for details.) When operating in systems that do not implement the D3cold state, PWRON_RST# should be driven together with PEX_PERST#. (Refer to Chapter 5, "Reset and Initialization," for details.)
WAKE#	OD	B56	128	**PCI Express WAKE#** Bidirectional signal used in systems that implement the remote Wakeup function. When the PEX 8605 is in the D3cold state: • PEX 8605 asserts WAKE# Low, if a PCI Express beacon is received by a downstream Port • If another device asserts WAKE# Low, the PEX 8605 drives PCI Express beacon signaling toward the Root Complex (Refer to Section 10.3.1.4, "D3cold Device Power Management State," for further details.) When operating in systems that do not implement the D3cold state, PWRON_RST# should be driven together with PEX_PERST#. WAKE# should be externally pulled High to VAUX_IO.
XTAL_IN	I PU	B30	68	***Factory Test Only/Not Used*** Pull or tie this pin Low to VSS (Ground).

3.4.7 No Connect Signals

Notice: ***Do not connect these pins to board electrical paths. These pins are internally connected to the device.***

Table 3-9. No Connect Signals – 14 Pins

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
N/C	***Reserved***	A1, A2, A3, A4, A17, A33, A35, A44, A49, B1, B2, B38, C1, C2	2, 69, 85, 86	**No Connect (14 Pins (Dual-Row aQFN) or 4 Pins (Exposed Pad TQFP))** Do not connect these pins to board electrical paths.

3.4.8 Power and Ground Signals

Table 3-10. Power and Ground Signals – 51 Pins and Center Pad

Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
GROUND (VSS)	GND	CENTER PAD	CENTER PAD	**Ground**
PEX_VDDA_P3 PEX_VDDA_P2 PEX_VDDA_P1 PEX_VDDA_P0	APWR	B50 B44 B13 B8	114 101 26 14	**2.5 or 3.3V SerDes Analog Power Supply (4 Pins)** Must be the same voltage as VDD_IO. ***Note:*** *If stand-by power is implemented, power for these pins should be derived from the Vaux supply.*
PEX_VDDD0_P3 PEX_VDDD0_P2 PEX_VDDD0_P1 PEX_VDDD0_P0	DPWR	B51 B45 B12 B7	116 103 24 12	**1.0V SerDes Digital Power Supply (4 Pins)** ***Note:*** *If stand-by power is implemented, power for these pins should be derived from the Vaux supply.*
PEX_VDDD1_P3 PEX_VDDD1_P2 PEX_VDDD1_P1 PEX_VDDD1_P0	DPWR	B52 B46 A13 A7	119 106 21 9	**1.0V SerDes Digital Power Supply (4 Pins)** ***Note:*** *If stand-by power is implemented, power for these pins should be derived from the Vaux supply.*
PEX_VSSA_P3 PEX_VSSA_P2 PEX_VSSA_P1 PEX_VSSA_P0	GND	A58 A51 A15 A9	115 102 25 13	**SerDes Analog Ground (4 Pins)** Connect to VSS (Ground).
PEX_VSSD0_P3 PEX_VSSD0_P2 PEX_VSSD0_P1 PEX_VSSD0_P0	GND	B53 A54 A12 B5	120 107 20 8	**SerDes Digital Ground (4 Pins)** Connect to VSS (Ground).
PEX_VSSD1_P3 PEX_VSSD1_P2 PEX_VSSD1_P1 PEX_VSSD1_P0	GND	B54 B48 B9 B4	123 110 17 5	**SerDes Digital Ground (4 Pins)** Connect to VSS (Ground).
PLL_AGND	GND	B27	59	**PLL Analog Ground** Connect to VSS (Ground).
PLL_AVDD	PLLPWR	A31	58	**1.0V Analog Power for PLL Circuits** Connect to the main 1.0V supply (VDD_CORE) through an Inductor Capacitor (LC) filter circuit.
VAUX_CORE	CPWR	A10, A57, B49	15, 16, 112, 113	**Auxiliary Core Voltage (3 Pins (Dual-Row aQFN) or 4 Pins (Exposed Pad TQFP))** 1.0V, derived from Vaux. If standby power is not implemented, connect to VDD_CORE.
VAUX_IO	I/OPWR	A18, A26, A64, B19	33, 42, 49, 127	**Auxiliary I/O Power (4 Pins)** 2.5 or 3.3V, derived from Vaux. Must be the same voltage as VDD_IO. If standby power is not implemented, connect to VDD_IO.

Table 3-10. Power and Ground Signals – 51 Pins and Center Pad *(Cont.)*

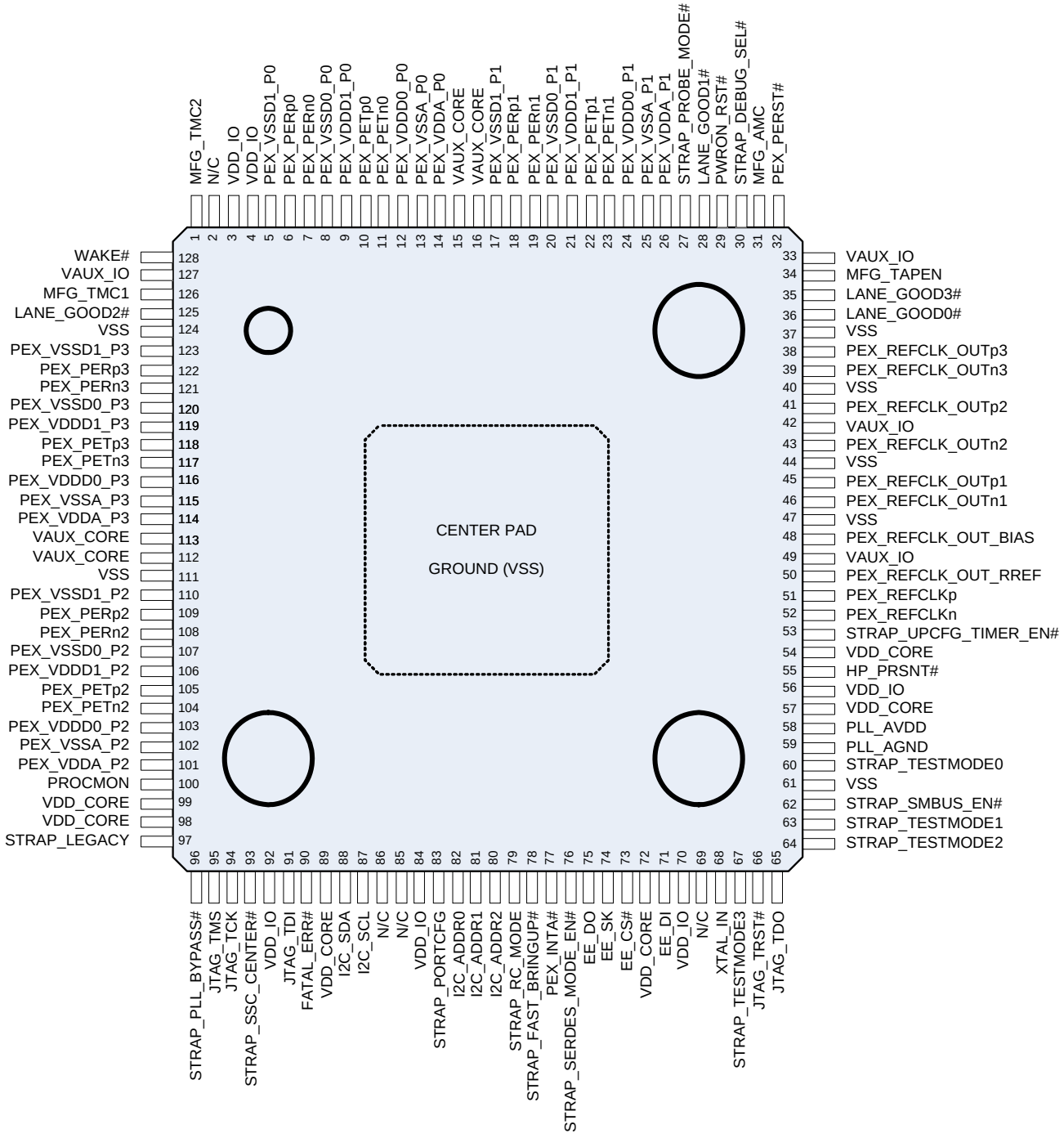
Signal Name	Type	Dual-Row aQFN Location	Exposed Pad TQFP Location	Description
VDD_CORE	CPWR	A29, A37, A46, A50, B26, B43	54, 57, 72, 89, 98, 99	**Core Logic Supply Voltage (6 Pins)** 0.95 to 1.10V.
VDD_IO	I/OPWR	A30, A43, B3, B31, B41	3, 4, 56, 70, 84, 92	**I/O Supply Voltage (5 Pins (Dual-Row aQFN) or 6 Pins (Exposed Pad TQFP))** 2.5 or 3.3V.
VSS	GND	A25, A32, A56, A63, B17, B18, B20	37, 40, 44, 47, 61, 111, 124	**Ground (7 Pins)**

3.5 Physical Layout

Figure 3-2. PEX 8605 Physical Signal Locations (Bottom View, as seen from Underside of Chip, 10 x 10 mm^2 Dual-Row aQFN Package)

Note: *Drawing not to scale.*

Figure 3-3. PEX 8605 Physical Signal Locations (Bottom View, as seen from Underside of Chip, 14 x 14 mm^2 Exposed Pad TQFP Package)



Note: *Drawing not to scale.*

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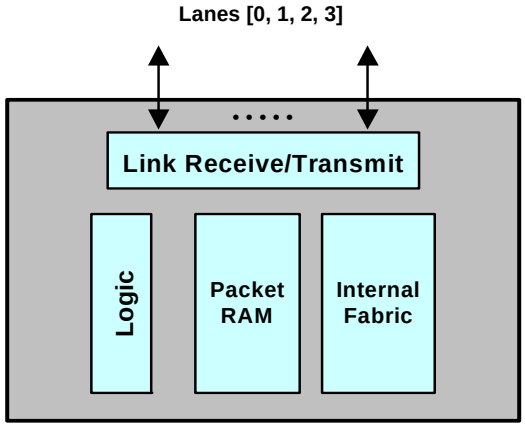
Chapter 4 Functional Overview

4.1 Hardware Architecture

The PEX 8605 is designed with a flexible, modular architecture. The four PCI Express Lanes are connected to one another by the internal fabric to the central RAM. Figure 4-1 provides a block diagram of the PEX 8605.

Figure 4-1. PEX 8605 Block Diagram



4.1.1 Port Functions

Each Port implements the *PCI Express Base r2.1* Physical, Data Link, and Transaction Layers (PHY, DLL, and TL, respectively). The PEX 8605 supports four integrated Serializer/De-Serializer (SerDes) modules, which provide the four PCI Express hardware interface Lanes. The Lanes can be combined, for a total of three to four Ports.

4.1.1.1 Port Configurations

The Port Link widths are initially defined by the STRAP_PORTCFG input, which is pulled or tied High to VDD_IO or Low to Ground. The serial EEPROM option can be used to re-configure the Ports, with the options defined in Table 4-1. Serial EEPROM configuration occurs following a Fundamental Reset, and overrides the configuration defined by STRAP_PORTCFG at that time. Port configuration can also be changed through the I^2C Slave interface. The final Link width can be automatically negotiated down from the programmed width, through Link-width negotiation for linkup to a device with fewer Lanes. The narrowest Port on one end of the Link determines the maximum Link width. Additionally, if a connection is broken on one of the Lanes, the training sequence removes the broken Lane and negotiates to a narrower width. A x2 Link Port can negotiate down to x1.

If the Port cannot train to x1 (Lane 0 is broken), the Port reverses its Lanes and attempts to retrain. *For example*, a x2 Link Port that cannot train to x2 attempts to negotiate down to x1; if x1 linkup fails, the Port reverses its Lanes and attempts again to negotiate linkup. Either the lowest Lane (Lane 0) or highest Lane (if Lanes are reversed) of the programmed Link width must connect to the other device's Lane 0.

Each Port can run independently at Gen 1 (2.5 GT/s) or Gen 2 (5.0 GT/s) Link speed.

Table 4-1 defines the PEX 8605 Port and Lane configurations. The Lanes are assigned to each enabled Port, in sequence. Ports that are not configured nor enabled are invisible to software.

Table 4-1. Port Configurations

STRAP_PORTCFG Value	Port 0	Port 1	Port 2	Port 3
(default) 0	x1	x1	x1	x1
(Lanes)	0	1	2	3
1	x2		x1	x1
(Lanes)	0-1		2	3

4.1.1.2 Port Numbering

The Port Numbers – 0, 1, 2, and 3 (defined in Table 4-1) have a direct relationship to the downstream Ports for the PCI Device Number assigned to the internal PCI-to-PCI bridges on the internal virtual PCI Bus. *For example*, if Port 1 is a downstream Port, the PCI-to-PCI bridge associated with that Port is Device Number 1. Each downstream Device Number matches its corresponding Port Number. Port 0 is the upstream Port, and Ports 1, 2, and 3 are the downstream Ports. The Device Numbers for the PCI-to-PCI bridges implemented on the downstream Ports are 1, 2, and 3, respectively.

The PCI-to-PCI bridge implemented on Port 0 does not assume a Device Number – it accepts the Device Number assigned by the upstream device. Generally, the upstream device assigns Device Number 0, according to the *PCI Express Base r2.1*.

4.1.2 General-Purpose Input/Output

The PEX 8605 provides four General-Purpose Input/Output (GPIO) pins (signals). As inputs, GPIO pins can sense external signals and generate interrupts on High or Low transitions. As outputs, GPIO pins can output a constant value (High or Low), or they can output a programmable pulse-width-modulated (PWM) output.

GPIO functions are described in Section 8.5, "General-Purpose Input/Output."

4.1.3 Reference Clock Outputs

The PEX 8605 provides three pairs of PCI Express-compliant, buffered, 100-MHz, HCSL output clocks, PEX_REFCLK_OUTn*x*/p*x*, one pair for each of its downstream Ports. Clock outputs are buffered versions of the input Reference Clock pair, PEX_REFCLKn/p.

Each clock output pair can be disabled by software or serial EEPROM when not in use, for additional power savings, by Clearing their **Clock Enable** register *REFCLK x Enable* bit (Port 0, offset 1D8h[10:8])

It is recommended that system designs that make use of PEX_REFCLK_OUT outputs limit their total PC board trace lengths to approximately 10 inches or less, with one connector.

4.1.4 I^2C/SMBus Slave Interface

The PEX 8605 provides an I^2C/SMBus Slave interface. This interface can be used to access internal registers and other debug features of the PEX 8605, independently of the PCI Express interface.

I^2C/SMBus functions are described in Chapter 7, "I2C/SMBus Slave Interface Operation."

4.2 PCI Express Link Functional Description

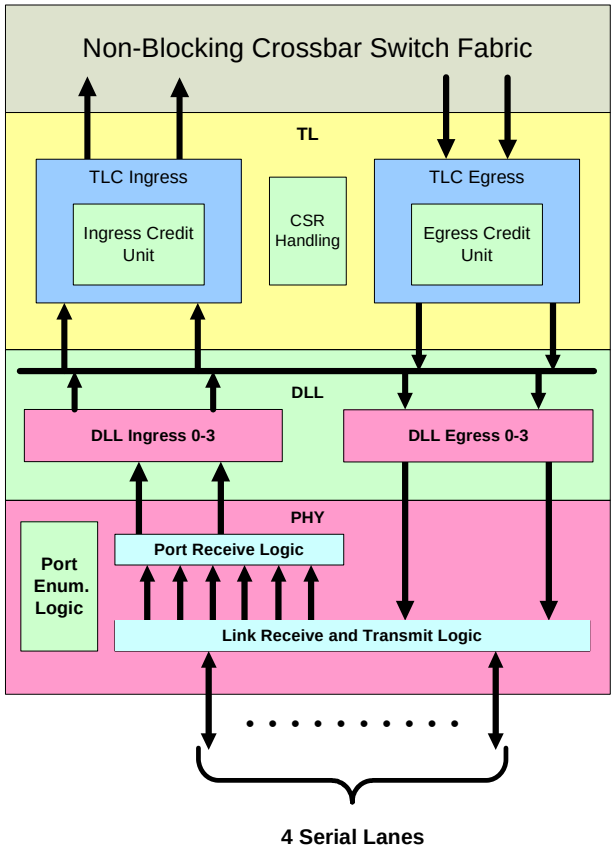
The PEX 8605 groups four SerDes together, which can comprise a total of three to four Ports. (Refer to Table 4-1.) The Ports forward ingress packets to the internal fabric and central RAM, and pull egress packets from the central RAM to send out of the PEX 8605.

The PEX 8605 implements the PCI Express PHY and DLL functions for each of its Ports, and aggregates traffic from these Ports onto a transaction-based, non-blocking internal crossbar fabric. All packet queuing and ordering aspects of this layer are handled by the Crossbar Switch Control blocks.

During system initialization, software initiates Configuration Requests that set up the PCI Express interfaces, Device Numbers, and Address maps across the various Ports. These maps are used to direct traffic between Ports during standard system operation. Traffic flow between the Ports is supported through the central internal fabric.

At the top level, the PEX 8605 has a layered organization consisting of the PHY, DLL, and TL blocks, as illustrated in Figure 4-2. The PHY and DLL blocks have Port-specific data paths (one per PCI Express Port) that operate independently of one another. The Transaction Layer Control (TLC) ingress section of the TL block aggregates traffic for all ingress Ports, and then sends the traffic to the internal crossbar fabric. The TLC egress section of the TL block accepts packets, by way of the internal crossbar fabric, from all ingress Ports, and schedules them to be sent out the appropriate egress Port.

Figure 4-2. PCI Express Block Diagram



4.3 Physical Layer

The Physical Layer (PHY) converts information received from the DLL into an appropriate serialized format and transmits it across the PCI Express Link. The PHY also receives the serialized input from the Serializer/De-Serializer (SerDes), converts it to parallel data (internal Data Bus), then writes it to the Transaction Layer Control (TLC) Ingress buffer.

The PHY includes all circuitry for PCI Express Link Interface operation, including:

- Driver and Input buffers
- Parallel-to-serial and serial-to-parallel conversion
- Phase-Locked Loops (PLLs) and clock circuitry
- Impedance Matching circuitry
- Interface Initialization and Maintenance functions

The PHY module interfaces to the PCI Express Lanes and implements the PHY functions. The quantity of available PCI Express Ports is three to four, with a cumulative Lane bandwidth of x4. PHY functions include:

- SerDes modules, which provide functions required by the *PCI Express Base r2.1*
- User-configurable Port division
- Link widths – x1 or x2
- Link speeds supported – 2.5 and 5.0 GT/s
- Hardware Link training and initialization
- Hardware detection of polarity reversal
- Hardware detection of Lane reversal (Port 0 only, when Port 0 is configured with a x2 Link width)
- Hardware Autonomous Speed Control supported
- Dynamic Link speed control supported
- Dynamic Link width supported
- Data scrambling/de-scrambling and 8b/10b encode/decode
- Packet framing
- Loopback Master and Slave support
- Programmable test pattern with SKIP Ordered-Set insertion and return data checking
- Receiver error checking (Elastic buffer over/underflow, disparity, and symbol encoding)
- Modified Compliance Pattern support with Receiver Error Counters, per Lane
- Link state Power Management (PM) – Supports L0, L0s, L1, L2, L2/L3 Ready, and L3 Link PM states
- Supports cross-linked Port 0 and downstream Ports

4.3.1 PHY Status and Command Registers

The PHY operating conditions are defined in:

- Section 11.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)"
- Section 11.16.7, "Device-Specific Registers – Physical Layer (Offsets B80h – B88h)"

The System Host can track the Link operating status and re-configure Link parameters, by way of these registers.

4.3.2 Hardware Link Interface Configuration

The PHY can include up to four integrated SerDes modules, which provide the PCI Express hardware interface Lanes. The SerDes modules also provide all physical communication controls and functions required by the *PCI Express Base r2.1*, as well as the Links (clustered into Ports) that connect the PEX 8605 to other PCI Express devices.

The quantity of enabled Ports, and Link widths associated with those Ports, are configurable, on a Port-by-Port basis. Initial Port configuration is determined by Strapped signal pins, serial EEPROM, or auto Link-width negotiation. If the PEX 8605 Ports are configured using the auto-negotiation process, the Link widths can narrow or widen (by combining multiple adjacent Lanes).

4.4 Transaction Layer

The upper layer of the architecture is the Transaction Layer (TL). The TL assembles and disassembles TLPs, which are used to communicate transactions, *such as* Read and Write, as well as certain types of events. The TL also manages credit-based FC for TLPs.

The TL supports four Address spaces – it includes the three PCI Address spaces (Memory, I/O, and Configuration) and adds a Message space. (Refer to Table 4-2.) This specification uses Message space to support all prior sideband signals, *such as* interrupts, Power Management (PM) Requests, and so forth, as in-band Message transactions. PCI Express Message transactions are considered *virtual wires* that support *virtual pins*. As virtual wires, Assert and De-assert Messages are sent when a triggering event changes the state of the wire.

Table 4-2. Address Spaces Support Differing Transaction Types

Address Space	Transaction Types	Transaction Functions
Configuration	Read/Write	Device configuration or setup
Input/Output		Transfers data from/to an I/O space
Memory		Transfers data from/to a memory location
Message	Baseline/Virtual Wires	General-purpose Messages Event signaling (status, interrupts, and so forth)

All Request packets requiring a Response packet are implemented as Split Transactions. Each packet has a unique identifier that enables Response packets to be directed to the correct originator. The packet format supports various forms of addressing, depending upon the transaction type – *Memory*, *I/O*, *Configuration*, or *Message*.

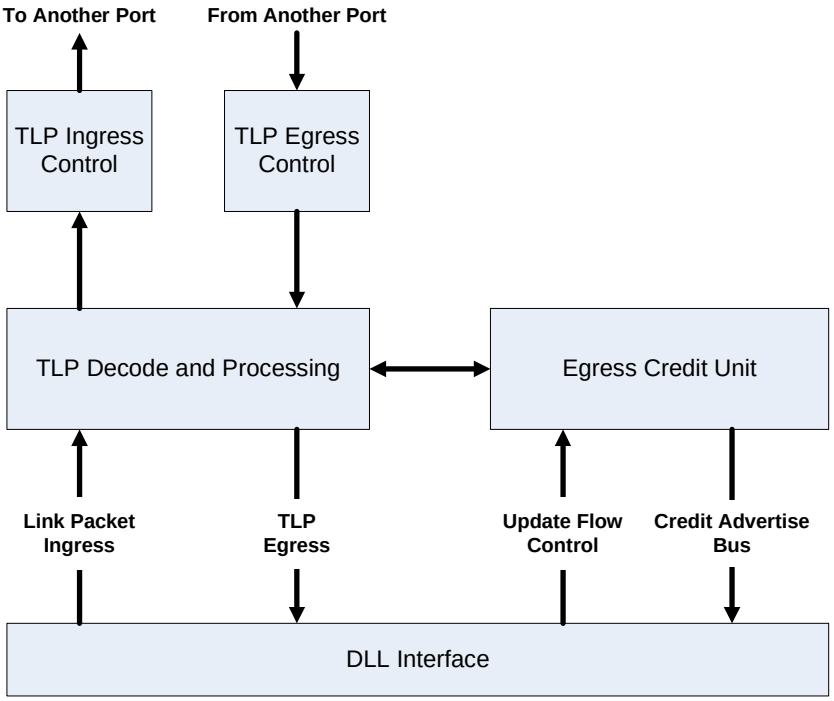
TL functions include:

- Decoding and checking rules for the incoming TLP
- Memory-Mapped Configuration Space register (CSR) access
- Checking incoming packets for malformed or unsupported packets
- Data Poisoning and end-to-end data integrity detection
- Error logging and reporting for incoming packets
- TLP dispatching
- Write control to the packet RAM and packet Link List RAM
- Destination lookup and TC-VC mapping
- Credit-based scheduling
- Pipelined full Split Transaction protocol
- PCI/PCI-X-compatible ordering
- Interrupt handling (INT*x* or MSI)
- Power Management (PM) support
- Hot Plug support
- Link State event support
- QoS support
- Ordering
- Ingress and Egress credit management

The PEX 8605 does ***not support*** Locked transactions. This is consistent with limitations for Locked transaction use, as outlined in the *PCI r3.0* (Appendix F, "Exclusive Accesses"), and prevents potential deadlock, as well as serious performance degradation, that could occur with Locked transaction use. The PEX 8605 responds to "lock"-type Read Requests (MRdLk) with a Completion with UR status.

The hardware functions provided by the PEX 8605 to implement *PCI Express Base r2.1* TL requirements are illustrated in Figure 4-3. The blocks provide a combination of Ingress and Egress control, as well as the data management at each stage in the flow sequence.

Figure 4-3. TL Controller



4.4.1 TL Receive/Ingress Protocol

The ingress side TL collects and stores inbound TLP traffic in the packet RAM. The incoming data is checked for valid type field, length matching the Header *Transfer Size* field, and other TLP-specific errors defined by the *PCI Express Base r2.1*.

Header and Data Payload information is forwarded to the Source Scheduler, to be routed across the internal fabric, to the egress Port.

4.4.2 Flow Control Credit Initialization

The initial quantity of VC0 Flow Control (FC) credits is advertised as programmed for each type of Header and Payload. After VC0 FC initialization is complete, the FC credits received are transferred to the TL egress. The TL ingress must schedule an UpdateFC Data Link Layer Packet (DLLP) for transmission, to increase the quantity of advertised credits.

4.4.3 Flow Control Protocol

The PEX 8605 implements FC protocol that ensures that the switch:

- Does not transmit a TLP over a Link to a remote Receiver, unless the receiving device has sufficient VC Buffer space to accommodate the packet
- Generates FC credit updates to the remote Transmitter, to replace credits used to send TLPs to the PEX 8605

This FC is automatically managed by the hardware, and is transparent to software. Software is used only to enable additional Buffer space, to supplement the initial default buffer assignment.

The initial default FC credits, which are enabled after Link training, allow TLP traffic immediately after Link training completes. The Configuration transactions are the first transactions to use the default VC credits, to set up the initial device operating modes and capabilities.

The TL Ingress Credit Unit transmits DLLPs (referred to as *FC packets*) that update the FC to the remote Transmitter device, on a periodic basis. The DLLPs contain FC credit information that updates the Transmitter regarding the amount of available Buffer space in the PEX 8605.

The TL Egress Credit Unit receives DLLPs from the remote device, indicating the amount of Buffer space available in the remote Receiver. The unit uses this credit information to schedule the sending of TLPs to the remote device.

4.5 PCI-Compatible Software Model

The PEX 8605 can be thought of as a hierarchy of PCI-to-PCI bridges, with one upstream PCI-to-PCI bridge and one or more downstream PCI-to-PCI bridges connected by an internal virtual bus. (Refer to Figure 4-4.) PCI-to-PCI bridges are compliant with the PCI and PCI Express system models. Figure 4-4 illustrates the concept of hierarchical PCI-to-PCI bridges, with the bus in the middle being the internal virtual PCI Bus. The Configuration Space registers (CSRs) in the upstream PCI-to-PCI bridge are accessible by Type 0 Configuration Requests that target the upstream bus interface. Port 0 captures the Type 0 Configuration Write Target Bus Number and Device Number. Port 0 uses this Captured Bus Number and Captured Device Number as part of the Requester ID and Completer ID for the Requests and Completions generated by Port 0.

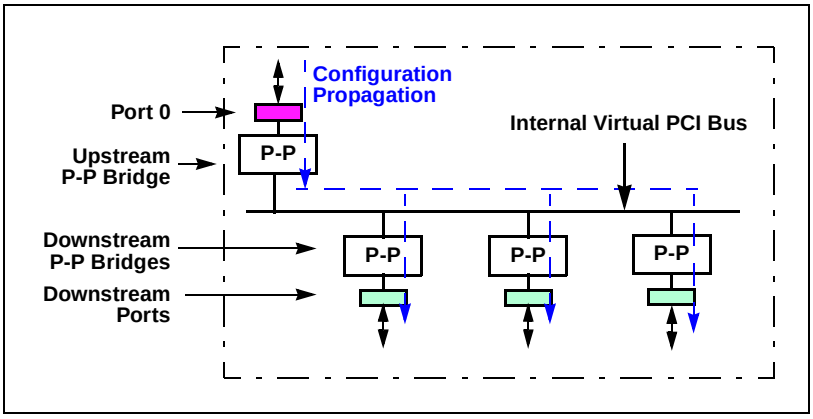
The CSRs in the downstream Port PCI-to-PCI bridges are accessible by Type 1 Configuration Requests received at Port 0 that target the internal virtual PCI Bus, by having a Bus Number value that matches the upstream bridge's Secondary Bus Number value. Each downstream bridge is associated with a unique Device Number, as explained in Section 4.1.1.

The CSRs of downstream devices are hit in two ways. If the Configuration Request matches the PEX 8605 downstream Port Secondary Bus Number, the PEX 8605 converts the Type 1 Configuration Request into a Type 0 Configuration Request. However, if the Bus Number does ***not*** match the Secondary Bus Number, but falls within the Subordinate Bus Number range, the Type 1 Configuration Request is forwarded out of the PEX 8605, unchanged. A Type 1 Configuration Request that targets a Bus Number that is not within range is invalid, and is terminated by Port 0 as an Unsupported Request (UR).

After all PCI devices have been located and each assigned a Bus Number and Device Number, software can assign a Memory map and I/O map. Requests (Memory or I/O) go downstream if they fall within a bridge's Base and Limit range. In the PEX 8605, each downstream bridge has its own Base and Limit. Alternatively, Requests (Memory or I/O) go upstream if they do not target anything within the upstream bridge's Base and Limit range.

Completions are routed by the Bus Number established in the Configuration registers. If the Bus Number is in the Secondary or Subordinate range, the packet goes downstream; otherwise, the packet goes upstream.

Figure 4-4. PEX 8605 System Configuration Propagation



Chapter 5 Reset and Initialization

5.1 Reset

This section describes the resets that the PEX 8605 supports. (Refer to Table 5-1.) *Reset* is a mechanism that returns a device to its initial state. Reset is propagated from upstream to downstream. Hardware or software mechanisms can trigger four different levels of reset – Fundamental, Power On, Hot, or Secondary Bus (each is described in the sections that follow). The re-initialized states following a reset vary, depending upon the reset type.

Table 5-1. Reset Summary

PCI Express Definition	Reset Source	Impact to Different Internal Components (upon De-Assertion)	Impact to Internal Registers
Fundamental Reset • Cold Reset • Warm Reset	PEX_PERST# input assertion	• Initializes everything • Serial EEPROM contents are loaded • HwInit types are evaluated	All registers are initialized
Power-On Reset	PWRON_RST#, generated from connector Vaux supply	• Used as the reset to logic operating on Vaux	Auxiliary power logic is initialized. Must be held logic High when in the D3cold state, to support Wakeup operation. When support for wakeup from the D3cold state is not needed, connect PWRON_RST# to PEX_PERST#.
Hot Reset	• TS Ordered-Set *Hot Reset* bit is Set, at Port 0 • Port 0 enters the *DL_Down* state	• Initializes all Ports • Initializes internal credits and queues • Selectively reloads serial EEPROM contents	All registers, except: • Port Configuration registers • All Sticky bits not affected by Hot Reset (HwInit, ROS, RW1CS, RWS)
Secondary Bus Reset	**Bridge Control** register *Secondary Bus Reset* bit (Downstream Ports, offset 3Ch[22]) is Set	• Downstream Port PHY generates a Hot Reset • Downstream Port Data Link Layer (DLL) is down • Downstream Port Transaction Layer (TL) is initialized, exhibits DL_Down behavior, and TLP Requests to that Port are dropped • Port 0 and downstream Ports drain traffic, corresponding to the DL_Down condition on the downstream Port, and initialize credits corresponding to that downstream Port	Does not affect registers (other than to initialize credits)
	Bridge Control register *Secondary Bus Reset* bit (Port 0, offset 3Ch[22]) is Set	• All downstream Ports propagate a Hot Reset • DLL of each downstream Port is down • TL of each downstream Port is initialized, exhibits DL_Down behavior, and drops TLP Requests that target downstream Ports • Port 0 TL exhibits DL_Up behavior	Initializes downstream Ports registers to default values

5.1.1 Fundamental Reset

Fundamental Reset is a hardware mechanism defined by the *PCI Express Base r2.1*, Section 6.6. Fundamental Reset input, through the PEX_PERST# input, resets all Port states and Configuration registers to default conditions. Reset remains asserted until PEX_PERST# is de-asserted.

5.1.2 Power-On Reset

The PEX 8605 implements a Power-On Reset input, which is mainly used to reset the D3cold-operated auxiliary powered circuit inside the PEX 8605. For systems where wakeup is supported when in the D3cold state, this reset must be held High when in D3cold. In such cases, PWRON_RST# is mostly derived from the Vaux supply, from the PCI Express connector.

For systems that do not support the Wakeup event in the D3cold state, PWRON_RST# input can be tied to PEX_PERST# on the PCI Express connector. In such systems, the maximum allowed skew between PWRON_RST# and PEX_PERST# pins to the PEX 8605 is 50 ns.

5.1.3 Hot Reset

Hot Reset is an in-band Reset that propagates from an upstream PCI Express Link to all its downstream Ports, through the Physical Layer (PHY) mechanism. The PHY mechanism communicates a reset to downstream devices through a training sequence (TS1/TS2 Ordered-Set, in which the *Hot Reset* Training Control Bit is Set). Hot Reset is also referred to as a *Soft Reset*.

A Hot Reset initializes all Ports, resets registers that are not defined as Sticky, and resets the serial EEPROM logic to reload registers (except Port Configuration registers) from serial EEPROM, if present[a]. Hot Reset does not reset the Clock logic, and can be caused by any of the following:

- Port 0 PHY receives two consecutive TS1 Ordered-Sets in which the *Hot Reset* Training Control Bit is Set. Hot Reset is generated from an upstream device, *such as* by Setting its **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).
- Port 0 unexpectedly enters the *DL_Down* state.

  Exception – If the Port 0 Link is in the L2 Link PM state and the Link goes down, the downstream Ports do ***not*** generate Hot Reset.
- Port 0 PHY enters either the *Loopback* or *Disabled* state, upon receiving two consecutive TS1 or TS2 Ordered-Sets in which either the *Loopback* or *Disable Link* Training Control Bit is Set, respectively. An upstream device can generate the *Disable Link* sequence, by Setting its **Link Control** register *Link Disable* bit (offset 78h[4]).

*a. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its Status register. This value is copied to the **Serial EEPROM Status** register Status Data from Serial EEPROM fields (Port 0, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present.*

5.1.4 Secondary Bus Reset

Any virtual upstream or downstream PCI-to-PCI bridge within the PEX 8605 can reset its downstream hierarchy, by Setting the **Bridge Control** register *Secondary Bus Reset* bit (All Ports, offset 3Ch[22]).

When the *Secondary Bus Reset* bit is Set on Port 0, all the downstream Ports are initialized to their default states, as defined by the *PCI Express Base r2.1*. Each of the downstream Ports generates an in-band Hot Reset onto its downstream Links. In addition, writable registers (registers with the RW attribute) defined by the *PCI Express Base r2.1*, in all downstream Ports, are initialized to default values (Port 0 registers are not reset, and the serial EEPROM does not reload registers).

When the *Secondary Bus Reset* bit is Set on a downstream Port, that Port is reset to its default state as defined by the *PCI Express Base r2.1*, and generates an in-band Hot Reset onto its downstream Link. The registers of that downstream Port are not affected.

5.1.5 Register Bits that Affect Hot Reset

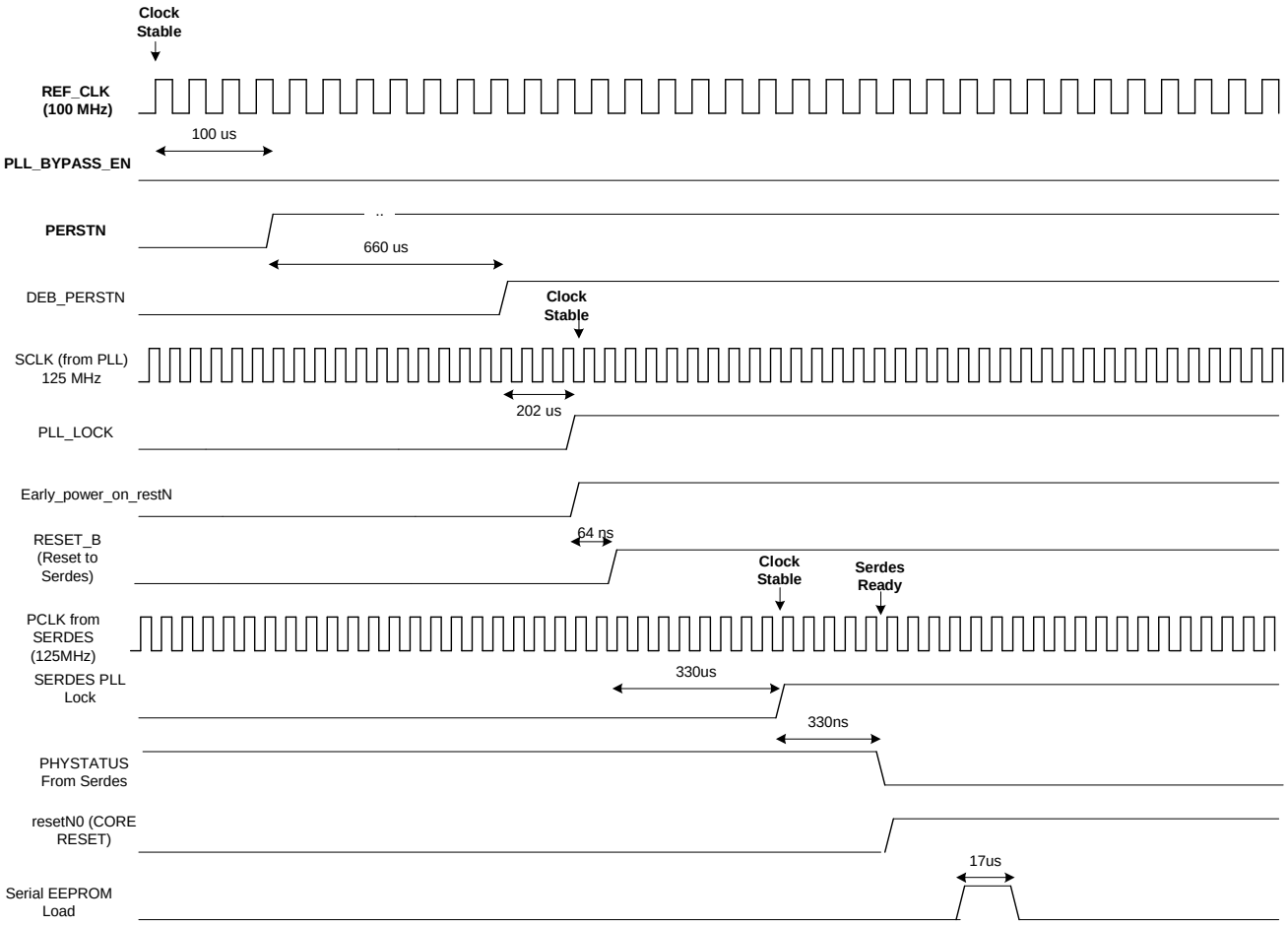
Setting the **Bridge Control** register *Secondary Bus Reset* bit (All Ports, offset 3Ch[22]) generates a Hot Reset to downstream Ports and downstream devices.

5.1.6 Reset and Clock Initialization Timing

Table 5-2. Reset and Clock Initialization Timing

Symbol	Description	Typical Delay
td1	REFCLK stable to PEX_Reset release time	100 µs
td2	PEX_Reset release to Reset de-bounce	660 µs
td3	Reset de-bounce to Phase-Locked Loop (PLL) Lock	202 µs
td4	Reset de-bounce to Core Reset release	331 µs
td5	Serial EEPROM load time with no serial EEPROM present	17 µs

Figure 5-1. Initialization – Reset and Clock Timing (with Internal PLL)



5.2 Initialization Procedure

The PEX 8605 initialization process starts upon exit from a Fundamental Reset. There are two or more steps in the process, depending upon the availability of an external initialization serial EEPROM and I^2C.

The initialization sequence executed is as follows:

1. PEX 8605 reads the Strapping input Lane configuration (STRAP_PORTCFG) of each enabled Port.
2. If a serial EEPROM is present, serial EEPROM data is downloaded to the PEX 8605 Configuration registers. The configuration from STRAP_PORTCFG can be changed by serial EEPROM data.

   Alternatively, I^2C can be used to program all the registers to configure the PEX 8605 (the same as would be done with the serial EEPROM), except, if PHY or DLL register values that affect SerDes parameters or Link initialization need to be changed, those registers must be programmed by serial EEPROM, so that the values are loaded prior to initial Link training. Because I^2C is relatively slow, the Links are usually up by the time the first I^2C Write occurs. The first I^2C command might be to block system access while the configuration is being changed, by disabling Port 0; Ports can be disabled, by Setting the Port's **Port Control** register *Disable Port x* bit (Port 0, offset 234h[19:16]).

   Switch configuration, including Port Configuration (Port 0, offset 574h[0]), can be changed by I^2C and/or serial EEPROM reload. Changes take effect upon subsequent Hot Reset.

Note: *As described in Chapter 7, "I2C/SMBus Slave Interface Operation," an external I^2C Master can send the register Read/Write Requests to PEX 8605 after reset. To prevent conflict, first Set the Disable Port 0 bit. Restoration of Port 0 should be the last register Write of the entire I^2C programming procedure.*

3. After configuration from the Strapping inputs, serial EEPROM, and/or I^2C is complete, the Physical Layer (PHY) of the configured Ports attempts to bring up the Links. After both components on a Link enter the initial Link Training state, the components proceed through PHY Link initialization and then through Flow Control initialization for VC0, preparing the DLL and TL to use the Link. Following Flow Control initialization for VC0, it is possible for VC0 TLP and DLL Packets (DLLPs) to be transmitted across the Link.

5.2.1 Default Port Configuration

The upstream Port is fixed at Port 0, and cannot be changed by Strapping inputs, I^2C, and/or serial EEPROM. Port configuration of the downstream Ports/overall Link width configuration is determined by the Strapping inputs, which must be pulled or tied High to VDD_IO or Low to Ground, to define the default device configuration. (Refer to Section 3.4.3, "Strapping Signals.") The configuration defined by the Strapping inputs can be changed by downloading serial EEPROM data, and/or by I^2C programming followed by a Hot Reset.

5.2.2 Default Register Initialization

Each PEX 8605 Port defined in the Port Configuration process has a set of assigned registers that control Port activities and status during standard operation. These registers are programmed to default/ initial values, as defined in Chapter 11, "Registers."

Following a Fundamental Reset, the basic PCI Express Support registers are initially programmed to the values specified in the *PCI Express Base r2.1*. The Device-Specific registers are programmed to the values specified in their register description tables. These registers can be changed by loading new data with the attached serial EEPROM, the I^2C Slave interface, or by CSR accesses using Configuration or Memory Writes; however, registers identified as RO ***cannot*** be modified by Configuration nor Memory Write Requests.

The Ports support the following mechanisms for accessing registers by way of the TL, as described in:

- Section 11.4.1, "PCI r3.0-Compatible Configuration Mechanism"
- Section 11.4.2, "PCI Express Enhanced Configuration Access Mechanism"
- Section 11.4.3, "Device-Specific Memory-Mapped Configuration Mechanism"

5.2.3 Device-Specific Registers

The Device-Specific registers are unique to the PEX 8605, and are not referenced in the *PCI Express Base r2.1*. The registers are organized into the following sections:

- Section 11.14, "Device-Specific Registers (Offsets 1C0h – 444h)"
- Section 11.16, "Device-Specific Registers (Offsets 530h – B88h)"

5.2.4 Serial EEPROM Load Time

Serial EEPROM initialization loads only the Configuration register data that is specifically programmed into the serial EEPROM. Registers that are not included in the serial EEPROM data are initialized to default register values.

Each register entry in the serial EEPROM consists of two Address bytes and four Data bytes (refer to Section 6.4, "Serial EEPROM Data Format"); therefore, each register entry (6 bytes, or 48 bits) requires 48 serial EEPROM clocks to download. Thus, at the serial EEPROM clock default frequency of 1 MHz, after initial overhead to read the **Serial EEPROM Status** register (Port 0, offset 260h) (16 serial EEPROM clocks, or 16 µs), plus another 40 serial EEPROM clocks (40 µs) to begin reading the register data, each register entry in the serial EEPROM requires 48 µs to download. A serial EEPROM containing 50 register entries (typical configuration, assuming the serial EEPROM is programmed only with non-default register values) and clocked at 1 MHz takes approximately 2.5 ms to load (16 + 40 + (48 x 50 µs)) = 2,456 µs).

To reduce the serial EEPROM initialization time, the first register entry in the serial EEPROM can increase the clock frequency, by programming the **Serial EEPROM Clock Frequency** register (Port 0, offset 268h) to a value of 2h (5 MHz), or 3h (9.62 MHz), if the serial EEPROM supports the higher frequency at the serial EEPROM supply voltage (typically 2.5 or 3.3V). At 5-MHz clocking, the serial EEPROM load time for 50 register entries can be reduced to approximately 575 µs. Because the *PCI Express Base r2.1* allows a 20-ms budget for system hardware initialization, the default 1-MHz serial EEPROM clock is often sufficient when the quantity of Ports and registers programmed by serial EEPROM is relatively small.

For further details, refer to Chapter 6, "Serial EEPROM Controller."

5.2.5 I^2C Load Time

Initialization using I^2C is slower than serial EEPROM initialization, because the I^2C Slave interface operates at a lower clock frequency (100 KHz maximum) and the quantity of bits per Register access is increased (because the Device address is included in the bit stream). Writing one register using 100-KHz clocking takes approximately 830 µs (83 clock periods).

For further details, refer to Section 7.2, "I2C Slave Interface."

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Chapter 6 Serial EEPROM Controller

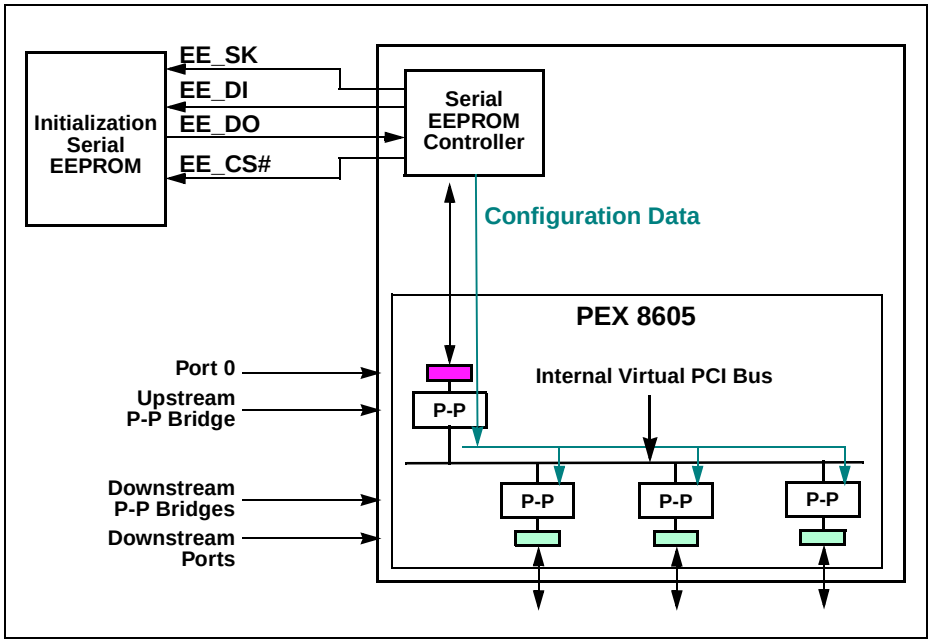
6.1 Overview

The PEX 8605 provides a Serial EEPROM Controller and interface to Serial Peripheral Interface (SPI)-compatible serial EEPROMs, as illustrated in Figure 6-1. The interface consists of a Chip Select, Clock and Write Data outputs, and a Read Data input, and operates at a programmable frequency of up to 17.86 MHz. The PEX 8605 supports serial EEPROMs that use 1-, 2-, or 3-byte addressing (2-byte addressing is recommended); the PEX 8605 automatically determines the appropriate addressing mode.

The controller provides access to non-volatile memory. This external memory can be used for the following purposes:

- The serial EEPROM can be used to store register data, for switch configuration and initialization. When a serial EEPROM device is connected to the PEX 8605, immediately after reset, the Serial EEPROM Controller reads data from the serial EEPROM that is used to update the PEX 8605 register default values.
- System or application data can be stored into, and read from, the serial EEPROM, by software, I^2C and/or SMBus, initiating random-access Read or Write Requests to the serial EEPROM.

Figure 6-1. Serial EEPROM Connections



6.2 Features

- Detection of whether a serial EEPROM is present/not present
- Supports high-speed serial EEPROMs with Serial Peripheral Interface (SPI) interface
- Non-volatile storage for register default values loaded during Power-On Reset
- 4-byte Read/Write access to the serial EEPROM, through Port 0
- Serial EEPROM data format allows for loading registers by Port/Address location
- Required serial EEPROM size is dependent upon the number of registers being changed
- Automatic support for 1-, 2-, or 3-byte-addressable serial EEPROMs
- Manual override for quantity of serial EEPROM Address bytes
- Programmable serial EEPROM clock frequency
- Programmable serial EEPROM clock-to-chip select timings
- No Cyclic Redundancy Check (CRC), single *Valid* byte at the start of serial EEPROM memory

6.3 Serial EEPROM Load following Port 0 Reset

The Serial EEPROM Controller performs a serial EEPROM download when the following conditions exist:

- Serial EEPROM is present[a], and
- Validation signature (first byte read from the serial EEPROM) value is 5Ah, and
- One of the following events occur:
  - PEX_PERST# is returned High, following a Fundamental Reset (*such as*, a Cold or Warm Reset to the entire PEX 8605)
  - Hot Reset is received at Port 0 (downloading upon this event can be optionally disabled, by Setting the **Debug Control** register *Disable Serial EEPROM Load on Hot Reset* and/or *Upstream Hot Reset Control* bit (Port 0, offset 1DCh[17 and/or 16], respectively))
  - Port 0 exits a *DL_Down* state (downloading upon this event can be optionally disabled by Setting the **Debug Control** register *Upstream Port DL_Down Reset Propagation Disable* and/or *Upstream Hot Reset Control* bit (Port 0, offset 1DCh[20 and/or 16], respectively))

*a. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its Status register. This value is copied to the **Serial EEPROM Status** register Status Data from Serial EEPROM fields (Port 0, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present.*

6.4 Serial EEPROM Data Format

The data in the serial EEPROM is stored in the format defined in Table 6-1. The Validation Signature byte is located in the first address. The Serial EEPROM Controller reads this byte to determine whether a valid serial EEPROM image exists versus a blank image. REG_BYTE_COUNT[15:0] contains the quantity of bytes of serial EEPROM data to be loaded. It is equal to the quantity of registers to be loaded times 6 (6 serial EEPROM bytes per register). If the REG_BYTE_COUNT[15:0] value is not a multiple of 6, the last incomplete register entry is ignored.

For the remaining register-related locations, data is written into a 2-byte address that represents the Configuration register offset and Port Number, and the 4 bytes following are the data loaded for that Configuration register. Only Configuration register data specifically programmed into the serial EEPROM is loaded after the PEX 8605 exits reset.

Table 6-2 defines the Configuration register Address format (REGADDR[15:0] from Table 6-1):

- Bits [9:0] represent bits [11:2] of the Register address
- Bits [15:10] represent the Port Number of the register selected to be programmed by serial EEPROM

Because the PEX 8605 Serial EEPROM Controller always accesses 4 bytes of serial EEPROM data (for DWord-aligned Register addresses), register offsets are stored in the serial EEPROM as DWord address values.

To determine the 2-byte serial EEPROM value that represents the PEX 8605 Port and register offset, shift the register offset 2 bits to the right (divide by 4), then OR the resulting value with the appropriate Port Identifier value from Table 6-2.

For example, to load Port 2 register offset 1F8h, shift the address to the right by 2 bits (this becomes 07Eh) and concatenate 0001_00b. The resulting DWord address in the serial EEPROM will be 0001_0000_0111_1110b, which is 107Eh.

Table 6-1. Serial EEPROM Data Format

Location	Value	Description
0h	5Ah	Validation Signature
1h	00h	***Reserved***
2h	REG_BYTE_COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG_BYTE_COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
Eh	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
…	…	…
FFFFh	REGDATA (Byte 3)	Last Configuration Register Data (Byte 3)

Note: *The first Configuration register programmed by the serial EEPROM **must** be the **Debug Control** register (Port 0, offset 1DCh), serial EEPROM locations 4h through 9h, as listed in Table 6-1.*

Table 6-2. Configuration Register Address Format

Port Number	REGADDR Bits [15:10] Value[a]	Port Identifier
Port 0	0000_00b	0000h
Port 1	0000_01b	0400h
Port 2	0000_10b	0800h
Port 3	0000_11b	0C00h

*a. Encodings not listed are **reserved**.*

6.5 Serial EEPROM Initialization

After the device Reset is de-asserted, the PEX 8605 determines whether a serial EEPROM is present. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its **Status** register. This value is copied to the **Serial EEPROM Status** register *Status Data from Serial EEPROM* fields (Port 0, offset 260h[31:24]). Serial EEPROM presence is reported in the register's *EepPrsnt[1:0]* field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present. A pull-up resistor on the EE_DO input produces a value of FFh if a serial EEPROM is not installed.

If a serial EEPROM is detected, the first byte (validation signature) is read. If a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8605. The serial EEPROM address width is determined while the first byte is read. If the first byte's value is not 5Ah, the serial EEPROM is blank or programmed with invalid data. In this case, no more data is read from the serial EEPROM, and the **Serial EEPROM Status** register *EepAddrWidth* field (Port 0, offset 260h[23:22]) reports a value of 00b (undetermined width).

If the *EepAddrWidth* field reports a value of 00b, any subsequent accesses to the serial EEPROM (through the PEX 8605 Serial EEPROM registers) default to a serial EEPROM address width of 1 byte unless the **Serial EEPROM Status** register *EepAddrWidth Override* bit (Port 0, offset 260h[21]) is Set. The *EepAddrWidth* field is usually Read-Only; however, it is writable if the *EepAddrWidth Override* bit is Set (both can be programmed by a single Write instruction).

If the serial EEPROM contains valid data, the REG_BYTE_COUNT values in Bytes 2 and 3 determine the quantity of serial EEPROM locations that contain Configuration register addresses and data. Each Configuration register entry consists of 2 bytes of register Address and 4 bytes of register Write data. The REG_BYTE_COUNT must be a multiple of 6.

The EE_SK output clock frequency is determined by the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, offset 268h[2:0]). The default clock frequency is 1 MHz. At this clock rate, it takes approximately 48 µs per DWORD during Configuration register initialization. For faster loading of large serial EEPROMs that support a faster clock, the first Configuration register load from the serial EEPROM could be to the **Serial EEPROM Clock Frequency** register.

6.6 PCI Express Configuration, Control, and Status Registers

The PCI Express Configuration, Control, and Status registers that can be initialized are detailed in Chapter 11, "Registers."

6.7 Serial EEPROM Registers

The Serial EEPROM register (Port 0, offsets 260h through 26Ch) parameters defined in Section 11.14.3, "Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)," can be changed, using the serial EEPROM. It is recommended that the first serial EEPROM entry (after the pair of **Debug Control** register (Port 0, offset 1DCh) entries, if programmed), be used to change the value in the **Serial EEPROM Clock Frequency** register (Port 0, offset 268h) to increase the clock frequency, and thereby reduce the time needed for the remainder of the serial EEPROM load. At the last serial EEPROM entry, the **Serial EEPROM Status and Control** register (Port 0, offset 260h) can be programmed to issue a Write Status (WRSR) command, to enable the write protection feature(s) within the serial EEPROM data, if needed.

6.8 Serial EEPROM Random Read/Write Access

To access the serial EEPROM, a PCI Express, I^2C, or SMBus Master uses the following registers:

- **Serial EEPROM Status and Control** (Port 0, offset 260h)
- **Serial EEPROM Buffer** (Port 0, offset 264h)
- **Serial EEPROM 3rd Address Byte** (Port 0, offset 26Ch)

The Master can only access the serial EEPROM on a DWord basis (4 bytes aligned to one DWord address).

6.8.1 Writing to Serial EEPROM

To write a DWord to the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (Port 0, offset 260h[23:22]) are both Set), write the value to the *Serial EEPROM 3rd Address Byte* field (Port 0, offset 26Ch[7:0]).
2. Write the 32-bit data into the **Serial EEPROM Buffer** register (Port 0, offset 264h).
3. Issue a Write Enable instruction to the serial EEPROM (Command = 110b, Set Write Enable Latch), by writing the value 0000_C000h into the **Serial EEPROM Status and Control** register (Port 0, offset 260h).
4. Calculate and write the combined Address and Command value to write into the **Serial EEPROM Control** register, by combining the serial EEPROM 3-bit Write Data instruction (value 010b) as bits [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into **Serial EEPROM Control** register bits [12:0], and serial EEPROM Address bit 15 must be programmed into **Serial EEPROM Status** register bit 20 (*that is*, Set bit 20 if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM). The data in the **Serial EEPROM Buffer** register is written to the serial EEPROM when the **Serial EEPROM Status and Control** register is written.
5. The serial EEPROM Write operation is complete when a subsequent read of the **Serial EEPROM Status** register bit 18 returns a value of 0. At this time, another serial EEPROM access can be started.

Because each PEX 8605 Port and Register address value (REGADDR; refer to Section 6.5), and its corresponding data value (REGDATA), require 6 bytes of serial EEPROM memory, and the PEX 8605 serial EEPROM interface accesses 4 bytes at a time, two serial EEPROM Writes may be needed to store each set of REGADDR (one Word) and REGDATA (1 Dword) entries into the serial EEPROM. To avoid overwriting a Word of another set of 6-byte REGADDR and REGDATA values, one of the two Serial EEPROM Writes might need to be a Read-Modify-Write type of operation (preserving one Word read from the serial EEPROM and writing the value back along with a new Word value).

6.8.2 Reading from Serial EEPROM

To read a DWord from the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (Port 0, offset 260h[23:22]) are both Set), write the value to the **Serial EEPROM 3rd Address Byte** register *Serial EEPROM 3rd Address Byte* field (Port 0, offset 26Ch[7:0]).
2. Calculate the combined Address and Command value to write into the **Serial EEPROM Control** register (Port 0, offset 260h), by combining the serial EEPROM 3-bit Read Data instruction (value 011b) as bits [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into **Serial EEPROM Control** register bits [12:0], and serial EEPROM Address bit 15 must be programmed into **Serial EEPROM Status** register bit 20 (*that is*, Set bit 20 if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM).
3. Poll the **Serial EEPROM Status** register until the *EepCmdStatus* bit (Port 0, offset 260h[18]) is Cleared, which signals that the transaction is complete.
4. Read the four bytes of serial EEPROM data from the **Serial EEPROM Buffer** register (Port 0, offset 264h).

   For example, to read the first DWord in the serial EEPROM, write the value 0000_6000h to Port 0, register offset 260h, and then read Port 0, register offset 264h.

6.8.3 Programming a Blank Serial EEPROM

The PEX 8605 supports 1-, 2-, or 3-byte serial EEPROM addressing. 8-Kbit to 512-Kbit SPI EEPROMs use 2-byte addressing. The PEX 8605 requires that the first byte in the serial EEPROM must be the value 5Ah (ASCII Z), as a Validation Signature.

The 2nd and 3rd bytes contain the quantity of bytes within the serial EEPROM image, beginning with the first register entry at serial EEPROM address 04h. If this Byte Count value exceeds the actual quantity of register entries times 6 (*such as*, if the first DWord is programmed to the value 5A00_FFFFh), the system could hang. To simplify programming of a blank EEPROM (*such as* in a typical production build), the serial EEPROM could be pre-programmed with the first DWord, program to 0000_005Ah.

A 2-byte address serial EEPROM that is blank (or corrupted) can be programmed according to the following procedure (when the PEX 8605 is in 1-Byte Address mode).

To program a blank serial EEPROM:

1. Write the value 0000_005Ah into the **Serial EEPROM Buffer** register at address [Port 0 **BAR0** + 264h]. (Register offset 264h is also located in Port 0.)
2. Issue a Write Enable instruction (Command = 110b, Set Write Enable Latch, and enable 2-byte addressing, by writing the value 00A0_C000h into the **Serial EEPROM Status and Control** register (Port 0, offset 260h).
3. Copy this data value to serial EEPROM location 0, by writing the value 00A0_4000h into the **Serial EEPROM Status and Control** register. At this point, the first four bytes in the serial EEPROM now contain the value 0000_005Ah.
4. Reboot the system, to reset the PEX 8605 so that it re-detects the serial EEPROM.

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Chapter 7 I²C/SMBus Slave Interface Operation

7.1 Introduction

This chapter discusses the I2C Slave Interface and SMBus Slave Interface.

7.2 I²C Slave Interface

7.2.1 I²C Support Overview

Note: *This section applies to the I²C Slave interface, which uses the I2C_ADDR[2:0], I2C_SCL, and I2C_SDA signals for PEX 8605 register access by an I²C Master.*

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at relatively low rates (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the *I2C Bus, v2.1*.

The PEX 8605 is an I²C Slave. Slave operations allow the PEX 8605 Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

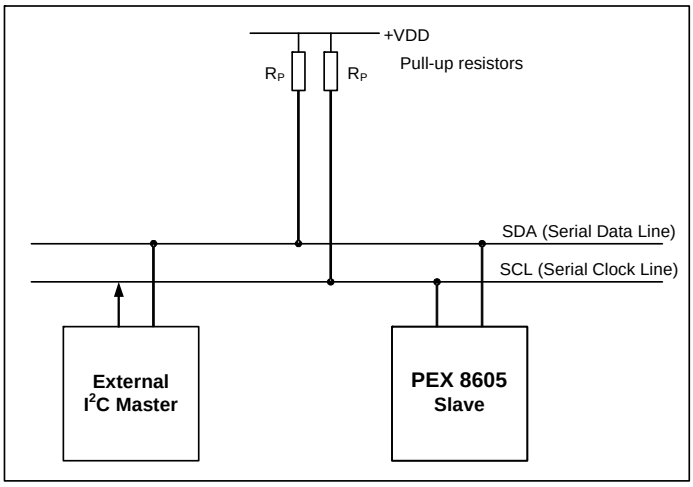
With I²C, users have the option of accessing all PEX 8605 registers through the I²C Slave interface. I²C provides an alternative to using a serial EEPROM. I²C can also be used for debugging, such as if Port 0 fails to linkup.

Accordingly, it is recommended that both I²C/SMBus access, and the serial EEPROM (or at least its footprint), be included in designs.

The I2C_SCL and I2C_SDA signals can be brought out to a 2x2 pin header on the board, to allow PLX software (*for example*, running on a laptop computer) to access the PEX 8605 registers, using an Aardvark USB-I²C adapter connected to this header. (Refer to the *PEX 8605 RDK Hardware Reference Manual* for the header pin design.)

Figure 7-1 provides a block diagram that illustrates how standard devices connect to the I²C Bus.

Figure 7-1. Standard Devices to I2C Bus Connection Block Diagram



7.2.2 I2C Addressing – Slave Mode Access

To access the PEX 8605 Configuration registers through the I2C Slave interface, the PEX 8605 I2C Slave address must be configured.

The PEX 8605 supports a 7-bit I2C Slave address. The 7-bit I2C Address bits can be configured by the serial EEPROM (recommended, if the default address must be changed), or by a Memory Write, in the **I2C Configuration** register (Port 0, offset 294h, default value 5Fh), with the lower three bits of the address derived from the I2C_ADDR[2:0] inputs. Bits [6:0] correspond to Address Byte bits [7:1], with bit 0 of the byte indicating a Write (0) or Read (1).

The I2C_ADDR[2:0] inputs can be pulled or tied High or Low, to select a different Slave address. Up to eight PEX 8605 devices can share the same I2C Bus segment without conflict, provided that each PEX 8605 has its I2C_ADDR[2:0] inputs strapped to a unique state. More than eight PEX 8605 devices can share the I2C Bus, however, if the upper Address bits are programmed in the serial EEPROM. The default state for I2C_ADDR[2:0] inputs that are not externally connected High or Low is 111, due to the internal pull-up resistors.

Note: *If the I2C_ADDR[2:0] inputs must be a value of 000, Address bits [2:0] must be externally driven Low, due to internal pull-up resistors.*

7.2.3 I2C Slave Interface Register

The **I2C Slave Interface** register, **I2C Configuration** (Port 0, offset 294h), is described in Section 11.14.4, "Device-Specific Registers – I2C and SMBus Slave Interfaces (Offsets 290h – 2C4h)." The default I2C Slave address can be changed in the **I2C Configuration** register to a different value, using the serial EEPROM or a Memory Write. **The I2C Slave address must not be changed by an I2C Write command.** (Refer to Section 7.2.2.)

Other I2C Slave interface registers exist; however, they are for ***Factory Test Only***.

7.2.4 I2C Command Format

An I2C transfer starts as a packet with Address Phase bytes, followed by four Command Phase bytes, and one or more Data Phase bytes. The I2C packet Address Phase Byte format is illustrated in Figure 7-2a. The Command Phase portion must include 4 bytes of data that contain the following:

- I2C Transfer type (Read/Write)
- PCI Express Configuration Register address
- PEX 8605 Port Number being accessed
- Byte Enable(s) of the register data being accessed

When the I2C Master is writing to the PEX 8605, the I2C Master must transmit the Data bytes to be written to that register within the same packet that contains the Command bytes. Table 7-2 describes each I2C Command byte for Write access. Figure 7-2b illustrates the Command phase portion of an I2C Write packet.

When the I2C Master is reading from the PEX 8605, the I2C Master must separately transmit a Command Phase packet and Data Phase packet. Table 7-6 describes each I2C Command byte for Read access. Figure 7-4b illustrates the Command phase portion of an I2C Read packet.

Each I2C packet must contain 4 bytes of data. Pad unused packet Data bytes with zeros (0) to meet this requirement.

7.2.5 I2C Register Write Access

The PEX 8605 Configuration registers can be read from and written to, based upon I2C register Read and Write operations, respectively. An I2C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I2C Data bytes. Table 7-1 defines mapping of the I2C Data bytes to the Configuration register Data bytes. Figure 7-2c illustrates the I2C Data byte format.

The I2C packet starts with the *S* (START condition) bit. Data bytes are separated by the *A* (Acknowledge Control Packet (ACK)) or *N* (Negative Acknowledge (NAK)) bit. The packet ends with the *P* (STOP condition) bit.

If the Master generates an invalid command, the targeted PEX 8605 register is not modified.

The PEX 8605 considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I2C Master sends more than the four Data bytes (violating PEX 8605 protocol), the PEX 8605 returns a NAK for the extra Data byte(s). (For further details regarding I2C protocol, refer to the *I2C Bus, v2.1*.)

Table 7-2 describes each I2C Command byte for Write access. In the packet described in Figure 7-2, Command Bytes 0 through 3 for Writes follow the format specified in Table 7-2.

Table 7-1. I2C Register Write Access

I2C Data Byte Order	PCI Express Configuration Register Bytes
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 7-2. I2C Command Format for Write Access

Byte	Bit(s)	Description
1st (0)	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register Do not use other encodings for Writes.
2nd (1)	7:2	***Reserved*** Should be Cleared.
	1:0	**Port Selector, Bits [2:1]** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector.
3rd (2)	7	**Port Selector, Bit 0** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector. *Port Selector[2:0]* select the Port to access. 000b = Port 0 001b = Port 1 010b = Port 2 011b = Port 3 All other encodings are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8605 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8605 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8605 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8605 register bits [31:24]) 0 = Corresponding PEX 8605 register byte will not be modified 1 = Corresponding PEX 8605 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8605 Register Address [11:10]**
4th (3)	7:0	**PEX 8605 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I2C byte Writes.*

Figure 7-2. I2C Write Packet

Figure 7-2a I2C Write Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-2b I2C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

Figure 7-2c I2C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 (to selected register Byte 3)	A	Data Byte 1 (to selected register Byte 2)	A	Data Byte 2 (to selected register Byte 1)	A	Data Byte 3 (to selected register Byte 0)	A	P

7.2.5.1 I2C Register Write Example

The following tables illustrate a sample I2C packet for writing the **MSI Upper Address** register (Port 0, offset 50h), with data 1234_5678h.

Note: *The PEX 8605 has a default I2C Slave address [6:0] value of 5Fh, with the I2C_ADDR[2:0] inputs having a value of 111. The byte sequence on the I2C Bus, as listed in the following tables and figures, occurs after the START and before the STOP bits, by which the I2C Master frames the transfer.*

Table 7-3. I2C Register Write Access Example – 1st Cycle

Phase	Value	Description
Address	70h	**Bits [7:1] for PEX 8605 I2C Slave Address (5Fh)** Last bit (bit 0) for Write = 0.

Table 7-4. I2C Register Write Access Example – Command Cycle

Byte	Value	Description
0	03h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 011b = Write register
1	00h	[7:2] ***Reserved*** Should be Cleared. [1:0] **Port Selector, Bits [2:1]**
2	BCh	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **PEX 8605 Register Address [11:10]**
3	14h	[7:0] **PEX 8605 Register Address [9:2]**

Table 7-5. I2C Register Write Access Example – Write Cycle

Byte	Value	Description
0	12h	**Data to Write for Byte 3**
1	34h	**Data to Write for Byte 2**
2	56h	**Data to Write for Byte 1**
3	78h	**Data to Write for Byte 0**

Figure 7-3. I2C Write Command Packet Example

Figure 7-3a I2C Write Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 1011_111b	Read/Write Bit 0 0 = Write	A

Figure 7-3b I2C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0 0000_0011b	A	Command Byte 1 0000_0000b	A	Command Byte 2 1011_1100b	A	Command Byte 3 0001_0100b	A

Figure 7-3c I2C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 0001_0010b	A	Data Byte 1 0011_0100b	A	Data Byte 2 0101_0110b	A	Data Byte 3 0111_1000b	A	P

7.2.6 I2C Register Read Access

When the I2C Master attempts to read a PEX 8605 register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the *I2C Bus, v2.1*, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I2C Read access occurs, the internal buffer value is transferred on to the I2C Bus, starting from Byte 3 (bits [31:24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I2C Master requests more than four bytes, the PEX 8605 re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I2C Read packets (illustrated in Figure 7-4 and Figure 7-5, respectively) perform the following functions:

- **1st packet** – Selects the register to read
- **2nd packet** – Reads the register (sample 2nd packet provided is for a 7-bit PEX 8605 I2C Slave address)

Although two packets are shown for the I2C Read, the I2C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 7-6 describes each I2C Command byte for Read access. In the packet described in Figure 7-4, Command Bytes 0 through 3 for Reads follow the format specified in Table 7-6.

Table 7-6. I2C Command Format for Read Access

Byte	Bit(s)	Description
1st (0)	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 100b = Read register Do not use other encodings for Reads.
2nd (1)	7:2	***Reserved*** Should be Cleared.
	1:0	**Port Selector, Bits [2:1]** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector.
3rd (2)	7	**Port Selector, Bit 0** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector. *Port Selector[2:0]* select the Port to access. 000b = Port 0 001b = Port 1 010b = Port 2 011b = Port 3 All other encodings are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8605 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8605 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8605 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8605 register bits [31:24]) 0 = Corresponding PEX 8605 register byte will not be modified 1 = Corresponding PEX 8605 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8605 Register Address [11:10]**
4th (3)	7:0	**PEX 8605 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I2C byte Writes.*

Figure 7-4. I2C Read Command Packet (1st Packet)

Figure 7-4a I2C Read Command Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-4b I2C Read Command Packet Command Phase Bytes

Command Cycle								
7 6 5 4 3 2 1 0	ACK/ NAK	7 6 5 4 3 2 1 0	ACK/ NAK	7 6 5 4 3 2 1 0	ACK/ NAK	7 6 5 4 3 2 1 0	ACK/ NAK	STOP
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A	P

Figure 7-5. I2C Read Data Packet (2nd Packet)

Figure 7-5a I2C Read Data Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit, 1 = Read	A

Figure 7-5b I2C Read Data Packet Data Phase Bytes

Read Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

7.2.6.1 I2C Register Read Address Example – Phase and Command Packet

The following is a sample I2C packet for reading the **Serial EEPROM Buffer** register (Port 0, offset 264h), assuming the register value is ABCD_EF01h.

Note: *The PEX 8605 has a default I2C Slave address [6:0] value of 5Fh, with the I2C_ADDR[2:0] inputs having a value of 111. The byte sequence on the I2C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I2C Master frames the transfer.*

Table 7-7. I2C Register Read Access Example – 1st Packet

Phase	Value	Description
Address	70h	**Bits [7:1] for PEX 8605 I2C Slave Address (5Fh)** Last bit (bit 0) for Write = 0.

Table 7-8. I2C Register Read Access Example – Command Cycle

Byte	Value	Description
0	04h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 100b = Read register
1	00h	[7:2] ***Reserved*** Should be Cleared. [1:0] **Port Selector, Bits [2:1]**
2	BCh	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **PEX 8605 Register Address [11:10]**
3	99h	[7:0] **PEX 8605 Register Address [9:2]**

7.2.6.2 I2C Register Read Example – Data Packet

Note: *The PEX 8605 has a default I2C Slave address [6:0] value of 5Fh, with the I2C_ADDR[2:0] inputs having a value of 111. The byte sequence on the I2C Bus, as listed in the following tables and figures, occurs after the START and before the STOP bits, by which the I2C Master frames the transfer.*

Table 7-9. I2C Register Read Access Example – 2nd Packet

Phase	Value	Description
Address	71h	**Bits [7:1] for PEX 8605 I2C Slave Address (5Fh)** Last bit (bit 0) for Read = 1.
Read	ABh	**Byte 3 of Register Read**
	CDh	**Byte 2 of Register Read**
	EFh	**Byte 1 of Register Read**
	01h	**Byte 0 of Register Read**

Figure 7-6. 1st Packet – Command Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 1011_111b	Read/Write Bit 0 = Write	A

Command Cycle								
7 6 5 4 3 2 1 0	ACK/ NAK	7 6 5 4 3 2 1 0	ACK/ NAK	7 6 5 4 3 2 1 0	ACK/ NAK	7 6 5 4 3 2 1 0	ACK/ NAK	STOP
Command Byte 0 0000_0100b	A	Command Byte 1 0000_0000b	A	Command Byte 2 1011_1100b	A	Command Byte 3 1001_1001b	A	P

Figure 7-7. 2nd Packet – Read Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1] 1011_111b	Read/Write Bit 1 = Read	A

Read Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Register Byte 3 1010_1011b	A	Register Byte 2 1100_1101b	A	Register Byte 1 1110_1111b	A	Register Byte 0 0000_0001b	P

7.3 SMBus Slave Interface

7.3.1 SMBus Features

- Compliant to the *SMBus v2.0*
- Supports the SMBus Slave function only
- PEX 8605 internal registers can be read and written, through the SMBus Slave interface
- Supports Address Resolution Protocol (ARP-capable)
- I2C_ADDR[2:0] inputs, serial EEPROM, software, or ARP Set the SMBus Device address
- Supports Block Read, Block Write, and Block Write - Block Read Process Call commands to access the registers
- Supports Packet Error Checking
- 10 to 100 KHz Bus operation frequency range

7.3.2 SMBus Operation

Based upon I^2C's principles of operation, SMBus is a two-wire bus used for communication between IC components and the remainder of the system. Electrically, I^2C and SMBus devices are compatible, and both protocol devices can co-exist on the same bus. Multiple devices, both Masters and Slaves, can be connected to an SMBus segment. PCI Express cards have two optional SMBus pins defined on the connector – SMCLK and SMDAT.

The PEX 8605 implements an *SMBus v2.0*-compliant Slave device, and is used to read and write PEX 8605 registers, through SMBus commands. The PEX 8605 SMBus uses the same SDA data and SCL clock pins that are used for I^2C, and the I2C_ADDR[1:0] inputs, to define Device address assignment (I2C_ADDR2 is not used as an Address bit in SMBus mode). The SMBus Device Address is the same value as the I^2C Slave address, used by the I^2C protocol.

At any time, either the I^2C or the SMBus feature is enabled, dependent upon the **SMBus Configuration** register *SMBus Enable* bit (Port 0, offset 2ACh[0]) state, which is latched (at Fundamental Reset) to the inverse value of the STRAP_SMBUS_EN# input. Software can toggle this bit to switch between I^2C and SMBus functionality.

The PEX 8605 SMBus Slave interface supports three command protocols for register access:

- Block Write
- Block Read
- Block Write - Block Read Process Call

The PEX 8605 SMBus logic also supports the commands that are required to support ARP. ARP is a feature specific to *SMBus v2.0*, through which an SMBus ARP Master can dynamically assign a unique address to each of the SMBus Targets residing on the same bus. Although ARP is an optional feature of the *SMBus v2.0*, PCI and PCI Express cards are required to support ARP. The ARP feature is enabled when the **SMBus Configuration** register *ARP Disable* bit (Port 0, offset 2ACh[8]) is Cleared; this bit is initially latched (at Fundamental Reset) to the value of the I2C_ADDR2 input.

If ARP is disabled, by I2C_ADDR2 input being pulled High, the SMBus Slave Address bits [6:2] default to value 001_10b. Address bits [1:0] are initially latched (at Fundamental Reset) to the value of the I2C_ADDR[1:0] inputs, which allows a maximum of four SMBus-enabled PEX 8605 to co-exist on the same SMBus segment. Software can change the SMBus Slave address, by programming the **SMBus Configuration** register *SMBus Device Address* field (Port 0, offset 2ACh[7:1]).

The PEX 8605 also supports Packet Error Checking and Packet Error Code (PEC) generation, as explained in the *SMBus v2.0*. The *SMBus v2.0* optional feature, *Notify ARP Master* (which requires Master capability on the SMBus) is ***not*** supported.

7.3.3 SMBus Commands Supported

For register access, the SMBus logic supports three commands:

- Block Write (command BEh) is used to write the registers
- Block Write (command BAh), followed by Block Read (command BDh), can be used to read the registers
- Block Write - Block Read Process Call (commands BAh, CDh) can also be used to read registers

SMBus Commands that are not supported by the PEX 8605 (Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read Word, and Process Call), are NACKed.

7.3.3.1 SMBus Block Write

The Block Write command is used to write to the PEX 8605 registers. General SMBus Block Writes are illustrated in Figure 7-8 and Figure 7-9. The sequence of Bytes include the following, in the sequence listed:

- 7-bit address,
- Command Code that indicates it is Block Write,
- *Byte Count* field with a value of 8h that indicates 4 bytes to set up the register to write (Port Number, register address, Command Byte Enable, and so forth), followed by
- 4 bytes of data to be written into the register

Figure 7-10 explains the elements used in Figure 7-8 and Figure 7-9, and Figure 7-11 indicates the Data Bytes written.

Figure 7-8. SMBus Block Write Command Format, to Write to a PEX 8605 Register without PEC

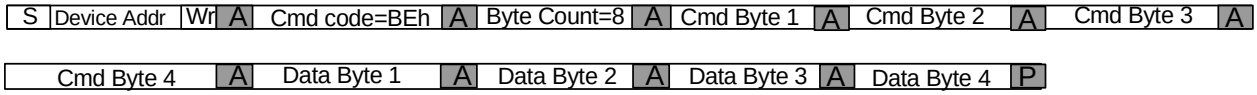


Figure 7-9. SMBus Block Write Command Format, to Write to a PEX 8605 Register with PEC

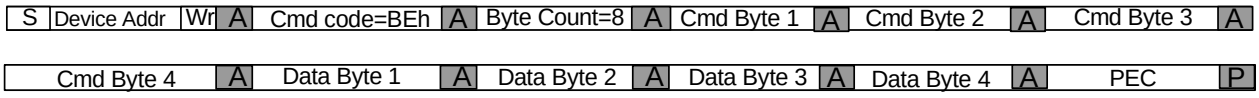


Figure 7-10. SMBus Packet Protocol Diagram Element Key

S -> START condition
P -> STOP condition

A -> Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)

-> Master to Slave
-> Slave to Master

Figure 7-11. SMBus Block Write Bytes, as Written to Register

31:24	23:16	15:8	7:0
Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4

Note: *In each byte, the Most Significant Byte (MSB) is transmitted first.*

Table 7-10 provides a description of bytes for an SMBus Block Configuration Space register (CSR) Write.

Block Write transactions that are received with incorrect byte Settings are NACKed, starting from the wrong byte Setting, and including subsequent bytes in the packet. *For example*, if the Byte Count value is not 8, the PEX 8605 NACKs the byte corresponding to the Byte Count value, as well as any Data bytes following within the same packet.

The byte after Data Byte 4, if present, is taken as the PEC byte, and if present, the PEC is checked. If a packet fails Packet Error Checking, the PEX 8605 drops the packet (ignores the Write), and returns NACK for the PEC byte, to the SMBus Master. Packet Error Checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Port 0, offset 2ACh[9]). The Byte Count value, by definition, does not include the PEC byte.

Table 7-10. Bytes for Block CSR Write on SMBus

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BEh for **B**lock Writ**E**.
Byte Count	7:0	08h = 8 bytes to follow (4 Command and 4 Data bytes). The PEC byte is not counted.
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register 100b = Read register All other encodings are ***reserved***. ***Do not use.***
Command Byte 2	7:2	***Reserved*** Should be Cleared.
	1:0	**Port Selector, Bits [2:1]** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector.
Command Byte 3	7	**Port Selector, Bit 0** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector. *Port Selector[2:0]* select the Port to access. 000b = Port 0 001b = Port 1 010b = Port 2 011b = Port 3 All other encodings are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8605 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8605 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8605 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8605 register bits [31:24]) 0 = Corresponding PEX 8605 register byte will not be modified 1 = Corresponding PEX 8605 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8605 Register Address [11:10]**
Command Byte 4	7:0	**PEX 8605 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I2C byte Writes.*

Sample Register Write Byte Sequence Using SMBus Block Write

An SMBus Block Write packet to write to the **MSI Upper Address** [63:32] register (Port 2, offset 50h), is listed in Table 7-11. The register value is 1234_5678h, with all Bytes enabled, and without PEC. The default SMBus Device Address is 0111_000b.

Table 7-11. SMBus Sample Block Write Byte Sequence

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] for the PEX 8605 default address is 38h, with bit 0 Cleared to indicate a Write.
2	Command Code	BEh	Command Code for register Write, using a Block Write.
3	Byte Count	08h	Byte Count. Four Command Bytes and Four Data Bytes.
4	Command Byte 1	03h	For Write command.
5	Command Byte 2	01h	Bits [7:2] are ***reserved***. Bits [1:0] – Port Selector [2:1].
6	Command Byte 3	3Ch	Bit 7 is Port Selector, bit 0. *Port Selector [2:0]*=010b for Port 2. Bit 6 is ***reserved***. Bits [5:2] are the four Byte Enables; all are active. Bits [1:0] are register Address bits [11:10].
7	Command Byte 4	14h	PEX 8605 Register Address bits [9:2] (for offset 50h).
8	Data Byte 1	12h	Data MSB.
9	Data Byte 2	34h	Data Byte for register bits [23:16].
10	Data Byte 3	56h	Data Byte for register bits [15:8].
11	Data Byte 4	78h	Data LSB.

7.3.3.2 SMBus Block Read

A Block Read command is used to read PEX 8605 registers. Similar to register Reads using I2C, an SMBus Write sequence must first be performed to select the register to read, followed by an SMBus Read of the corresponding register. There are two ways a PEX 8605 register can be read:

- Use a Block Write, followed by a Block Read. The Block Write sets up the parameters including Port Number, register address and Byte Enables, and the Block Read performs the actual Read operation.
- Use a Block Write - Block Read Process Call. This command is defined by the *SMBus v2.0*, and performs a Block Write and Block Read, using a single command. The Block Write portion of the Message sets up the register to be read, and then a repeated START followed by the Block Read portion of the Message returns the register data specified by the Block Write.

Note: *There is no STOP condition before the repeated START condition.*

CSR Read, Using SMBus Block Write, Followed by Block Read

A general SMBus Block Write and Block Read sequence is illustrated in Figure 7-12.

Table 7-12 describes the Byte definitions for a Block Write bus protocol, to prepare for a subsequent Block Read of the PEX 8605 register.

The PEX 8605 always NACKs any incorrect command sequences, starting with the wrong Byte. Upon receiving the Block Read command, the PEX 8605 returns a PEC to the Master if, after the 4th byte of register data, the Master still requests one more Byte. As a Slave, the PEX 8605 recognizes the end of the Master's Read cycle, by observing the Master's NACK response for the last Data Byte transmitted by the PEX 8605.

Incorrect command sequences are always NACKed, starting with the byte that is incorrect. (Refer to Table 7-13.) On the Block Read command, a PEC is returned to the Master, if after the 4th byte of CSR data, the return Master still requests for one additional byte. As a Slave, the PEX 8605 will know the end of the Master Read cycle, by observing the NACK for the last byte read from the Master.

Figure 7-12. SMBus Block Write to Set up Read, and Resulting Read that Returns CSR Value

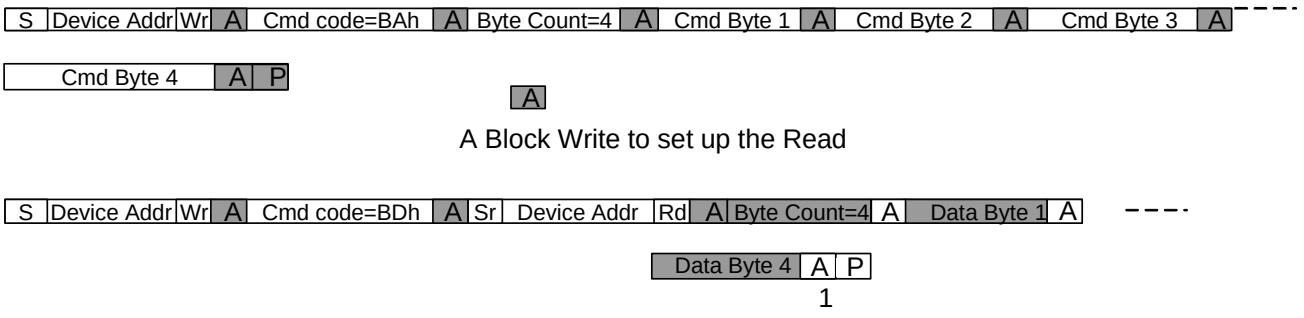


Table 7-12. SMBus Block Read Bytes

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BAh, to set up the Read, using Block Writes.
Byte Count	7:0	04h = 4 Command bytes.
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register 100b = Read register All other encodings are ***reserved***. ***Do not use.***
Command Byte 2	7:2	***Reserved*** Should be Cleared.
	1:0	**Port Selector, Bits [2:1]** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector.
Command Byte 3	7	**Port Selector, Bit 0** 2nd Command byte, bits [1:0], and 3rd Command byte, bit 7, combine to form a 3-bit Port Selector. *Port Selector[2:0]* select the Port to access. 000b = Port 0 001b = Port 1 010b = Port 2 011b = Port 3 All other encodings are ***reserved***.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8605 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8605 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8605 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8605 register bits [31:24]) 0 = Corresponding PEX 8605 register byte will not be modified 1 = Corresponding PEX 8605 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8605 Register Address [11:10]**
Command Byte 4	7:0	**PEX 8605 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I2C byte Writes.*

Table 7-13. Command Format for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/Description
Cmd Code	7:0	CDh, for Block Read (Process **C**all Rea**D**).

Sample CSR Read Byte Sequence, Using SMBus Block Write Followed by Block Read

An SMBus sequence to write and read the **MSI Upper Address** [63:32] register (Port 2, offset 50h), is listed in Table 7-14 and Table 7-15, respectively. The register value is ABCD_EF01h, and without PEC. The Block Write sets up the Port Numbers, Register address and Byte Enables, and the Block Read performs the real Read operation. The default SMBus Device Address is 0111_000b.

Table 7-14. SMBus Block Write Portion

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] value for the PEX 8605 Slave address is 38h, with bit 0 Cleared to indicate a Write.
2	Block Write Command Code	BAh	Command Code for register Read setup, using a Block Write.
3	Byte Count	04h	Byte Count. Four Command Bytes.
4	Command Byte 1	04h	Write command.
5	Command Byte 2	01h	Bits [7:2] are ***reserved***. Bits [1:0] – Port Selector [2:1].
6	Command Byte 3	3Ch	Bit 7 is Port Selector, bit 0. *Port Selector [2:0]*=010b for Port 2. Bit 6 is ***reserved***. Bits [5:2] are the four Byte Enables; all are active. Bits [1:0] are register Address bits [11:10].
7	Command Byte 4	9Dh	PEX 8605 Register Address bits [9:2] (for offset 50h).

Table 7-15. SMBus Block Read Portion

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] value for the PEX 8605 Slave address is 38h, with bit 0 Cleared to indicate a Write.
2	Block Read Command Code	BDh	Command code for Block Read of PEX 8605 registers.

Table 7-16. SMBus Read Command following Repeat START from Master

Byte Number	Byte Type	Value	Description
1	Address	71h	Bits [7:1] value for the PEX 8605 Slave address is 38h, with bit 0 Set to indicate a Read.

Table 7-17. PEX 8605 SMBus Return Bytes

Byte Number	Byte Type	Value	Description
1	Byte Count	04h	Four bytes in register.
2	Data Byte 1	ABh	Register data MSB.
3	Data Byte 2	CDh	Register data [23:16].
4	Data Byte 3	EFh	Register data [15:8].
5	Data Byte 4	01h	Register data LSB.

7.3.3.3 CSR Read, Using SMBus Block Write - Block Read Process Call

A general SMBus Block Write - Block Read Process Call sequence is illustrated in Figure 7-13. Alternatively, a general SMBus Block Write - Block Read Process Call with PEC sequence is illustrated in Figure 7-14.

Using this command, the register to be read can be set up and read back with one SMBus cycle (a transaction with a START and ending in STOP). There is no STOP condition before the repeated START condition. The command format for the Block Write part of this command has the same sequence as in Table 7-14, except that the Command Code changes to CDh, as illustrated below. Other Bytes remain the same as used in the sequence for SMBus Block Write followed by Block Read.

Table 7-13 lists the Command format for Block Read.

Figure 7-13. SMBus CSR Read Operation Using Block Write - Block Read Process Call

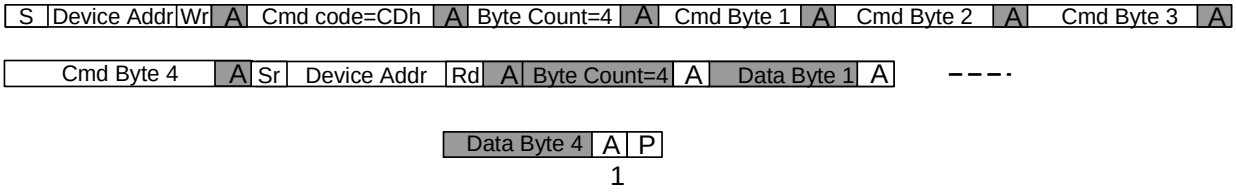
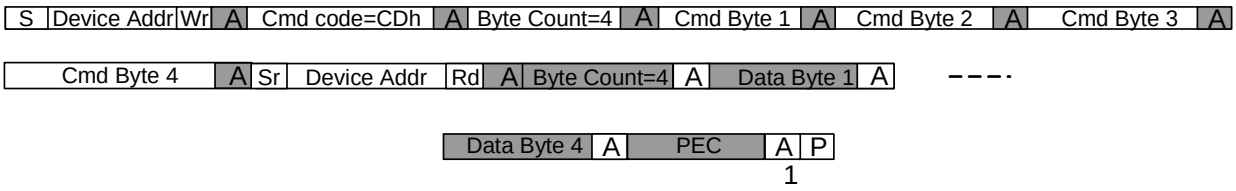


Figure 7-14. SMBus CSR Read Operation Using Block Write - Block Read Process Call with PEC



7.3.4 SMBus Address Resolution Protocol

Address Resolution Protocol (ARP) is a protocol by which SMBus devices that implement an assignable SMBus Device address feature are enumerated and dynamically assigned non-conflicting Slave addresses, rather than using a fixed Slave address. Although optional in the *SMBus v2.0*, it is mandatory per the *PCI r3.0* for add-in boards, to support ARP. This feature avoids conflicts with addresses used by other devices on a motherboard. ARP also allows multiple devices of the same type to co-exist on the same bus segment, without address conflicts.

To support this feature, a Slave device must implement a unique 128-bit ID, called *Unique Device Identifier (UDID)*. The fields of this ID are provided in Figure 7-15. All ARP commands use the default Device Address, 1100_001b. There are also two flags that the SMBus devices must implement to support the ARP process:

- **Address Resolved flag (AR)** – A flag bit or device internal state that indicates whether the ARP Master has resolved the device's SMBus Device address
- **Address Valid flag (AV)** – A flag bit or device internal state that indicates whether the device's SMBus Device address is valid

The process of assigning a SMBus Device address starts with the ARP Master issuing a Reset Device or Prepare to ARP command, using the default Device address. This Clears the *AR* flag in the Slave device (both flags are Cleared by a Reset Device command). The Master then issues a general Get UDID command. This causes all devices that support ARP to start driving their UDID onto the serial bus. A Target that loses the SMBus arbitration, backs off. Arbitration loss means that a device keeps the SMDAT line floating and it detects 0 driven by another device on the bus. Slave devices that lose arbitration issue NACK in response to further Bytes transmitted on the bus. After the ARP Master finishes the Get UDID sequence, it issues a Set Address command to the Slave device, using the Slave's UDID. All Slave devices on the bus monitor the UDID that is transmitted by the ARP Master, but only the particular device that has the matching UDID adopts the new SMBus Device address, and Sets its own *AV* and *AR* flags. After the Slave device Sets its *AR* flag, that device no longer responds to a general Get UDID command, which allows other devices to participate in the ARP process. All ARP commands require PEC checking and generation.

7.3.4.1 SMBus UDID

The 128-bit UDID is comprised of the following fields, as illustrated in Figure 7-15 (not to scale). Each UDID field and its default value implemented in the PEX 8605 and meaning are explained in the tables that follow.

Figure 7-15. 128-Bit SMBus UDID

8 bits	8 bits	16 bits	16 bits	16 bits	16 bits	16 bits	32 bits
127:120	119:112	111:96	95:80	79:64	63:48	47:32	31:0
Device Capability	Version/ Revision	Vendor ID	Device ID	Interface	Subsystem Vendor ID	Subsystem Device ID	Vendor-Specific ID

Table 7-18. SMBus Vendor-Specific ID [31:0]

Field	Name	Default Value	Description
31:0	Vendor-Specific ID	Depends upon I2C_ADDR[2:0] input states. The four combinations provide the following ID values: 00b = 7000_0000h 01b = B000_0000h 10b = D000_0000h 11b = E000_0000h	The Vendor-Specific ID is used to provide a unique ID for functionally equivalent devices. This is for devices that would otherwise return identical UDIDs for the purpose of dynamic address assignment. The combination of two Address bits produces four unique Vendor-Specific ID values, for a maximum of four SMBus-enabled PEX 8605s to co-exist on the same SMBus segment.

Table 7-19. SMBus Subsystem Device ID [47:32]

Field	Name	Default Value	Description
15:0	Subsystem Device ID	8605h	PLX part number for the PEX 8605.

Table 7-20. SMBus Subsystem Vendor ID [63:48]

Field	Name	Default Value	Description
15:0	Subsystem Vendor ID	10B5h	PLX Vendor ID.

Table 7-21. SMBus Interface [79:64]

Field	Name	Default Value	Description
3:0	SMBus Version	0100b	*SMBus v2.0*.
15:4	***Reserved***	0-0h	Supported protocols.

Table 7-22. SMBus Device ID [95:80]

Field	Name	Default Value	Description
15:0	Device ID	8605h	PEX 8605 default Device ID value.

Table 7-23. SMBus Vendor ID [111:96]

Field	Name	Default Value	Description
15:0	Vendor ID	10B5h	PLX Vendor ID.

Table 7-24. SMBus Version/Revision [119:112]

Field	Name	Default Value	Description
2:0	Silicon Revision ID	010b	PEX 8605, Silicon Revisions AA and AB.
5:3	UDID Version	001b	UDID version defined for *SMBus v2.0*.
7:6	***Reserved***	00b	

Table 7-25. SMBus Device Capability [127:120]

Field	Name	Default Value	Description
0	PEC Supported	1	By default, PEC generation and checking are enabled.
5:1	***Reserved***	00_000b	
7:6	Address Type	10b	The PEX 8605 SMBus Address Type is implemented as dynamic and volatile. 00b = Fixed address 01b = Dynamic and persistent 10b = Dynamic and volatile (default) 11b = Random number device

7.3.4.2 Supported SMBus ARP Commands

The PEX 8605 supports all ARP Slave commands. The Notify ARP Master command, which requires Master functionality, is ***not*** supported. Table 7-26 explains the PEX 8605 response to each received ARP command.

Table 7-26. SMBus ARP Commands Supported, Format, and Actions

ARP Command	SMBus Command Format	SMBus Device Address	Command Code	Action
Prepare to ARP (Only General)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	01h	Clear the *AR Flag* and prepare for the ARP process. *AV Flag* will have no change.
Reset Device (General)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	02h	Clear the *AR Flag* and *AV Flag*.
Reset Device (Directed)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 0	If the *AV Flag* is Set, Set ACK and Clear the *AR Flag* and *AV Flag*; else, NACK/REJECT.
Get UDID (General)	Block Read (Refer to Figure 7-17)	SMBus default Device Address 1100_001b	03h	Respond only if the *AR Flag* is Cleared; else, NACK/REJECT. *AR Flag* and *AV Flag* are not changed. Address returned is all ones (1), if the *AV Flag* is Cleared.
Get UDID (Directed)	Block Read	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 1	*AR Flag* and *AV Flag* are not changed. ACK if *AV Flag*=1; else, NACK/REJECT. Data Byte 17 returned will be the SMBus Device address.
Assign Address ARP	Block Write (Refer to Figure 7-18)	SMBus default Device Address 1100_001b	04h	Always ACK and Set the *AR Flag* and *AV Flag*, if the UDID matches.

Figure 7-16. Prepare SMBus ARP Command and Reset Device Command Format

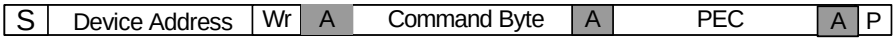
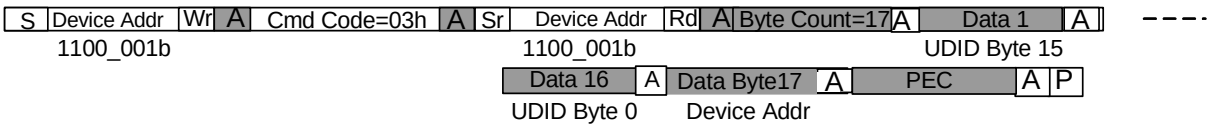
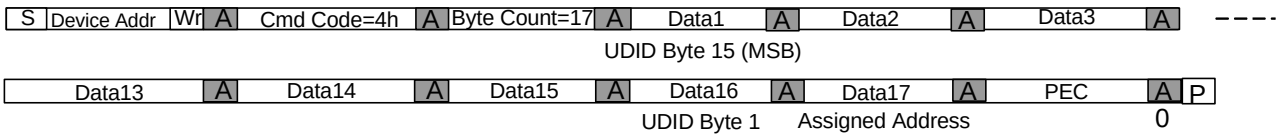


Figure 7-17. Get SMBus UDID Command Format (General Get UDID Command with PEC)



Note: *If the **SMBus Configuration** register AR Flag bit (Port 0, offset 2ACh[11]) is Cleared, the device returns the register's SMBus Device Address field (Port 0, offset 2ACh[7:1]) as 1111_111b; otherwise, it returns the device SMBus Device address. Bit 0 (LSB) in the Data Byte 17 field should be 1.*

Figure 7-18. Assign SMBus Address ARP Command Format



Note: *Bit 0 (LSB) of the Data 17 field is ignored in the Assign Address command field.*

7.3.5 SMBus PEC Handling

The PEX 8605 supports the optional *SMBus v2.0* PEC generation and checking feature. This feature is required for the ARP process; however, it is optional for standard data transfer operation. The PEX 8605 supports PEC Cyclic Redundancy Check (CRC) generation and checking during ARP, as well as during Read/Write transfers to PEX 8605 registers. The CRC polynomial used for PEC calculation is:

$$C(x) = x^8 + x^2 + x + 1$$

An 8-bit parallel CRC is implemented. The PEC calculation does not include ACK, NACK, START, STOP, nor repeated START bits. An SMBus Master can determine whether a Slave device supports PEC, from the value of the UDID returned by the Slave device in response to a Get UDID command.

As a Slave device, the PEX 8605 checks PEC, if the Master transmits the additional PEC byte and the PEX 8605 PEC checking feature is enabled (default). PEC checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Port 0, offset 2ACh[9]).

Additionally, when PEC is enabled, packets received with an incorrect PEC value are dropped. If PEC checking is disabled and a received PEC byte value is incorrect, the PEX 8605 accepts the packet. During a register Read, if the Master requests the additional PEC byte, the PEX 8605 generates and transmits the PEC byte after the register data.

7.3.6 Addressing PEX 8605 SMBus Slave

By default, the PEX 8605 supports ARP when the I2C_ADDR2 input is tied Low, and expects the ARP Master to define the PEX 8605 SMBus Device address. If ARP is disabled by I2C_ADDR2 input being pulled High, the default address is 38h (Address bits [7:1] are 0111_000b, with Address bit [1:0] values loaded from the I2C_ADDR[1:0] inputs). The two Address bits allow a maximum of four PEX 8605 SMBus Slaves to co-exist without address conflict on the SMBus, using SMBus address byte values of 70h, 72h, 74h, and 78h. The I2C_ADDR[2:0] inputs are loaded immediately after Fundamental Reset, and any subsequent change of input value does not affect functionality.

If the **SMBus Configuration** register *UDID Address Type* field is programmed as Fixed Address (Port 0, offset 2ACh[13:12], is Cleared) without disabling ARP, the PEX 8605 still participates in ARP, but does not Set the Device address after ARP successfully completes.

The SMBus Slave Address can be changed at any time, by using software to write to the register's *SMBus Device Address* field (Port 0, offset 2ACh[7:1]). ARP can also be enabled or disabled at runtime, by writing to the register's *ARP Disable* bit (Port 0, offset 2ACh[8]). If ARP is disabled by software after initially being enabled, the default address (70h) is not used for subsequent transactions. In this case, software must program a Slave address into the *SMBus Device Address* field. When software writes the Device address, it must also Set the register's *AR Flag* and *AV Flag* bits (Port 0, offset 2ACh[11:10], respectively), to indicate that the address is valid and resolved.

Whenever software changes the register's *AV Flag*, *ARP Disable*, or *SMBus Device Address* values, software must also Set the register's *SMBus Parameter Re-Load* bit (Port 0, offset 2ACh[15]). Writes to this register bit take effect only when the register's *SMBus Command In-Progress* bit (Port 0, offset 2ACh[28]) is Cleared, which indicates that the PEX 8605 SMBus interface is in the Idle state.

7.3.7 SMBus Timeout

Unlike I^2C, where the Slave or Master can indefinitely hold the I2C_SCL line Low, SMBus has a timeout condition. No device is allowed to hold the I2C_SCL line Low for more than 25 ms. When the PEX 8605, as a slave-transmitter, detects that it has pulled the I2C_SCL line Low for more than 25 ms, the PEX 8605 releases I2C_SCL, and the logic returns to its default state and waits for another START condition. This can also occur when the Master pulls the I2C_SCL line Low for more than 25 ms during single clock Low interval within a transfer in progress, or during the ACK phase if the Master pulls the I2C_SCL line Low to process a task. Generally, the PEX 8605 pulls the I2C_SCL line Low if SMBus access to registers is delayed by internal arbitration for register access.

7.3.8 Switching between SMBus and I^2C Bus Protocols

The PEX 8605's I^2C implementation allows switching between the SMBus and I^2C protocols, by toggling the **SMBus Configuration** register *SMBus Enable* bit (Port 0, offset 2ACh[0]).

When operating in SMBus mode, Clearing this bit, using the SMBus Block Write protocol, enables I^2C protocol for subsequent register accesses. This SMBus Block Write can be transmitted from an SMBus or I^2C Master, provided the Block Write Byte sequence conforms to the sequence explained in Section 7.3.3.1. In I^2C mode, writing 1 to the *SMBus Enable* bit turns On the SMBus protocol, immediately after the Write operation is complete.

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Chapter 8 Interrupts

8.1 Interrupt Support

The PEX 8605 supports the PCI Express interrupt model, which uses two mechanisms:

- INT*x* Interrupt Message-type emulation (compatible with the *PCI r3.0*-defined Interrupt signals)
- Message Signaled Interrupt (MSI), when enabled

For Conventional PCI compatibility, the PCI INT*x* emulation mechanism is used to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software, provides the same level of service as the corresponding PCI interrupt signaling mechanism, and is independent of System Interrupt Controller specifics. The PCI INT*x* emulation mechanism virtualizes PCI physical Interrupt signals, by using an in-band signaling mechanism, for the assertion and de-assertion of INT*x* interrupt signals.

In addition to PCI INT*x*-compatible interrupt emulation, the PEX 8605 supports the MSI mechanism. The PCI Express MSI mechanism is compatible with the MSI Capability defined in the *PCI r3.0*.

INT*x* and MSI are mutually exclusive, on a per-Port basis; either can be enabled in a system (depending upon which interrupt type the system software supports, for assertion and de-assertion of interrupt signals), but never concurrently within the same domain. (Refer to the **PCI Command** register *Interrupt Disable* bit (All Ports, offset 04h[10]), and **MSI Control** register *MSI Enable* bit (All Ports, offset 48h[16]), respectively.) The PEX 8605 does not convert received INT*x* Messages to MSI Messages.

The PEX 8605's external Interrupt output, PEX_INTA#, indicates the assertion and/or de-assertion of the internally generated INT*x* signal:

- **Hot Plug and Power Management-triggered INT*x* events** – PEX_INTA# assertion is controlled by the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for Hot Plug Event-Triggered Interrupts* bit (All Ports, offset 1C8h[4]). When this bit is Set, Hot Plug and Power Management events trigger PEX_INTA# assertion; however, an INT*x* Message is not generated in this case.
- **GPIO-triggered interrupts** – PEX_INTA# assertion is controlled by the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* bit (All Ports, offset 1C8h[6]).

PEX_INTA# assertion and INT*x* Message generation are mutually exclusive, on a per-Port basis.

8.1.1 Interrupt Sources or Events

The PEX 8605 internally generated interrupt/Message sources include:

- Power Management events:
  - Link Bandwidth Management Status
  - Link Autonomous Bandwidth Status
- Hot Plug events:
  - Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Data Link Layer State Changed
- General-Purpose Input/Output (GPIO) events (Port 0 only)

The PEX 8605 externally generated interrupt/Message sources include INT*x* Messages from downstream devices.

Table 8-1 lists the interrupt sources.

Table 8-1. Interrupt Sources

Event/Error	Description
Power Management events	**Link Status and Control** register (Downstream Ports, offset 78h): • *Link Bandwidth Management Interrupt Enable* and *Link Bandwidth Management Status* (bits [10 and 30], respectively) are both Set • *Link Autonomous Bandwidth Interrupt Enable* and *Link Autonomous Bandwidth Status* (bits [11 and 31], respectively) are both Set
Hot Plug events	The master control of Hot Plug interrupts is the **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]). The two sources of Hot Plug interrupt are controlled by the **Slot Status and Control** register (Downstream Ports, offset 80h): • *Presence Detect Changed Enable* and *Presence Detect Changed* (bits [3 and 19], respectively) are both Set • *Data Link Layer State Changed Enable* and *Data Link Layer State Changed* (bits [12 and 24], respectively) are both Set ***Note:*** *Presence (Presence Detect State, offset 80h[22], in each downstream Port) is determined by the logical OR of SerDes Receiver Detect (**Physical Layer Receiver Detect Status** register Receiver Detected on Lane x bits (Port 0, offset 200h[19:16])).*
General-Purpose Input Interrupt events	External interrupt from any of the GPIO[3:0] signals that are configured as an Interrupt input in the **GPIO Control** register (Port 0, offset 62Ch).

*a. The SerDes Receiver Detect mechanism is comprised of the **Physical Layer Receiver Detect Status** register Receiver Detected on Lane x bits (Port 0, offset 200h[19:16]).*

8.1.2 Interrupt Handling

The PEX 8605 provides an Interrupt Generation module with each Port. The module reads the Request for interrupts from different sources and generates an MSI or PCI-compatible Assert_INT*x*/ Deassert_INT*x* Interrupt Message. The MSI supports a PCI Express edge-triggered interrupt, whereas Assert_INT*x* and Deassert_INT*x* Message transactions emulate PCI level-triggered interrupt signaling. The System Interrupt Controller functions include:

- Sensing Interrupt events
- Signaling the interrupt, by way of the INT*x* mechanism, and Setting the Interrupt Status bit
- Signaling the interrupt, by way of the MSI mechanism
- Handling INT*x*-type Interrupt Messages from downstream devices

8.2 INT*x* Emulation Support

The PEX 8605 supports PCI INT*x* emulation, to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software. PCI INT*x* emulation virtualizes PCI physical Interrupt signals, by using the in-band signaling mechanism.

PCI **Interrupt** registers (defined in the *PCI r3.0*) are supported. The *PCI r3.0* **PCI Command** register *Interrupt Disable* and **PCI Status** register *Interrupt Status* bits are also supported (All Ports, offset 04h[10 and 19], respectively).

Although the *PCI Express Base r2.1* provides INTA#, INTB#, INTC#, and INTD# for INT*x* signaling, the PEX 8605 uses only INTA# for internal Interrupt Message generation, because it is a single-function device. However, incoming Messages from downstream devices can be of INTA#, INTB#, INTC#, or INTD# type. Internally generated INTA# Messages from the downstream Port are also re-mapped and collapsed at Port 0, according to the downstream Port's Device Number, with its own Device Number and Received Device Number from the downstream device.

When an interrupt is requested, the **PCI Status** register *Interrupt Status* bit is Set. If INT*x* interrupts are enabled (**PCI Command** register *Interrupt Disable* bit (All Ports, offset 04h[10]), and **MSI Control** register *MSI Enable* bit (All Ports, offset 48h[16]), are both Cleared), an Assert_INT*x* Message is generated and transmitted upstream to indicate the Port interrupt status. For each interrupt event, there is a corresponding *Interrupt Mask* bit; an Interrupt Message can be generated only when the corresponding *Interrupt Mask* bit is Cleared. Software reads and Clears the event and *Interrupt Status* bit after servicing the interrupt.

A Port de-asserts INT*x* or PEX_INTA# interrupts in response to one or more of the following conditions:

- Port's **PCI Command** register *Interrupt Disable* bit (All Ports, offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- Port 0 Link goes down (DL_Down condition), or receives a Hot Reset (unless Hot Reset/ DL_Down Reset is disabled, by Setting the **Debug Control** register *Upstream Port DL_Down Reset Propagation Disable* bit (Port 0, offset 1DCh[20]))
- Software Clears the corresponding *Interrupt Status* bit

8.2.1 INT*x*-Type Interrupt Message Re-Mapping and Collapsing

Port 0 re-maps and collapses the INT*x* *virtual wires* received at the downstream Port, based upon the downstream Port's Device Number and Received INT*x* Message Requester ID Device Number, and generates a new Interrupt Message, according to the mapping defined in Table 8-2.

Each virtual PCI-to-PCI bridge of a downstream Port specifies the Port Number associated with the INT*x* (Interrupt) Messages received or generated, and forwards the Interrupt Messages upstream.

A downstream Port transmits an Assert_INTA/Deassert_INTA Message to Port 0, due to a Power Management, Hot Plug, and/or GPIO error/event.

Internally generated INT*x* Messages always originate as type INTA Messages, because the PEX 8605 is a single-function device. Internally generated Interrupt INTA Messages from downstream Ports are re-mapped at Port 0 to INTA, INTB, INTC, or INTD Messages, according to the mapping defined in Table 8-2.

INT*x* Messages from downstream devices and from internally generated Interrupt Messages are ORed together to generate INTA, INTB, INTC, or INTD level-sensitive signals, and edge-detection circuitry in Port 0 generates the Assert_INT*x* and Deassert_INT*x* Messages. Port 0 then forwards the new Messages upstream, by way of its Link.

Table 8-2. Downstream Port/Port 0 INT*x* Interrupt Message Mapping

Device Number	At Downstream Port	By Port 0
0	INTA	INTA
	INTB	INTB
	INTC	INTC
	INTD	INTD
1	INTA	INTB
	INTB	INTC
	INTC	INTD
	INTD	INTA
2	INTA	INTC
	INTB	INTD
	INTC	INTA
	INTD	INTB
3	INTA	INTD
	INTB	INTA
	INTC	INTB
	INTD	INTC

8.3 MSI Support

One of the interrupt schemes supported by the PEX 8605 is the MSI mechanism, which is required for PCI Express devices. The MSI method uses Memory Write transactions to deliver interrupts. MSIs are edge-triggered interrupts.

Note: *MSI and INTx are mutually exclusive, on a per-Port basis. These interrupt mechanisms* ***cannot*** *be simultaneously enabled.*

8.3.1 MSI Operation

At configuration time, system software traverses the function Capability list. If a Capability ID of 05h is found, the function implements MSI. System software reads the **MSI Capability** Structure registers, to determine function capabilities.

The **MSI Control** register *Multiple Message Capable* field (All Ports, offset 48h[19:17]) default value is 010b, which indicates that the PEX 8605 requests up to four MSI Vectors (Address and Data). When the register's *Multiple Message Enable* field (All Ports, offset 48h[22:20]) is Cleared (default), only one MSI Vector is allocated, and therefore, the PEX 8605 can generate only one MSI Vector for all errors or events. When system software writes a non-zero value to the *Multiple Message Enable* field, multiple-Vector support is enabled (the quantity of MSI Vectors supported is dependent upon the value). The PEX 8605 supports the following MSI Vector types:

- Power Management or Hot Plug events
- GPIO-generated interrupts

System software initializes the MSI Address registers (All Ports, offsets 4Ch and 50h) and **MSI Data** register (All Ports, offset 54h) with a system-specified Vector. After system software enables the MSI function (by Setting the **MSI Control** register *MSI Enable* bit (All Ports, offset 48h[16]), when an Interrupt event occurs, the Interrupt Generation module generates a DWord Memory Write to the address specified by the **MSI Address** (lower 32 bits of the *Message Address* field) and **MSI Upper Address** (upper 32 bits of the *Message Address* field) register contents (All Ports, offsets 4Ch and 50h, respectively). The single DWord Payload includes zero (0) for the upper two bytes, and the lower two bytes are taken from the **MSI Data** register. The *Multiple Message Enable* field (All Ports, offset 48h[22:20]) can be programmed to any value of 000b through 111b. When programmed to 010b through 111b, the lower three bits of Message data are changed to indicate the general type of interrupt event that occurred.

The quantity of MSI Vectors generated is dependent upon the quantity enabled, as follows:

- If **one** MSI Vector is enabled (default mode), both interrupt events are combined into a single Vector
- If **two** MSI Vectors are enabled, the individual vectors indicate:
  - Vector[0] Hot Plug/Power Management event and GPIO-generated event
  - Vector[1] ***Reserved***
- If **four** MSI Vectors are enabled (up to two Vectors are used), the individual Vectors indicate:
  - Vector[0] Hot Plug/Power Management event
  - Vector[1] ***Reserved***
  - Vector[2] GPIO-generated event
  - Vector[3] ***Reserved***

If a non-masked Interrupt event occurs before system software Sets the *MSI Enable* bit, normally (but unlike Conventional PCI interrupts, which are level-triggered), an MSI packet is sent immediately after software Sets the *MSI Enable* bit, to notify the system of the prior event.

When the error or event that caused the interrupt is serviced, the PEX 8605 can generate a new MSI Memory Write as a result of new events. Because MSIs are edge-triggered events, the **MSI Mask** register *Interrupt Mask* bits (All Ports, offset 58h[2 and 0]) are provided, to use for masking the events. A new MSI can be generated only after the *Interrupt Mask* bits are serviced. System software should mask these bits when an MSI event is being processed.

The **MSI Control** register *MSI 64-Bit Address Capable* bit is enabled (All Ports, offset 48h[23], is Set), by default. If the serial EEPROM and/or I^2C/SMBus Clears the bit, the **MSI Capability** structure is reduced by 1 DWord (*that is*, register offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively).

8.3.2 MSI Capability Registers

For details, refer to Section 11.8, "MSI Capability Registers (Offsets 48h – 64h)."

8.4 PEX_INTA# Interrupts

PEX_INTA# Interrupt output is enabled when the following conditions exist:

- INT*x* Messages are enabled (**PCI Command** register *Interrupt Disable* bit (All Ports, offset 04h[10]) is Set) and
- MSI is disabled (**MSI Control** register *MSI Enable* bit (All Ports, offset 48h[16]) is Cleared)
- PEX_INTA# outputs are enabled for the following interrupts, when the **ECC Error Check Disable** register (All Ports, offset 1C8h) bit associated with that interrupt is Set:
  - *Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* bit (bit 6)
  - *Enable PEX_INTA# Interrupt Output(s) for Hot Plug Event-Triggered Interrupts* bit (bit 4)

The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources:

- Conventional PCI INT*x* Message generation
- Native MSI transaction generation
- Device-Specific PEX_INTA# assertion

PEX_INTA# assertion (Low) indicates that the PEX 8605 detected one or more of the events and/or errors (if not masked) listed in Table 8-1.

Note: *PEX_INTA# assertion and INTx messaging are mutually exclusive for a given interrupt event. When MSI is enabled (All Ports, offset 48h[16], is Set), both PEX_INTA# and INTx are disabled for PEX 8605 internally generated interrupts. The forwarding of external INTx Messages received from a downstream Port to Port 0 is always enabled.*

8.5 General-Purpose Input/Output

The PEX 8605 contains four General-Purpose Input/Output (GPIO) pins and five associated registers that can be programmed to function as GPIO or Link Status (Lane Good) indicators. Default functionality is LANE_GOOD[3:0]#; however, serial EEPROM, I^2C/SMBus, and/or software can program the GPIO registers to define functionality for each I/O.

GPIO functions are selected when the **Debug Control** register *LANE_GOODx#/GPIOx Pin Function Select* bit (Port 0, offset 1DCh[22]) is Cleared, as described in Table 8-3. Each GPIO*x* pin is then individually programmable through a set of **GPIO Control** registers (Port 0, offsets 62Ch through 63Ch). (Refer to Table 8-4.)

Table 8-3. GPIO Pin Selection

Signal Pin	Offset 1DCh[22]=0	Offset 1DCh[22]=1 (Default)
A19	GPIO0	LANE_GOOD0#
A16	GPIO1	LANE_GOOD1#
B55	GPIO2	LANE_GOOD2#
B16	GPIO3	LANE_GOOD3#

Table 8-4. GPIO Control Registers (Port 0)

Offset	Register
62Ch	**GPIO Control**
630h	**GPIO Interrupt Status**
634h	**GPIO PWM Value**
638h	**GPIO PWM Ramp Control**
63Ch	**GPIO PWM Clock Frequency**

When GPIO*x* is configured as an input, software can read the value presented on the pin. Additionally, the PEX 8605 can generate an interrupt based upon a state change (High to Low **and** Low to High) on the pin. GPIO inputs can also be configured with hardware-based de-bounce circuitry, which helps prevent multiple interrupts for noisy or slow transitions on the pin.

When GPIO*x* is configured as an output, software can program the pin to be High or Low. GPIO outputs also support programmable pulse-width-modulated (PWM) output, where software can program the quantity of Clock cycles that the signal drives High versus Low. This feature is useful for driving LEDs at various brightness levels, by varying the output waveform's duty cycle. Additionally, the PWM duty cycle can be increased or decreased linearly at a programmable rate, which can be used to make LEDs progressively brighter or dimmer at a regular rate.

PWM functions repeat in cycles of 256 steps. The duration (or period) of each step is determined by the **GPIO PWM Clock Frequency** register. The value in this register divides an input clock of 62.5 MHz by a programmed value of 0 to 128 (0 = 128).

The PWM Clock Frequency value is used to divide a 62.5 MHz input clock. Allowable values are from 1 to 256 (00h to FFh, where 00h corresponds to 256). For the highest output frequency, program the register's *PWM Clock Divider* field (field [7:0]) to 01h. This yields a PWM frequency of 245.1 KHz. For the slowest output frequency (default), program the field to 00h, for a PWM frequency of 1.908 KHz. Values of 02h through FFh linearly scale the PWM frequency within this range. The PWM step time is common to all GPIO outputs.

PWM High time is controlled by way of the **GPIO PWM Value** register. Values programmed into this register determine the quantity of steps (out of 256) that the output is driven High. For the remaining steps in the PWM cycle, the output is driven Low.

The PWM value for each GPIO can be incremented or decremented by one step every *n* PWM cycles, where *n* is the value programmed into the **GPIO PWM Ramp Control** register. PWM ramping starts when a value of *n*=1 to 255 is programmed, and ends when the PWM value reaches 255 or 0.

8.5.1 GPIO Control Registers

The **GPIO Control** registers, which includes the PWM registers, are located in Port 0 only. For details, refer to Section 11.16.2, "Device-Specific Registers – General-Purpose Input/Output Control (Offsets 62Ch – 63Ch)."

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Chapter 9 Hot Plug Support

9.1 Introduction

Hot Plug capability allows insertion and extraction of boards from a running system, without adversely affecting that system. The PEX 8605 provides limited support for Hot Plug, providing a single HP_PRSNT# input pin that can be assigned to any one downstream Port.

9.2 Hot Plug Features

The PEX 8605 Hot Plug features are as follows:

- Any one downstream Port can be assigned as Hot Plug-capable
- HP_PRSNT# input detects insertion/removal of a board within a sleeping system
- PME event generation on insertion of board in sleeping system (D1, D2, and D3hot states)
- In-band presence detection in a powered system (D0 state)
- Interrupt generation when the following events occur:
  - Presence Detect Changed (logical OR of HP_PRSNT# pin state and in-band presence detect)
  - Data Link Layer State Changed

9.3 HP_PRSNT# Input Pin

The PEX 8605 provides a single HP_PRSNT# input pin. HP_PRSNT# is typically pulled High, externally. Insertion of an add-in board causes this input to be tied to Ground. The HP_PRSNT# input implements a 10-ms de-bounce circuit.

The HP_PRSNT# input can be assigned to one of the PEX 8605 downstream Ports, by way of the **Power Management Hot Plug User Configuration** register *Present Pin Assignment Register* field (Port 0, offset 1E0h[17:16]). By default, HP_PRSNT# pin is assigned to Port 1 when STRAP_PORTCFG=0 (x1x1x1x1), and to Port 2 when STRAP_PORTCFG=1 (x2x1x1). The optional serial EEPROM can be used to override the defaults, by programming this register field to the desired Port.

The downstream Port that has been designated as the Hot Plug-capable Port is indicated in the Port's **Slot Capability** register *Hot Plug Capable* bit (Downstream Ports, offset 7Ch[6]).

9.4 Interrupt, Power Management Event Generation

The PEX 8605 supports generation of Hot Plug interrupts when the following events occur:

- HP_PRSNT# input state changed, reflected in the **Slot Status** register *Presence Detect Changed* bit (Downstream Ports, offset 80h[19])
- Data Link Layer state changed, reflected in the **Slot Status** register *Data Link Layer State Changed* bit (Downstream Ports, offset 80h[24])

Depending upon the downstream Port's power state, a Hot Plug event can generate either a System interrupt or Power Management event (PME):

- When the Hot Plug-capable downstream Port is in the D0 state, Hot Plug events cause an Interrupt Message to be generated, if enabled
- When in the D1, D2 or D3hot state, a PME (PME Message, WAKE# assertion) can be generated on Hot Plug events

9.4.1 Data Link Layer State Change Reporting

The PEX 8605 supports Data Link Layer State Change Event reporting, on all Downstream ports. This is reported through the **Slot Status** register *Data Link Layer State Changed* bit (Downstream Ports, offset 80h[24]). This bit is Set when the value reported in the **Link Status** register *Data Link Layer Link Active* bit (Downstream Ports, offset 78h[29]) is changed.

9.4.2 Surprise Down Generation

The PEX 8605 supports Surprise DL_Down error reporting, on all downstream Ports. When the Data Link Layer status changes from DL up o DL down, a Surprise Down is reported, if the conditions described in the *PCI Express Base r2.1*, Section 3.2.1, are met.

9.5 Hot Plug Board Insertion and Removal Process

Table 9-1 defines the board insertion procedure supported by the PEX 8605. Table 9-2 defines the board removal procedure.

Table 9-1. Hot Plug Board Insertion Process

Operator / Action	Hot Plug Controller	Software
A. Places board in slot.	**1.** Sets the **Slot Status** register *Presence Detect State* bit (Downstream Ports, offset 80h[22]). **2.** Sets the **Slot Status** register *Presence Detect Changed* bit (Downstream Ports, offset 80h[19]). **3.** Generates Interrupt Message due to Presence Detect Changed event, if enabled.	Clears *Presence Detect Changed* bit.
	4. Transmits an Interrupt de-assertion Message, if enabled.	
	5. After the Data Link Layer is up (after successful Link training and Flow Control (FC) initialization), Sets the **Slot Status** register *Data Link Layer State Changed* bit (Downstream Ports, offset 80h[24]), and transmits the corresponding interrupt, if enabled.	Software can now read the **Link Status** register *Data Link Layer Link Active* bit (Downstream Ports, offset 78h[29]). A value of 1 in this bit indicates that the board is ready to be used. Clears the *Data Link Layer State Changed* bit and interrupt, if enabled.
	6. Transmits an Interrupt de-assertion Message, if enabled.	Add-in board is ready to be enumerated by software.

Table 9-2. Hot Plug Board Removal Process

Operator / Action	Hot Plug Controller	Software
A. Removes board from slot.	**1.** Clears the **Slot Status** register *Presence Detect State* bit (Downstream Ports, offset 80h[22]). **1.** Sets the **Slot Status** register *Presence Detect Changed* bit (Downstream Ports, offset 80h[19]). **2.** Generates an Interrupt Message due to Presence Detect change, if enabled. **3.** Clears the **Link Status** register *Data Link Layer Link Active* bit (Downstream Ports, offset 78h[29]). **4.** Sets the **Slot Status** register *Data Link Layer State Changed* bit (Downstream Ports, offset 80h[24]).	Clears the *Presence Detect Changed* bit. Clears the *Data Link Layer State Changed* bit.
	5. Transmits an Interrupt de-assertion Message, if enabled.	

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Chapter 10 Power Management

10.1 Overview

The PEX 8605 Power Management (PM) features provide the following services:

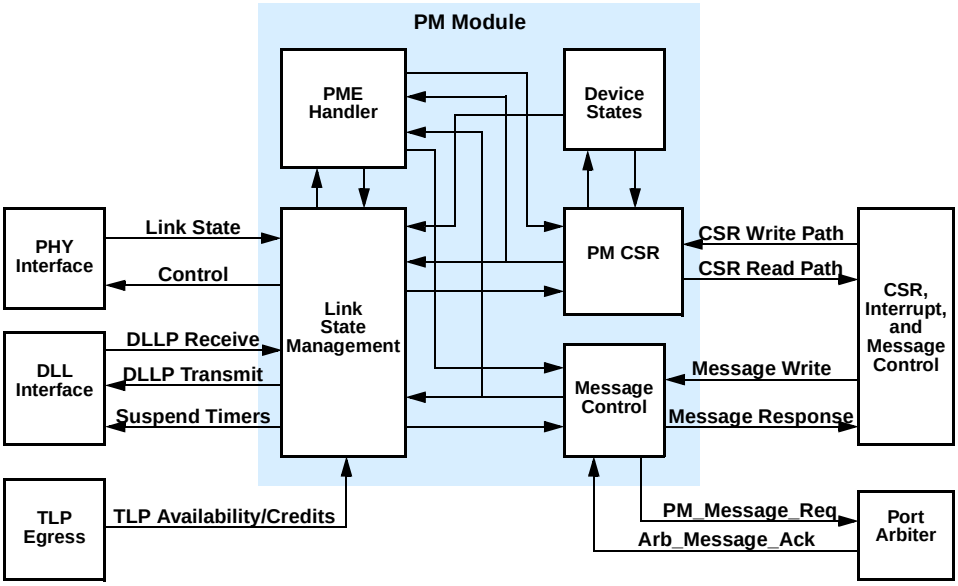
- Mechanisms to identify PM capabilities
- Ability to transition into certain PM states
- Notification of the current PM state of each Port
- Support for the option to wakeup the system upon a specific event in the D3cold state

The PEX 8605 supports hardware-autonomous PM and software-driven D-State PM. The switch also supports the L0s and L1 Link PM states in hardware-autonomous Active State Power Management (ASPM), as well as the L1, L2/L3 Ready, and L3 Link PM states in Conventional PCI-compatible PM. D0, D1, D2, D3hot, and D3cold states are supported in Conventional PCI-compatible PM. The PEX 8605 supports Vaux; therefore, Power Management Event (PME) generation from the D3cold state is supported.

The PM module interfaces with a Physical Layer (PHY) electrical sub-block, to transition the Link state into a low-power state, when the module receives a Power State Change Request from a downstream component, or an internal event forces the Link state entry into low-power states in hardware-autonomous ASPM mode. PCI Express Link states are not directly visible to Conventional PCI Bus driver software; however, they are derived from the PM state of the components residing on those Links.

Figure 10-1 provides a functional block diagram of the PEX 8605 PM module.

Figure 10-1. PM Module Functional Block Diagram



10.2 Power Management Features

- *PCI Express Base r2.1*-compliant
- *PCI Power Mgmt. r1.2*-compliant
- Link Power Management States (*L-States*; also referred to as *Link PM states*)
  - PCI Bus Power Management – L1, L2/L3 Ready, and L3 (Vaux is supported)
  - Active State Power Management (ASPM) – L0s and L1
- Device Power Management States (*D-States*; also referred to as *Device PM states*)
  - D0 (D0 Uninitialized and D0active), D1, D2, and D3 (D3hot and D3cold) support
- Power Management Event (PME) support from the D3hot state
- Wakeup forward support from the D3cold state, when Vaux is present
- Beacon forwarding and WAKE#-to-beacon conversion functionality in the D3cold state, when Vaux is present
- PME due to Hot Plug events
- Forwards PME_Turn_Off broadcast Messages
- Implements Gen 2-specific Control and Status registers, and associated interrupts
- Supports *PCI Express Base r2.1*-compliant ASPM optionality compliance feature

10.3 Power Management Capability

10.3.1 Device Power Management States

The PEX 8605 supports the PCI Express PCI-PM D0, D1, D2, D3hot, and D3cold states.

The D1, D2, and D3hot states can be entered from the D0 Uninitialized or D0 Active states, when system software programs the Port's **PCI Power Management Status and Control** register *Power State* field (All Ports, offset 44h[1:0]) to the corresponding Device PM state. The PCI-PM D0 Uninitialized state can be entered from the D3hot state when system software Clears the Port's *Power State* field.

10.3.1.1 D0 State

A PCI Express device must be put into the PCI Express PCI-PM D0 state before it can be used. When the device enters the D0 state following a Fundamental Reset, it is in the D0 Uninitialized state. A subsequent Reset forces the device into the D0 Uninitialized state.

Other than the Fundamental Reset that brings the device to the D0 Uninitialized state, all other PM state transitions are explicitly controlled by software.

A device enters the PCI Express PCI-PM D0 Active state when system software Sets any combination of the **PCI Command** register *Bus Master Enable*, *Memory Access Enable*, and/or *I/O Access Enable* bits (All Ports, offset 04h[2, 1, and/or 0], respectively).

10.3.1.2 D1 and D2 States

After the PEX 8605 is in the D0 state, the switch can later be transitioned into the D1 or D2 state. When in the D1 or D2 state, Hot Plug and/or Port Link state operations can cause the PEX 8605 to generate a PME.

Only Type 0 Configuration accesses are allowed in the D1 or D2 state. Memory and I/O transactions result in an Unsupported Request (UR). Completions flowing in either direction are not affected.

Type 1 transactions flowing toward a PEX 8605 Port in the D1 or D2 state are terminated as URs. Type 0 Configuration transactions successfully complete. When Port 0 is programmed into the D1 or D2 state, the Port initiates Conventional PCI-PM L1 Link PM state entry.

10.3.1.3 D3hot State

In the PCI Express PCI-PM D3hot state, PCI Express Hot Plug or Link State operations can cause the PEX 8605 to generate a PME.

Only Type 0 Configuration accesses are allowed in the D3hot state. Memory and I/O transactions result in an Unsupported Request (UR). Completions flowing in either direction are not affected.

Type 1 transactions flowing toward a PEX 8605 Port in the D3hot state are terminated as URs. Type 0 Configuration transactions complete successfully. When the PEX 8605 Upstream Port is programmed to the D3hot state, the Port initiates Conventional PCI-PM L1 Link PM state entry.

After the PEX 8605 is in the D3hot state, the switch can later be transitioned into the D3cold state. This is done by removing power from PLL_AVDD, VDD_CORE, and VDD_IO supplies, while the remaining power supply pins are powered from auxiliary power (Vaux). Functions that are in the D3hot state can be transitioned, by software, to the D0 Uninitialized state. When in the D3hot state, Hot Plug or Link State operations cause a PME in the PEX 8605.

10.3.1.4 D3cold Device Power Management State

After the PEX 8605 is in the D3cold state, the switch can be transitioned into the D3cold state. The PCI Express Host system can later transition the upstream Link to the L2/L3 Ready Link PM state, by sending the PME_Turn_Off Message.

After Port 0 enters the L2/L3 Ready Link PM state, the system asserts PEX_PERST# input, and Reference Clocks and PLL_AVDD, VDD_CORE, and VDD_IO power supplies are removed. The PEX 8605 enters the D3cold state and Links settle into the L2 Link PM state if the system provides a Vaux supply.

If the system provides a Vaux supply, when in the D3cold state with Vaux, the PEX 8605 has the ability to forward remote Wakeup signaling toward the Root Complex from PCI Express endpoint devices. Devices can generate remote Wakeup, by driving WAKE# signaling or by in-band beacon signaling.

The PEX 8605 drives beacon signaling toward the upstream Root Complex, when either of the following occurs:

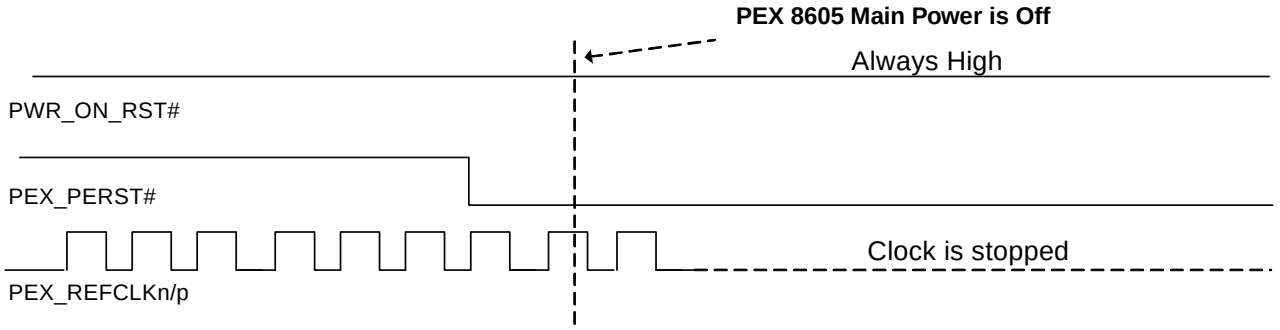
- Beacon signaling is detected on any downstream Port that was in the L2 Link PM state
- WAKE# is sampled as asserted Low, when the PEX 8605 is in the D3cold state, in systems that provide a Vaux supply

D3cold State Entry

Entry to the D3cold state is initiated by the PCI Express Host sending PME_Turn_Off Messages. After all Links are in the L2/L3 Ready Link PM state, the PEX 8605 is ready to enter the D3cold state. The PCI Express Host asserts PEX_PERST#, removes the PCI Express 100 MHz Reference Clock, and turns Off main power. After main power is removed, and if the connector Vaux supply is present, the PEX 8605 settles into the D3cold state, drawing minimum current from the Vaux power rails. All PCI Express Links settle into the L2 Link PM state.

Figure 10-2 explains the timing diagram of D3cold entry. PWRON_RST# is asserted High and PEX_PERST# is asserted Low. After PEX_PERST# assertion, PEX_REFCLKn/p can be turned Off.

Figure 10-2. D3cold Entry Timing Diagram



D3cold State Exit

Exit from the D3cold state can be initiated by the PCI Express device, by driving beacon or WAKE# (WAKE# input) signaling. The system WAKE# pin must be connected to the PEX 8605's bidirectional WAKE# pin.

Figure 10-3 explains the PCI Express device exiting the D3cold state, by driving beacon signaling. In turn, the PEX 8605 drives beacon signaling toward the Root Complex, and also drives WAKE# Low.

Figure 10-4 explains another way of the PCI Express device exiting the D3cold state, by driving WAKE# signaling. In this case, PEX 8605 drives WAKE# and beacon signaling toward the Root Complex, to wakeup the system.

After main power is On and the PCI Express Host wakes up, the Reference Clock is turned On. Then, after power and clocks are stable (100-ms minimum), PEX_PERST# is de-asserted.

Figure 10-5 explains the timing diagram when exiting D3cold state. Exit from the D3cold state can also be due to the Host returning to the D0 state after turning On the main power and Reference Clock.

Figure 10-3. Exit from D3cold Due to Beacon Signaling from PCI Express Device

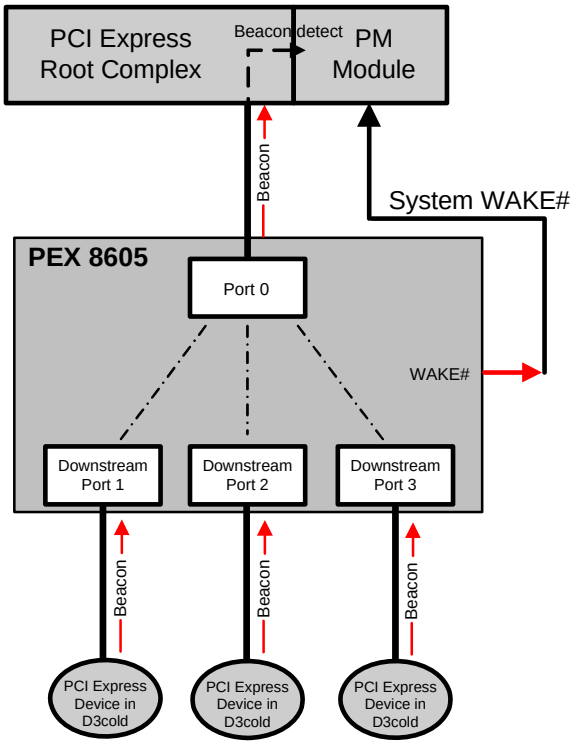


Figure 10-4. D3cold Exit Due to PCI Express Device Driving WAKE# Pin Low

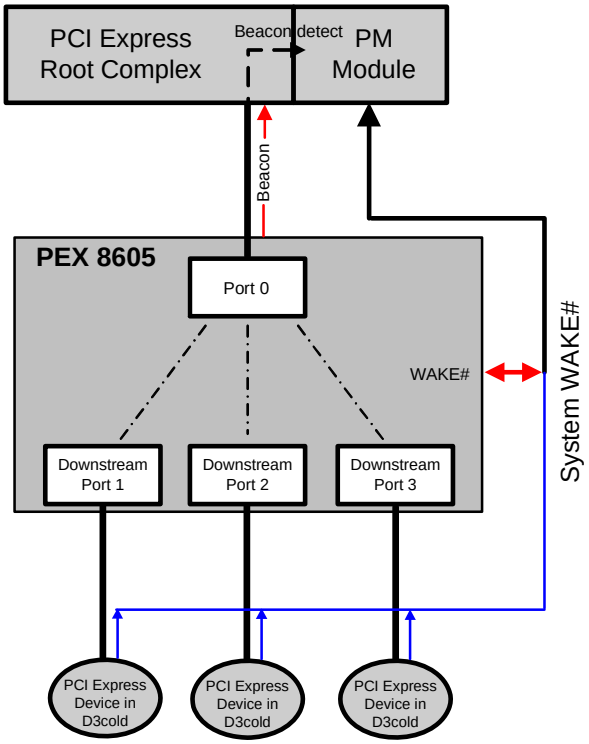
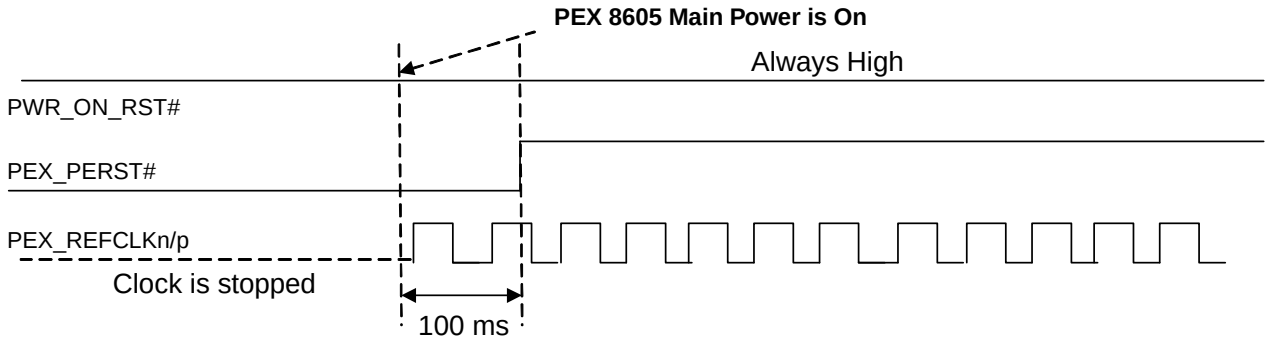


Figure 10-5. D3cold Exit Timing Diagram



10.3.2 Link Power Management States

The PEX 8605 components hold their upstream Link and downstream Links in the L0 Link PM state when they are in the standard operational state (Conventional PCI-PM state is in the D0 Active state). ASPM defines a mechanism for components in the D0 state, to reduce Link power by placing their Links into a low-power state and instructing the other end of the Link to do likewise. This allows hardware-autonomous, dynamic Link power reduction beyond what is achievable by software-only-controlled PM. Table 10-1 defines the relationship between the Power state of a component and its upstream Link. Table 10-2 defines the relationship between Link PM states and power-saving actions.

Conventional PCI PM and the L1 Link PM state are controlled by system software programming the PEX 8605 into the D1, D2, or D3hot state. Similarly, the L2/L3 Ready and L2 Link PM states are controlled by the D3hot state, and subsequently cause the Root Complex to broadcast the PME_Turn_Off Message to the downstream hierarchy.

Table 10-1. Relationship between Component Power State and Upstream Link

Downstream Component State	Permissible Upstream Component State	Permissible Interconnect Link PM State
D0	D0	L0, L0s, L1 (optional) – ASPM.
D1	D0-to-D1	L1, L2/L3 Ready.
D2	D0-to-D2	L1, L2/L3 Ready.
D3hot	D0-to-D3hot	L1, L2/L3 Ready.
D3cold (Vaux)	D0-to-D3cold	L2 (Vaux present), L3 (Vaux not present).

Table 10-2. Relationship between Link PM States and Power-Saving Actions

Link PM State	Power-Saving Actions
Tx L0s	PHY Tx Lanes are in a High-Impedance state.
Rx L0s	PHY Rx Lanes are in a low-power state.
L1	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended.
L2/L3 Ready	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended. Can optionally turn off the PEX 8605 internal clocks.
L2 (D3cold with Vaux present)	Auxiliary power state when in D3cold with Vaux.
L3 (D3cold)	Component is fully powered Off. Vaux is not present.

10.3.3 PCI Express Power Management Support

The PEX 8605 supports PM features required in the *PCI Express Base r2.1*. Table 10-3 lists supported and non-supported features and the register bits/fields used for configuration or activation.

Table 10-3. Supported PCI Express PM Capabilities

Register		Description	Supported	
Offset	Bit(s)		Yes	No
	PCI Power Management Capability (All Ports)			
	7:0	**Capability ID** Program to 01h, to indicate that the Capability structure is the **PCI Power Management Capability** structure.	✔	
	15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	✔	
	18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	✔	
	19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns a value of 0.		✔
	21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	✔	
40h	24:22	**AUX Current** The **Data** register (All Ports, offset 44h[31:24]) is not implemented, by default. Until serial EEPROM and/or I^2C writes a value, the **Data** register field is all zeros (0s). If serial EEPROM and/or I^2C writes to the **Data** register, the **Data** register will show as implemented, and those agents can then Clear the AUX Current value. If the **Data** registers are implemented: **1.** This field returns a value of 000b. **2.** The **Data** register takes precedence over this field. If wakeup from the D3cold state is not supported, this field returns a value of 000b.	✔	
	25	**D1 Support** 1 = PEX 8605 supports the D1 state	✔	
	26	**D2 Support** 1 = PEX 8605 supports the D2 state	✔	
	31:27	**PME Support** Bits [31, 30, and 27] must be Set to indicate that the PEX 8605 will forward PME Messages, as required by the *PCI Express Base r2.1*.	✔	

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
44h		**PCI Power Management Status and Control (All Ports)**		
	1:0	**Power State** Used to determine the current Device PM state of the Port, and to program the Port into a new Device PM state. 00b = D0 01b = D1 10b = D2 11b = D3hot	✔	
	3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 state, because of Power State commands, do not perform an internal reset.	✔	
	8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8605 Port 1 = Enables PME generation by the corresponding PEX 8605 Port	✔	
	12:9	**Data Select** Initially writable by serial EEPROM and/or I^2C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I^2C Write occurs to this register. Selects the field [14:13] (*Data Scale*) and **PCI Power Management Data** register *Data* field (All Ports, offset 44h[31:24]). 0h = D0 power consumed 1h = D1 power consumed 2h = D2 power consumed 3h = D3 power consumed All other encodings are ***reserved***.	✔	
	14:13	**Data Scale** Writable by serial EEPROM and/or I^2C only[a]. Indicates the scaling factor to be used when interpreting the **PCI Power Management Data** register *Data* field (All Ports, offset 44h[31:24]) value. The value and meaning of the *Data Scale* field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal *Data Scale* fields (one each, per *Data Select* values 0h, 1h, 2h, and 3h), per Port. For other *Data Select* values, the *Data* value returned is 00h.	✔	
	15	**PME Status** 0 = PME is not generated by the corresponding PEX 8605 Port 1 = PME is being generated by the corresponding PEX 8605 Port	✔	

*a. With no serial EEPROM nor previous I^2C programming, Reads return a value of 00h for the **PCI Power Management Status and Control** register Data Scale and **PCI Power Management Data** register Data fields (for all Data Selects).*

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
44h		**PCI Power Management Control/Status Bridge Extensions (All Ports)**		
	22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
	23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
		PCI Power Management Data (All Ports)		
	31:24	**Data** Writable by serial EEPROM and/or I^2C only[a]. There are four supported *Data Select* values (0h, 1h, 2h, and 3h), per Port. For other *Data Select* values, the *Data* value returned is 00h. Selected by the **PCI Power Management Status and Control** register *Data Select* field (All Ports, offset 44h[12:9]).	✔	
6Ch		**Device Capability (All Ports)**		
	8:6	**Endpoint L0s Acceptable Latency** Because the PEX 8605 is a switch and not an endpoint, the PEX 8605 does ***not support*** this feature. 000b = Disables the capability		✔
	11:9	**Endpoint L1 Acceptable Latency** Because the PEX 8605 is a switch and not an endpoint, the PEX 8605 does ***not support*** this feature. 000b = Disables the capability		✔
	25:18	**Captured Slot Power Limit Value (Port 0)** Do not change for downstream Ports. For Port 0, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	✔	
	27:26	**Captured Slot Power Limit Scale (Port 0)** Do not change for downstream Ports. For Port 0, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	✔	

*a. With no serial EEPROM nor previous I^2C programming, Reads return a value of 00h for the **PCI Power Management Status and Control** register Data Scale and **PCI Power Management Data** register Data fields (for all Data Selects).*

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
70h		**Device Control (All Ports)**		
	10	**AUX Power PM Enable**	✔	
		Device Status (All Ports)		
	20	**AUX Power Detected**	✔	
74h		**Link Capability (All Ports)**		
	11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 10b = L1 ASPM is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	✔	
	14:12	**L1 Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Advertised N_FTS** register *Advertised N_FTS* field (Port 0, offset B84h[7:0]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Port's L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = Port's L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.	✔	
	17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Port's L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = Port's L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.	✔	
	18	**Clock Power Management Capable**		✔

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
		Link Control (All Ports)		
78h	1:0	**Active State Power Management (ASPM)** 00b = Disable[c] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries	✔	
	8	**Clock Power Management Enable**		✔
		Slot Capability (Downstream Ports)		
7Ch	0	**Attention Button Present**		✔
	1	**Power Controller Present**		✔
	2	**MRL Sensor Present**		✔
	3	**Attention Indicator Present**		✔

c. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
7Ch		**Slot Capability (Downstream Ports) *(Cont.)***		
	4	**Power Indicator Present**		✔
	5	**Hot Plug Surprise** ***Reserved*** for Port 0. 0 = No device in the corresponding PEX 8605 downstream Port (with an I^2C I/O Expander) slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8605 downstream Port slot can be removed from the system without prior notification	✔	
	6	**Hot Plug Capable** ***Reserved*** for Port 0. Set on the Port where HP_PRSNT# is currently assigned. The PEX 8605 reports Hot Plug capability on only one downstream Port. 0 = Corresponding PEX 8605 downstream Port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8605 Transparent downstream Port slot is capable of supporting Hot Plug operations	✔	
	14:7	**Slot Power Limit Value** ***Reserved*** for Port 0. The maximum power supplied by the corresponding PEX 8605 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the *Slot Power Limit Scale* field value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (Downstream Ports, offset 68h[24]) is Set (default). Serial EEPROM and/or I^2C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	✔	
	16:15	**Slot Power Limit Scale** ***Reserved*** for Port 0. The maximum power supplied by the corresponding PEX 8605 downstream slot is determined by multiplying the value in this field by the *Slot Power Limit Value* field value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (Downstream Ports, offset 68h[24]) is Set (default). Serial EEPROM and/or I^2C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
80h		**Slot Control (Downstream Ports)**		
	1	**Power Fault Detector Enable**		✔
	9:8	**Power Indicator Control**		✔
	10	**Power Controller Control**		✔
		Slot Status (Downstream Ports)		
	17	**Power Fault Detected**		✔
138h		**Power Budget Extended Capability Header (All Ports)**		
	15:0	**PCI Express Extended Capability ID** Program to 0004h, as required by the *PCI Express Base r2.1*.	✔	
	19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.1*.	✔	
	31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	✔	
13Ch		**Data Select (All Ports)**		
	7:0	**Data Select** Indexes the Power Budget data reported, **Power Budget Data** registers, two per Port, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 0 to 1.	✔	

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
140h		**Power Budget Data (All Ports)**		
	7:0	**Base Power** Two registers per Port. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (*Data Scale*) contents to produce the actual power consumption value.	✔	
	9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	
	12:10	**PM Sub-State** 000b = Power Management substate of the operating condition being described	✔	
	14:13	**PM State** Power Management state of the operating condition being described. 00b = D0 state 01b = D1 state 10b = D2 state 11b = D3 state	✔	
	17:15	**Type** Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	✔	
	20:18	**Power Rail** Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	✔	
		Note: *Two registers per Port can be programmed through the serial EEPROM, I^2C, and/or SMBus. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register Data Select field (All Ports, offset 13Ch[7:0]).*		
144h		**Power Budget Capability (All Ports)**		
	0	**System Allocated** 1 = Power budget for the device is included within the system power budget	✔	

Table 10-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
1E0h	Power Management Hot Plug User Configuration (All Ports)			
	0	**L0s Entry Idle Counter** Traffic idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs	✔	
	2	**HPC PME Turn-Off Enable** Functionality associated with this bit is enabled only on the downstream Ports. 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	✔	
	7	**Disable PCI Express PM L1 Entry** 1 = Disables L1 Link PM state entry on Port 0, when Port 0 is placed into the D3hot state	✔	
	10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	✔	

10.4 Power Management Tracking

Port 0 logic tracks the Link status of each downstream Port and Port 0 Link, to derive the following conditions:

- Port 0 enters the L0s Link PM state when all enabled downstream Receivers are in the L0s Link PM state or deeper, or in a Link Down state.
- Port 0 enters the active L1 Link PM state, only when all downstream Ports are in the active L1 Link PM state or deeper, or the Link is down.
- When a downstream Port is in the active L1 Link PM state and an ASPM L1 Link PM state exit is occurring in the downstream Port, Port 0 exits the L1 Link PM state.
- When Port 0 is in the active L1 Link PM state and an active L1 Link PM state exit is occurring, due to Receiver Electrical Idle exit, the downstream Port exits the L1 Link PM state.
- When a PME_TO_Ack Message is received only on all active (not in Link Down) downstream Ports, a PME_TO_Ack Message is issued toward Port 0.
- When all downstream Ports are in the L2/L3 Ready Link PM or Link Down state, Port 0 transmits PM_ENTER_L23 DLLPs toward the Root Complex.

10.5 Power Management Event Handler

PM_PME Messages are Posted Transaction Layer Packets (TLPs) that inform the PM software which agent within the PCI Express hierarchy has requested a PM-state change. PM_PME Messages are always routed toward the Root Complex.

PCI Express components are permitted to wake the system from any supported PM state, through the request of a PME.

When a PEX 8605 downstream Port is in the D1, D2, or D3hot state, the following Hot Plug events cause the **PCI Power Management Status and Control** register *PME Status* bit (All Ports, offset 44h[15]) to be Set:

- Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
- Data Link Layer State Changed

This causes the downstream Port to generate a PM_PME Message, if the **PCI Power Management Status and Control** register *PME Enable* bit (All Ports, offset 44h[8]) is Set.

*a. The SerDes Receiver Detect mechanism is comprised of the **Physical Layer Receiver Detect Status** register Receiver Detected on Lane x bits (Port 0, offset 200h[19:16]).*

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Chapter 11 Registers

11.1 Introduction

This chapter defines the PEX 8605 registers. Each PEX 8605 Port has its own Configuration, Capability, Control, and Status register space. The register mapping is the same for each Port. (Refer to Table 11-1.) This chapter also presents the PEX 8605 programmable registers and the order in which they appear in the register map. Register descriptions, when applicable, include details regarding their use and meaning in Port 0 and downstream Ports. (Refer to Table 11-4.)

All PEX 8605 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI-to-PCI Bridge r1.2*
- *PCI Express Base r2.1*

11.2 Type 1 Register Map

Table 11-1 defines the Type 1 register mapping.

Table 11-1. Type 1 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)		Capability Pointer (40h)	00h … 34h … 3Ch
PCI Power Management Capability Registers (Offsets 40h – 44h)	Next Capability Pointer (48h)	Capability ID (01h)	40h 44h
MSI Capability Registers (Offsets 48h – 64h)	Next Capability Pointer (68h)	Capability ID (05h)	48h … 64h
PCI Express Capability Registers (Offsets 68h – A0h)	Next Capability Pointer (A4h)	Capability ID (10h)	68h … A0h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)	Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh)	A4h … FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)	100h
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)			… 134h
Next Capability Offset (148h)	1h	PCI Express Extended Capability ID (0004h)	138h
Power Budget Extended Capability Registers (Offsets 138h – 144h)			… 144h
Next Capability Offset (950h or 520h)	1h	PCI Express Extended Capability ID (0002h)	148h
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)			… 1BCh
Device-Specific Registers (Offsets 1C0h – 444h)			1C0h … 51Ch
Next Capability Offset (950h)	1h	PCI Express Extended Capability ID (000Dh)	520h
ACS Extended Capability Registers (Offsets 520h – 52Ch)			… 52Ch

Table 11-1. Type 1 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers (Offsets 530h – B88h)		530h …
Next Capability Offset 2 (000h)	1h PCI Express Extended Capability ID 2 (000Bh)	950h …
Device-Specific Registers (Offsets 530h – B88h)		B88h
Factory Test Only/Reserved	B8Ch –	FB0h
Next Capability Offset (138h or 148h)	1h PCI Express Extended Capability ID (0001h)	FB4h …
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)		FDCh
Reserved	FE0h –	FFCh

11.3 Register Configuration and Map

The PEX 8605 registers are configured similarly – not all the same. Port 0 includes more Device-Specific registers than the other Ports. Port 0 also contains registers that are used to set up and control the PEX 8605, as well as a serial EEPROM interface, I^2C Slave interface, and SMBus Slave interface logic and control. The Port registers contain setup and control information specific to each Port.

Table 11-2 defines the register configuration and map.

Table 11-2. Register Configuration and Map

Register Types	Port 0	Ports 1, 2, and 3
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)	00h – 3Ch	00h – 3Ch
PCI Power Management Capability Registers (Offsets 40h – 44h)	40h – 44h	40h – 44h
MSI Capability Registers (Offsets 48h – 64h)	48h – 64h	48h – 64h
PCI Express Capability Registers (Offsets 68h – A0h)	68h – A0h	68h – 80h 8Ch – A0h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)	A4h – FCh	A4h – FCh
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)	100h – 134h	100h – 134h
Power Budget Extended Capability Registers (Offsets 138h – 144h)	138h – 144h	
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)	148h – 1BCh	148h – 1BCh
Device-Specific Registers (Offsets 1C0h – 444h)		
Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)	1C0h – 1FCh	1E0h – 1ECh, 1F8h, 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h – 25Ch	
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)	260h – 26Ch	
Device-Specific Registers – I2C and SMBus Slave Interfaces (Offsets 290h – 2C4h)	290h – 2C4h	
ACS Extended Capability Registers (Offsets 520h – 52Ch)	Downstream Port 520h – 52Ch	
Device-Specific Registers (Offsets 530h – B88h)		
Device-Specific Registers – Port Configuration (Offset 574h)	574h	
Device-Specific Registers – General-Purpose Input/Output Control (Offsets 62Ch – 63Ch)	62Ch – 63Ch	
Device-Specific Registers – Negotiated Link Width (Offsets 660h – 67Ch)	660h – 67Ch	
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)	950h – 95Ch	950h – 95Ch
Device-Specific Registers – Ingress Credit Handler Control and Status (Offsets 9F0h – 9FCh)	9F0h – 9FCh	
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – A2Ch)	A00h – A2Ch	
Device-Specific Registers – Physical Layer (Offsets B80h – B88h)	B80h – B88h	
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)	FB4h – FDCh	FB4h – FDCh

Table 11-3 lists registers that are generally individual registers that support all Ports (changing the register value in one Port changes the same register in all Ports).

Table 11-3. Singular Registers Shared by All Ports

Offset	Register	Comment
00h	Vendor ID and Device ID	
08h	PCI Class Code and Revision ID	
34h	Capability Pointer	
A4h	Subsystem Capability	
A8h	Subsystem Vendor ID and Subsystem ID	
100h	Device Serial Number Extended Capability Header	
104h	Serial Number (Lower DW)	
108h	Serial Number (Upper DW)	
520h	ACS Extended Capability Header	
950h	Vendor-Specific Extended Capability 2	
954h	Vendor-Specific Header 2	
958h	Hardwired Vendor ID and Hardwired Device ID	
95Ch	Hardwired Revision ID	

11.4 Register Access

Each Port implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8605 supports six mechanisms for accessing the registers:

- PCI r3.0-Compatible Configuration Mechanism
- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- I^2C Slave Interface (refer to Section 7.2, "I2C Slave Interface")
- SMBus Slave Interface (refer to Section 7.3, "SMBus Slave Interface")
- Serial Peripheral Interface (SPI) Bus (refer to Chapter 6, "Serial EEPROM Controller")

The sideband register access mechanisms (serial EEPROM, I^2C, and/or SMBus) can modify Read-Only (RO) register values.

Each Port captures the Bus Number and Device Number on every Type 0 Configuration Write, as required by the *PCI r3.0*. Therefore, following a Fundamental Reset, software must initially perform a Configuration Write to each Port (using either the PCI r3.0-Compatible Configuration Mechanism or PCI Express Enhanced Configuration Access Mechanism), to allow each Port to capture its designated Bus Number and Device Number. The initial access to each Port, *for example*, could be a Configuration Write Request to a RO register, *such as* the **Device ID** / **Vendor ID** register (All Ports, offset 00h).

11.4.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8605 Ports' first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space. The mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8605 Configuration registers. Each Port can convert a Type 1 Configuration Request (destined to a downstream Port or device) to a Type 0 Configuration Request (targeting the next downstream Port or device), as described below.

The PEX 8605 decodes all Type 1 Configuration accesses received on Port 0, when any of the following conditions exist:

- If the Bus Number in the Configuration access is not within Port 0's Secondary Bus Number and Subordinate Bus Number range, Port 0 responds with an Unsupported Request (UR).
- Specified Bus Number in the Configuration access is the PEX 8605 internal virtual PCI Bus Number, the PEX 8605 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the PCI-to-PCI bridge in one of the PEX 8605 downstream Ports, the PEX 8605 processes the Read or Write Request to the specified downstream Port register specified in the original Type 1 Configuration access.
  - If the specified Device Number does not correspond to any of the PEX 8605 downstream Port Device Numbers, the PEX 8605 responds with a UR.

- If the specified Bus Number in the Type 1 Configuration access is not the PEX 8605 internal virtual PCI Bus Number, but is the Bus Number of one of the PEX 8605 downstream Port secondary/subordinate buses, the PEX 8605 passes the Configuration access on to the PCI Express Link attached to that PEX 8605 downstream Port.
  - If the specified Bus Number is the downstream Port Secondary Bus Number, and the specified Device Number is 0, the PEX 8605 converts the Type 1 Configuration access to a Type 0 Configuration access before passing it on.
  - If the specified Device Number is not 0, the downstream Port drops the Transaction Layer Packet (TLP) and generates a UR.
- If the specified Bus Number is not the downstream Port Secondary Bus Number, the PEX 8605 passes along the Type 1 Configuration access, without change.

Because the mechanism is limited to the first 256 bytes of the PCI Express Configuration Space of the PEX 8605 Ports, the PCI Express Enhanced Configuration Access Mechanism or Device-Specific Memory-Mapped Configuration Mechanism must be used to access beyond Byte FFh. The PCI Express Enhanced Configuration Access mechanism can access the registers in the PCI-compatible region, as well as those in the PCI Express Extended Configuration Space.

11.4.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism is implemented on all PCI Express PCs and on systems that do not implement a processor-specific firmware interface to the Configuration Space. The mechanism provides a Memory-Mapped Address space in the Root Complex, through which the Root Complex translates a Memory access into one or more Configuration Requests. Device drivers normally use an application programming interface (API) provided by the Operating System (OS), to use this mechanism.

The mechanism can be used to access all PEX 8605 registers.

11.4.3 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the Configuration registers of all Ports within a single 128-KB Memory map, as listed in Table 11-4. The registers are contained within a 4-KB range. To use this mechanism, program the Port 0 Type 1 Configuration Space **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively), which are typically enumerated at boot time by BIOS and/or the OS software. After the Port 0 BARs are enumerated, Port 0 registers can be accessed with Memory Reads from and Writes to the first 4 KB (0000h to 0FFFh), Port 1 registers can be accessed with Memory Reads from and Writes to the second 4 KB (1000h to 1FFFh), and so forth. (Refer to Table 11-4.) Within each of these 4-KB windows, individual registers are located at the DWord offsets indicated in Table 11-1.

Port 0 **BAR0** and **BAR1** are typically enumerated at boot time, by BIOS and/or the OS software.

This mechanism follows the *PCI Express Base r2.1* Configuration Request Routing rules, which do not allow the propagation of Configuration Requests from downstream-to-upstream, nor peer-to-peer. By default, if a downstream Port receives a Memory Request from a downstream device targeting the PEX 8605 Configuration registers, the Port:

- Responds to a Memory Read Request with a UR
- By default, silently discards a Memory Write Request (in compliance with the *PCI Express Base r2.1*)

In Memory Requests that target PEX 8605 registers, the Payload Length indicated within the Memory Request Header must be 1 DWord. Lengths greater than 1 DWord result in a Completer Abort error.

Table 11-4. Port Register Offsets from Port 0 BAR0/1 Base Address

Port Number	Register Offset from Port 0 BAR0/1	Location Range
0 (upstream)	0000h to 0FFFh	0 to 4 KB
1 (downstream)	1000h to 1FFFh	4 to 8 KB
2 (downstream)	2000h to 2FFFh	8 to 12 KB
3 (downstream)	3000h to 3FFFh	12 to 16 KB

11.5 Register Descriptions

The remainder of this chapter details the PEX 8605 registers, including:

- Bit/field names
- Description of register functions for each Port
- Type (*such as* RW or HwInit; refer to Table 11-5 for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8605 serial EEPROM and/or I^2C/SMBus Initialization feature
- Default power-on/reset value

Table 11-5. Register Types, Grouped by User Accessibility

Type	Description
HwInit	**Hardware-Initialized** Refers to the PEX 8605 Hardware-Initialization mechanism or PEX 8605 Serial EEPROM or I^2C register Initialization features. RO after initialization and can only be reset with a Fundamental Reset. HwInit register bits are not modified by a Soft Reset.
RO	**Read-Only** Read-Only and cannot be altered by software. Permitted to be initialized by the PEX 8605 Hardware-Initialization mechanism or PEX 8605 serial EEPROM and/or I^2C register Initialization features.
ROS	**Read-Only, Sticky** Same as RO, except that bits are neither initialized nor modified by a Soft Reset.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are RO and must return a value of 0 when read. Software must preserve the value read for Writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are RO and must return a value of 0 when read. Software must use 0 for Writes to bits.
RW	**Read-Write** Read/Write and permitted to be Set or Cleared by software to the needed state.
RW1C	**Write 1 to Clear Status** Indicates status when read. A status bit Set by the system (to indicate status) is Cleared by writing 1 to that bit. Writing 0 to the bit has no effect.
RW1CS	**Write 1 to Clear, Sticky** Same as RW1C, except that bits are neither initialized nor modified by a Soft Reset.
RWS	**Read-Write, Sticky** Same as RW, except that bits are Set or Cleared by software to the needed state. Bits are neither initialized nor modified by a Soft Reset.
RWU	**Read/Write (Output Pin), Read-Only (Input Pin)** Specific to the GPIO*x Data* register bits. When the referenced GPIO*x* pin is configured as output, the value written appears on the output pin, and are returned by a Read. When the referenced GPIO*x* pin is configured as an input, Reads to this bit always return the pin state, and Writes have no effect.
RZ	**Software Read Zero** Software Read always returns a value of 0; however, software is allowed to write this register.
W1RZ	**Write 1 to Clear, Software Read Zero** Write 1 to activate the function. Reads to this bit always return a value of 0.

11.6 PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the PCI-Compatible Type 1 Configuration Header registers. Table 11-6 defines the register map.

Table 11-6. PCI-Compatible Type 1 Configuration Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Reserved)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Secondary Latency Timer ***(Not Supported)***	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status	***Not Supported/Reserved***	I/O Limit	I/O Base	1Ch
Memory Limit		Memory Base		20h
Prefetchable Memory Limit		Prefetchable Memory Base		24h
Prefetchable Memory Upper Base Address				28h
Prefetchable Memory Upper Limit Address				2Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		30h
Reserved			Capability Pointer (40h)	34h
Expansion ROM Base Address ***(Reserved)***				38h
Not Supported/Reserved	Bridge Control	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 11-1. 00h PCI Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8605, if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	8605h

Register 11-2. 04h PCI Command/Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Command				
0	**I/O Access Enable** 0 = PEX 8605 ignores I/O Space accesses on the Port's primary interface 1 = PEX 8605 responds to I/O Space accesses on the Port's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8605 ignores Memory Space accesses on the Port's primary interface 1 = PEX 8605 responds to Memory Space accesses on the Port's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8605 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8605 handles Memory and I/O Requests received on the Port's downstream/secondary interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8605 returns a Completion with UR Completion status. Because MSI Messages are in-band Memory Writes, disables MSI Messages as well. 1 = PEX 8605 forwards Memory and I/O Requests upstream.	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0

Register 11-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex, and, enables primary interface forwarding of ERR_FATAL and ERR_NONFATAL Messages from downstream Ports and devices when the Port's **Bridge Control** register *SERR# Enable* bit (All Ports, offset 3Ch[17]) is Set	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
10	**Interrupt Disable** 0 = Port is enabled to generate INT*x* Interrupt Messages and assert PEX_INTA# output 1 = Port is prevented from generating INT*x* Interrupt Messages and asserting PEX_INTA# output	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h

Register 11-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* Interrupt Message is pending 1 = INT*x* Interrupt Message is pending internally to the Port –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.1*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the Port Sets this bit when the Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the secondary to the primary interface, –or– • Receives a Completion marked as poisoned on the primary interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8605 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (All Ports, offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	00b
27	**Signaled Target Abort** Port 0 Sets this bit if one of the following conditions exist: • Port 0 receives a Memory Request targeting a PEX 8605 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • Port 0 receives a Memory Request targeting a PEX 8605 register address within a non-existent Port • Downstream Port Sets this bit if it detects an Access Control Services (ACS) violation This error is reported by the **Uncorrectable Error Status** register *Completer Abort Status* bit (All Ports, offset FB8h[15]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 11-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**Received Target Abort** ***Reserved***	RsvdP	No	0
29	**Received Master Abort** ***Reserved***	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the Port Sets this bit when it transmits or forwards an ERR_FATAL or ERR_NONFATAL Message upstream. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (All Ports, offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (All Ports, offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = Port received a Poisoned TLP on its primary side, regardless of the bit 6 (*Parity Error Response Enable*) state	RW1C	Yes	0

Register 11-3. 08h PCI Class Code and Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Revision ID				
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (AAh or ABh), the PLX-assigned Revision ID for this version of the PEX 8605. The PEX 8605 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	AAh or ABh
PCI Class Code				**060400h**
15:8	**Register-Level Programming Interface** The PEX 8605 Ports support the *PCI-to-PCI Bridge r1.2* requirements, but not subtractive decoding, on their upstream interface.	RO	Yes	00h
23:16	**Sub-Class Code** PCI-to-PCI bridge.	RO	Yes	04h
31:24	**Base Class Code** Bridge device.	RO	Yes	06h

Register 11-4. 0Ch Miscellaneous Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8605 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** The Port's Configuration Space Header adheres to the Type 1 PCI-to-PCI Bridge Configuration Space layout defined by the *PCI-to-PCI Bridge r1.2*.	RO	No	01h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	**PCI BIST** ***Reserved*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 11-5. 10h Base Address 0 (Port 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**Memory Space Indicator** 0 = Base Address register maps the PEX 8605 Configuration registers into Memory space ***Note:*** *Port 0 is hardwired to 0.*	Port 0	RO	No	0
	Reserved	Downstream	RsvdP	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	Port 0	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8605 Configuration registers into Non-Prefetchable Memory space ***Note:*** *Port 0 is hardwired to 0.*	Port 0	RO	Yes	0
	Reserved	Downstream	RsvdP	No	0
13:4	***Reserved***		RsvdP	No	0-0h
31:14	**Base Address 0** Base Address (**BAR0**) for the Device-Specific Memory-Mapped Configuration mechanism.	Port 0	RW	Yes	0-0h
	Reserved	Downstream	RsvdP	No	0-0h

Register 11-6. 14h Base Address 1 (Port 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1** RO when the **Base Address 0** (**BAR0**) register is not enabled as a 64-bit BAR (*Memory Map Type* field (Port 0, offset 10h[2:1]) is not programmed to 10b).	Port 0	RW	Yes	0000_0000h
	For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (Port 0, offset 10h[2:1]) is programmed to 10b.	Downstream	RsvdP	Yes	0000_0000h

Register 11-7. 18h Bus Number (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Primary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment to which the primary interface of this Port is connected. Set by Configuration software.	RW	Yes	00h
15:8	**Secondary Bus Number** Secondary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment that is the secondary interface of this Port. Set by Configuration software.	RW	Yes	00h
23:16	**Subordinate Bus Number** Subordinate Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the highest numbered PCI Bus segment that is subordinate to this Port. Set by Configuration software.	RW	Yes	00h
31:24	**Secondary Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	00h

Register 11-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *If ISA Addressing mode is enabled (**PCI Command** register I/O Access Enable bit (All Ports, offset 04h[0]) is Set), the Port forwards I/O transactions from its primary interface to its secondary interface (downstream) if an I/O address is within the range defined by the **I/O Base** and **I/O Limit** registers when the Base is less than or equal to the Limit.* *Conversely, the Port forwards I/O transactions from its secondary interface to its primary interface (upstream) if an I/O address is outside this Address range. If the Port does not implement an I/O Address range, the Port forwards all I/O transactions on its secondary interface upstream, to its primary interface.*				
I/O Base				
3:0	**I/O Base Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
7:4	**I/O_BAR[15:12]** I/O Base Address[15:12]. The Ports use their **I/O Base** and **I/O Limit** registers to determine the address range of I/O transactions to forward from one interface to the other. I/O Base Address[15:12] bits specify the Port's I/O Base Address[15:12]. The PEX 8605 assumes I/O Base Address[11:0]=000h. For 16-bit I/O addressing, the PEX 8605 assumes Address[31:16]=0000h. For 32-bit addressing, the PEX 8605 decodes Address[31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (All Ports, offset 30h[15:0 and 31:16], respectively).	RW	Yes	Fh
I/O Limit				
11:8	**I/O Limit Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
15:12	**I/O_Limit[15:12]** I/O Limit Address[15:12]. The Ports use their **I/O Base** and **I/O Limit** registers to determine the Address range of I/O transactions to forward from one interface to the other. The I/O Limit Address[15:12] bits specify the Port's I/O Limit Address[15:12]. The PEX 8605 assumes Address bits [11:0] of the I/O Limit Address are FFFh. For 16-bit I/O addressing, the PEX 8605 decodes Address bits [15:0] and assumes Address bits [31:16] of the I/O Limit Address are 0000h. For 32-bit addressing, the PEX 8605 decodes Address bits [31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (All Ports, offset 30h[15:0 and 31:16], respectively). If the I/O Limit Address is less than the I/O Base Address, the PEX 8605 does not forward I/O transactions from the Port's primary/upstream bus to its secondary/downstream bus. However, the PEX 8605 forwards all I/O transactions from the secondary bus of the Port to its primary bus.	RW	Yes	0h

Register 11-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Secondary Status			
20:16	***Reserved***	RsvdP	No	0-0h
21	**66 MHz Capable** ***Not supported*** 0 = Not enabled, because PCI Express does ***not support*** 66 MHz	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Reserved*** Not enabled, because PCI Express does ***not support*** this function.	RsvdP	No	0
24	**Master Data Parity Error** If the **Bridge Control** register *Parity Error Response Enable* bit (All Ports, offset 3Ch[16]) is Set, the Port Sets this bit when transmitting or receiving a TLP on its downstream side, and when either of the following two conditions occur: • Port receives Completion marked poisoned • Port forwards poisoned TLP Write Request If the *Parity Error Response Enable* bit is Cleared, the PEX 8605 never Sets this bit. These errors are reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (All Ports, offset FB8h[12]), and mirrored to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	00b
27	**Signaled Target Abort** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
28	**Received Target Abort** Cleared, as required by the *PCI Express Base r2.1*, because the PEX 8605 never initiates a Request itself.	RsvdP	No	0
29	**Received Master Abort** Cleared, as required by the *PCI Express Base r2.1*, because the PEX 8605 never initiates a Request itself.	RsvdP	No	0
30	**Received System Error** 1 = Downstream Port received an ERR_FATAL or ERR_NONFATAL Message on its secondary interface from a downstream device	RW1C	Yes	0
31	**Detected Parity Error** 1 = Downstream Port received a poisoned TLP from a downstream device, regardless of the **Bridge Control** register *Parity Error Response Enable* bit (All Ports, offset 3Ch[16]) state	RW1C	Yes	0

Register 11-9. 20h Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Memory Base*** *and* ***Memory Limit*** *registers (when the Base is less than or equal to the Limit).* *Conversely, the Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the* ***Prefetchable Memory Base*** *(All Ports, offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(All Ports, offsets 2Ch + 24h[31:16]) registers).*				
Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**MEM_BAR[31:20]** Memory Base Address[31:20]. Specifies the Port's Non-Prefetchable Memory Base Address[31:20]. The PEX 8605 assumes Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**MEM_Limit[31:20]** Memory Limit Address[31:20]. Specifies the Port's Non-Prefetchable Memory Limit Address[31:20]. The PEX 8605 assumes Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 11-10. 24h Prefetchable Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Prefetchable Memory Base*** *(All Ports, offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(All Ports, offsets 2Ch + 24h[31:16]) registers (when the Base is less than or equal to the Limit).* *Conversely, the Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the* ***Memory Base*** *and* ***Memory Limit*** *registers (All Ports, offset 20h)).*				
Prefetchable Memory Base				
0	**Prefetchable Memory Base Capability** 0 = Port supports 32-bit Prefetchable Memory Addressing 1 = Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.1* ***Note:*** *If the application needs 32-bit only Prefetchable space, the serial EEPROM and/or I^2C must Clear both this bit and bit 16 (Prefetchable Memory Limit Capability).*	RO	Yes	1
3:1	***Reserved***	RsvdP	No	000b
15:4	**PMEM_BAR[31:20]** Prefetchable Memory Base Address[31:20]. Specifies the Port's Prefetchable Memory Base Address[31:20]. The PEX 8605 assumes Prefetchable Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Prefetchable Memory Limit				
16	**Prefetchable Memory Limit Capability** 0 = Port supports 32-bit Prefetchable Memory Addressing 1 = Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.1*	RO	Yes	1
19:17	***Reserved***	RsvdP	No	000b
31:20	**PMEM_Limit[31:20]** Prefetchable Memory Limit Address[31:20]. Specifies the Port's Prefetchable Memory Limit Address[31:20]. The PEX 8605 assumes Prefetchable Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 11-11. 28h Prefetchable Memory Upper Base Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
31:0	**PBUP[63:32]** Prefetchable Memory Base Address[63:32]. The PEX 8605 uses this register for Prefetchable Memory Upper Base Address[63:32]. When the **Prefetchable Memory Base** register *Prefetchable Memory Base Capability* field indicates 32-bit addressing, this register is RO and returns a value of 0000_0000h.	Offset 24h[0]=1	RW	Yes	0000_0000h
		Offset 24h[0]=0	RO	No	0000_0000h

Register 11-12. 2Ch Prefetchable Memory Upper Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
31:0	**PLIMUP[63:32]** Prefetchable Memory Limit Address[63:32]. The PEX 8605 uses this register for Prefetchable Memory Upper Limit Address[63:32]. When the **Prefetchable Memory Limit** register *Prefetchable Memory Limit Capability* field indicates 32-bit addressing, this register is RO and returns a value of 0000_0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.*	Offset 24h[16]=1	RW	Yes	0000_0000h
		Offset 24h[16]=0	RO	No	0000_0000h

Register 11-13. 30h I/O Upper Base and Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** The PEX 8605 uses this register for I/O Base Address[31:16]. When the **I/O Base** register *I/O Base Addressing Capability* field indicates 16-bit addressing, this register is RO and returns a value of 0000h.	Offset 1Ch[3:0]=1h	RW	Yes	0000h
		Offset 1Ch[3:0]=0h	RO	No	0000h
31:16	**I/O Limit Upper 16 Bits** The PEX 8605 uses this register for I/O Limit Address[31:16]. When the **I/O Limit** register *I/O Limit Addressing Capability* field indicates 16-bit addressing, this register is RO and returns a value of 0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.*	Offset 1Ch[11:8]=1h	RW	Yes	0000h
		Offset 1Ch[11:8]=0h	RO	No	0000h

Register 11-14. 34h Capability Pointer (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 11-15. 38h Expansion ROM Base Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Expansion ROM Base Address** ***Reserved***	RsvdP	No	0000_0000h

Register 11-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Interrupt Line			
7:0	**Interrupt Line Routing Value** The PEX 8605 does ***not*** use this register; however, the register is included for operating system and device driver use.	RW	Yes	00h
	PCI Interrupt Pin			
15:8	**Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) that the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8605. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
	Bridge Control			
16	**Parity Error Response Enable** Controls the response to Poisoned TLPs. 0 = Disables the **Secondary Status** register *Master Data Parity Error* bit (All Ports, offset 1Ch[24]) 1 = Enables the **Secondary Status** register *Master Data Parity Error* bit (All Ports, offset 1Ch[24])	RW	Yes	0
17	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command** register *SERR# Enable* bit (All Ports, offset 04h[8]) is Set, enables the **PCI Status** register *Signaled System Error* bit (All Ports, offset 04h[30]).	RW	Yes	0
18	**ISA Enable** Modifies the PEX 8605's response to Conventional PCI ISA I/O addresses enabled by the Port's **I/O Base** and **I/O Limit** registers (All Ports, offset 1Ch[7:0 and 15:8], respectively) and located in the first 64 KB of the PCI I/O Address space (0000_0000h to 0000_FFFFh). 0 = Port's **I/O Base** and **I/O Limit** registers, and **I/O Base Upper 16 Bits** and **I/O Limit Upper 16 Bits** registers (All Ports, offset 30h[15:0 and 31:16], respectively), define the Port's I/O Address range 1 = If the Port's I/O Address range (defined by the Port's **I/O Base**, **I/O Limit**, **I/O Base Upper 16 Bits**, **I/O Limit Upper 16 Bits** registers) includes I/O addresses below 64 KB, the upper 768 I/O addresses within each 1-KB block below 64 KB are excluded from the Port's I/O Address range	RW	Yes	0

Register 11-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
19	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 18 (*ISA Enable*) Setting VGA address forwarding is qualified by the **PCI Command** register *Memory Access Enable* and *I/O Access Enable* bits (All Ports, offset 04h[1:0], respectively). The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *Memory Access Enable* and *I/O Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit ***Notes:*** *When Set in an egress Port, the Port is configured as a non-Cut-Thru path. (Refer to Section 2.1.3.2, "Cut-Thru Mode," for further details.)* ***Conventional PCI VGA support*** *– To avoid potential I/O address conflicts, if the VGA Enable bit is Set in Port 0 and a downstream Port, Set the **PCI Command** register I/O Access Enable bit (All Ports, offset 04h[0]) in the remaining downstream Ports, unless those downstream Ports are configured to use default 32-bit address decoding and their I/O Address range is Set above 1_0000h.*	RW	Yes	0

Register 11-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**VGA 16-Bit Decode Enable** Used only when bit 19 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
21	**Master Abort Mode** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
22	**Secondary Bus Reset** 1 = Causes a Hot Reset on the Port's downstream Link	RW	Yes	0
23	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
24	**Primary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
25	**Secondary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
26	**Discard Timer Status** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
27	**Discard Timer SERR# Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
31:28	***Reserved***	RsvdP	No	0h

11.7 PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the PCI Power Management Capability registers. Table 11-7 defines the register map.

Table 11-7. PCI Power Management Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 11-17. 40h PCI Power Management Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Capability ID** Program to 01h, to indicate that the Capability structure is the **PCI Power Management Capability** structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns a value of 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** 0 = Device-Specific Initialization is ***not*** required	RO	Yes	0
24:22	**AUX Current** The **Data** register (All Ports, offset 44h[31:24]) is not implemented, by default. Until serial EEPROM and/or I^2C writes a value, the **Data** register field is all zeros (0s). If serial EEPROM and/or I^2C writes to the **Data** register, the **Data** register indicates that it is implemented, and those agents can then Clear the AUX Current value. If the **Data** register is implemented: **1.** This field returns a value of 000b. **2.** The **Data** register takes precedence over this field. If wakeup from the D3cold state is not supported, this field returns a value of 000b.	RO	Yes	001b
25	**D1 Support** 1 = PEX 8605 supports the D1 state	RO	No	1
26	**D2 Support** 1 = PEX 8605 supports the D2 state	RO	No	1
31:27	**PME Support** Bits [31, 30, and 27] must be Set, to indicate that the PEX 8605 will forward PME Messages, as required by the *PCI Express Base r2.1*.	RO	Yes	1Fh

Register 11-18. 44h PCI Power Management Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the current Device PM state of the Port, and to program the Port into a new Device PM state. 00b = D0 01b = D1 10b = D2 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 0 = D3hot to D0 state change causes a Fundamental Reset of the Port. This reset is propagated to downstream Ports and devices. 1 = Devices transitioning from the D3hot to D0 state, because of Power State commands, do not perform an internal reset.	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8605 Port 1 = Enables PME generation by the corresponding PEX 8605 Port	RWS	No	0
12:9	**Data Select** Initially writable by serial EEPROM and/or I^2C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I^2C Write occurs to this register. Selects the field [14:13] (*Data Scale*) and **PCI Power Management Data** register *Data* field (All Ports, offset 44h[31:24]). 0h = D0 power consumed 1h = D1 power consumed 2h = D2 power consumed 3h = D3 power consumed All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and/or I^2C only[a]. Indicates the scaling factor to be used when interpreting the **PCI Power Management Data** register *Data* field (All Ports, offset 44h [31:24]) value. The value and meaning of the *Data Scale* field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal *Data Scale* fields (one each, per *Data Select* values 0h, 1h, 2h, and 3h), per Port. For other *Data Select* values, the *Data* value returned is 00h.	RO	Yes	00b
15	**PME Status** 0 = PME is not generated by the corresponding PEX 8605 Port 1 = PME is being generated by the corresponding PEX 8605 Port	RW1CS	No	0

Register 11-18. 44h PCI Power Management Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and/or I²C only[a]. There are four supported *Data Select* values (0h, 1h, 2h, and 3h), per Port. For other *Data Select* values, the *Data* value returned is 00h. Selected by the **PCI Power Management Status and Control** register *Data Select* field (All Ports, offset 44h[12:9]).	RO	Yes	00h

*a. With no serial EEPROM nor previous I²C programming, Reads return a value of 00h for the **PCI Power Management Status and Control** register Data Scale and **PCI Power Management Data** register Data fields (for all Data Selects).*

11.8 MSI Capability Registers (Offsets 48h – 64h)

This section details the Message Signaled Interrupt (MSI) Capability registers. Table 11-8 defines the register map.

Table 11-8. MSI Capability Register Map (All Ports)[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved			60h –	64h

*a. Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (All Ports, offset 48h[23]) is Cleared.*

Register 11-19. 48h MSI Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	MSI Capability Header			
7:0	**Capability ID** Program to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** Program to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
	MSI Control			
16	**MSI Enable** 0 = MSIs for the Port are disabled 1 = MSIs for the Port are enabled, and INT*x* Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = Port can request only one MSI Vector 001b = Port can request two MSI Vectors 010b through 111b = Port can request four Vectors	RO	Yes	010b
22:20	**Multiple Message Enable** 000b = Port is allocated one MSI Vector, by default 001b = Port is allocated two MSI Vectors 010b through 111b = Port is allocated four MSI Vectors ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8605 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8605 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8605 does not have Per Vector Masking capability 1 = PEX 8605 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 11-20. 4Ch MSI Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	***Reserved***	RsvdP	No	00b
31:2	**Message Address** ***Note:*** *If the **MSI Control** register MSI 64-Bit Address Capable bit (All Ports, offset 48h[23]) is Set (default), refer to the **MSI Upper Address** register for the MSI Upper Address (All Ports, offset 50h).*	RW	Yes	0-0h

Register 11-21. 50h MSI Upper Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Message Upper Address** This register is valid/used only when the **MSI Control** register *MSI 64-Bit Address Capable* bit (All Ports, offset 48h[23]) is Set. MSI Write transaction upper address[63:32]. ***Note:*** *Refer to the **MSI Address** register for the MSI Lower Address (All Ports, offset 4Ch).*	RW	Yes	0000_0000h

Register 11-22. 54h MSI Data (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The offset for this register changes from 54h, to 50h, when the **MSI Control** register MSI 64-Bit Address Capable bit (All Ports, offset 48h[23]) is Cleared.*				
15:0	**Message Data** MSI Write transaction TLP Payload.	RW	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 11-23. 58h MSI Mask (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Port interrupt sources are grouped into two categories – Power Management/Hot Plug events and GPIO-generated interrupts. The quantity of MSI Vectors that are generated is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (All Ports, offset 48h[19:17 and 22:20], respectively): • If **one** MSI Vector is enabled (default mode), both interrupt events are combined into a single Vector • If **two** MSI Vectors are enabled, the individual vectors indicate: – Vector[0] Hot Plug/Power Management event and GPIO-generated event – Vector[1] ***Reserved*** • If **four** MSI Vectors are enabled (up to two Vectors are used), the individual Vectors indicate: – Vector[0] Hot Plug/Power Management event – Vector[1] ***Reserved*** – Vector[2] GPIO-generated event – Vector[3] ***Reserved*** ***Notes:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (All Ports, offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (All Ports, offset 5Ch).*					
0	**MSI Mask for Power Management or Hot Plug Events** MSI mask for Power Management or Hot Plug event-generated interrupts.	Offset 48h[22:20]≥010b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]≤001b	RW	Yes	0
1	***Reserved***		RsvdP	No	0
2	**MSI Mask for GPIO-Generated Interrupts**	Offset 48h[19:17]≥010b and Offset 48h[22:20]≥010b	RW	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
31:3	***Reserved***		RsvdP	No	0-0h

Register 11-24. 5Ch MSI Status (All Ports)

<table>
<tr><th>Bit(s)</th><th>Description</th><th></th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="6">Port interrupt sources are grouped into two categories – Power Management/Hot Plug events and GPIO-generated interrupts.
The quantity of MSI Vectors that are generated is determined by the MSI Control register Multiple Message Capable and Multiple Message Enable fields (All Ports, offset 48h[19:17 and 22:20], respectively):
• If one MSI Vector is enabled (default mode), both interrupt events are combined into a single Vector
• If two MSI Vectors are enabled, the individual vectors indicate:
– Vector[0] Hot Plug/Power Management event and GPIO-generated event
– Vector[1] Reserved
• If four MSI Vectors are enabled (up to two Vectors are used), the individual Vectors indicate:
– Vector[0] Hot Plug/Power Management event
– Vector[1] Reserved
– Vector[2] GPIO-generated event
– Vector[3] Reserved
The bits in this register are self-Clearing, as soon as the PEX 8605 generates the MSI Message. In the event that a particular MSI source is masked in the MSI Mask register (All Ports, offset 58h), Status bits will not be automatically Cleared if Message generation is masked or blocked.
Notes: The offset for this register changes from 5Ch, to 58h, when the MSI Control register MSI 64-Bit Address Capable bit (All Ports, offset 48h[23]) is Cleared.
The bits in this register can be masked by their respective MSI Mask register bits (All Ports, offset 58h).</td></tr>
<tr><td rowspan="2">0</td><td>MSI Pending Status for Power Management or Hot Plug Events
MSI pending status for Power Management or Hot Plug event-generated interrupts.</td><td>Offset 48h[22:20]≥010b</td><td>RO</td><td>Yes</td><td>0</td></tr>
<tr><td>MSI Pending Status for Shared Interrupt Sources
MSI pending status for all interrupt sources when the MSI Control register Multiple Message Enable field indicates that the Host has allocated one or two Vectors.</td><td>Offset 48h[22:20]≤001b</td><td>RO</td><td>Yes</td><td>0</td></tr>
<tr><td>1</td><td colspan="2">Reserved</td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td rowspan="2">2</td><td>MSI Pending Status for GPIO-Generated Interrupts</td><td>Offset 48h[19:17]≥010b and Offset 48h[22:20]≥010b</td><td>RO</td><td>Yes</td><td>0</td></tr>
<tr><td>Reserved</td><td>Offset 48h[22:20]≤001b</td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>31:3</td><td colspan="2">Reserved</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
</table>

11.9 PCI Express Capability Registers (Offsets 68h – A0h)

This section details the PCI Express Capability registers. Hot Plug Capability, Command, Status, and Events are included in these registers. Table 11-9 defines the register map.

Table 11-9. PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability		Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability				6Ch
Device Status		Device Control		70h
Link Capability				74h
Link Status		Link Control		78h
Reserved (Port 0) Slot Capability (Downstream)				7Ch
Reserved (Port 0)				80h
Slot Status (Downstream)		Slot Control (Downstream)		
Reserved				84h – 88h
Device Capability 2				8Ch
Device Status 2 ***(Reserved)***		Device Control 2		90h
Reserved				94h
Link Status 2		Link Control 2		98h
Reserved				9Ch – A0h

Register 11-25. 68h List and Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
PCI Express Capability List					
7:0	**Capability ID** Program to 10h, as required by the *PCI Express Base r2.1*.		RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.		RO	Yes	A4h
PCI Express Capability					
19:16	**Capability Version** The Ports program this field to 2h, as required by the *PCI Express Base r2.1*.		RO	Yes	2h
23:20	**Device/Port Type** Set at reset, as required by the *PCI Express Base r2.1*.	Port 0	RO	Yes	5h
		Downstream	RO	Yes	6h
24	**Slot Implemented** 0 = Disables or connects to Port 0	Port 0	RsvdP	No	0
	0 = Disables or connects to an integrated component 1 = Indicates that the downstream Port connects to a slot, as opposed to being connected to an integrated component or being disabled ***Note:*** *The PEX 8605 serial EEPROM register Initialization capability and/or and/or I^2C can be used to Clear this bit, indicating that the corresponding PEX 8605 downstream Port connects to an integrated component or is disabled.*	Downstream	RO	Yes	1
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.		RO	Yes	00_000b
31:30	***Reserved***		RsvdP	No	00b

Register 11-26. 6Ch Device Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
2:0	**Maximum Payload Size Supported** 000b = Ports support a 128-byte maximum Payload 001b = Ports support a 256-byte maximum Payload No other encodings are supported.		RO	Yes	001b
4:3	**Phantom Functions Supported** ***Not supported***		RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = ***Reserved***		RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** ***Not supported*** Because the PEX 8605 is a switch and not an endpoint, the PEX 8605 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency** ***Not supported*** Because the PEX 8605 is a switch and not an endpoint, the PEX 8605 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
14:12	***Reserved***, as required by the *PCI Express Base r2.1*.		RsvdP	No	000b
15	**Role-Based Error Reporting**		RO	Yes	1
17:16	***Reserved***		RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For Port 0, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	Port 0	RO	Yes	00h
	Not valid	Downstream	RsvdP	No	00h
27:26	**Captured Slot Power Limit Scale** For Port 0, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	Port 0	RO	Yes	00b
	Not valid	Downstream	RsvdP	No	00b
31:28	***Reserved***		RsvdP	No	0h

Register 11-27. 70h Device Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Device Control				
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the Port to report Correctable errors	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the Port to report Non-Fatal errors	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the Port to report Fatal errors	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the Port to report UR errors	RW	Yes	0
4	**Enable Relaxed Ordering** 0 = Disables Relaxed Ordering on the Port 1 = Enables Relaxed Ordering on the Port	RW	Yes	1
7:5	**Maximum Payload Size** Software can change this field to configure the Ports to support other Payload Sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (All Ports, offset 6Ch[2:0]). 000b = Port supports a 128-byte maximum Payload 001b = Port supports a 256-byte maximum Payload No other encodings are supported.	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** 0 = Disables auxiliary power 1 = Enables auxiliary power	RWS	Yes	0
11	**Enable No Snoop** 0 = Disables the No Snoop feature on the Port 1 = Enables the No Snoop feature on the Port	RW	Yes	1
14:12	**Max Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.1*.	RsvdP	No	0

Register 11-27. 70h Device Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Status			
16	**Correctable Error Detected** Set when the Port detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state. 0 = Port did not detect a Correctable error 1 = Port detected a Correctable error	RW1C	Yes	0
17	**Non-Fatal Error Detected** Set when the Port detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state. 0 = Port did not detect a Non-Fatal error 1 = Port detected a Non-Fatal error	RW1C	Yes	0
18	**Fatal Error Detected** Set when the Port detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state. 0 = Port did not detect a Fatal error 1 = Port detected a Fatal error	RW1C	Yes	0
19	**Unsupported Request Detected** Set when the Port detects a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state. 0 = Port did not detect a UR 1 = Port detected a UR	RW1C	Yes	0
20	**AUX Power Detected** 1 = Auxiliary power is detected on the Port	ROS	Yes	1
21	**Transactions Pending** ***Not supported*** Cleared, as required by the *PCI Express Base r2.1*.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 11-28. 74h Link Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
3:0	**Supported Link Speeds** Indicates the Port's supported Link speed. 0010b = 5.0 and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.		RO	Yes	0010b
9:4	**Maximum Link Width** The PEX 8605 maximum Link width is x2 = 00_0010b. Valid widths are x1 or x2. Actual maximum Link width is defined by the STRAP_PORTCFG input. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 (Port 0 only) All other encodings are ***not supported***.		ROS	No	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 00b = ***Reserved*** 01b = L0s Link PM state entry is supported 10b = L1 ASPM is supported 11b = L0s and L1 Link PM states are supported		RO	Yes	11b

Register 11-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Advanced N_FTS** register *Advertised N_FTS* field (Port 0, offset B84h[7:0]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Port's L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = Port's L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.		RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Port's L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = Port's L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.		RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management Capable** ***Not supported***		RsvdP	No	0
19	***Reserved*** This bit must be hardwired to 0, for Port 0 and components that do not support this optional capability.	Port 0	RsvdP	No	0
	Surprise Down Error Reporting Capable Must be Set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. If this bit is Cleared, the **Uncorrectable Error Status** register *Surprise Down Error Status* bit (Downstream Ports, offset FB8h[5]) is disabled. ***Note:*** *If this bit is Set and later Cleared at runtime (such as by I²C), it must be Cleared while the Link is up; otherwise, if the Link is down when this bit is Cleared, a subsequent Surprise Down error event is not masked.*	Downstream	RO	Yes	1

Register 11-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
20	***Reserved***	Port 0	RsvdP	No	0
	Data Link Layer Link Active Reporting Capable Valid for downstream Ports only.	Downstream	RO	Yes	1
21	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.1*.	Port 0	RsvdP	No	0
	Link Bandwidth Notification Capability 1 = Indicates support for the Link Bandwidth Notification status and interrupt mechanisms	Downstream	RO	Yes	1
23:22	***Reserved***		RsvdP	No	00b
31:24	**Port Number** The Port Number is defined by the STRAP_PORTCFG input. (Refer also to Table 11-10.) Available Port Numbers are 0, 1, 2, and 3.		ROS	No	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])

Table 11-10. Port Configurations

STRAP_PORTCFG Value	Port 0	Port 1	Port 2	Port 3
(default) 0	x1	x1	x1	x1
(Lanes)	0	1	2	3
1	x2		x1	x1
(Lanes)	0-1		2	3

Register 11-29. 78h Link Status and Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Link Control					
1:0	**Active State Power Management (ASPM)** 00b = Disable[a] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries		RW	Yes	00b
2	***Reserved***		RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB). Cleared, as required by the *PCI Express Base r2.1*.		RO	Yes	0
4	***Not valid***	Port 0	RsvdP	No	0
	Link Disable 1 = Places the Link on the corresponding PEX 8605 downstream Port to the *Disabled* Link Training state	Downstream	RW	Yes	0
5	***Not valid*** Always read as 0.	Port 0	RsvdP	No	0
	Retrain Link For PEX 8605 Ports, always returns a value of 0 when read; however, software is allowed to write this register. Writing 1 to this bit causes the corresponding PEX 8605 downstream Port to initiate retraining of its PCI Express Link.	Downstream	RZ	Yes	0
6	**Common Clock Configuration** 0 = Port and the device at the other end of the Port's PCI Express Link use an asynchronous Reference Clock source 1 = Port and the device at the other end of the Port's PCI Express Link use a common (synchronous) Reference Clock source (constant phase relationship)		RW	Yes	0
7	**Extended Sync** When Set, causes the Port to transmit: • 4,096 FTS Ordered-Sets in the L0s Link PM state, • Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the *Recovery* state.		RW	Yes	0

Register 11-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
8	**Clock Power Management Enable** ***Reserved*** Read and Writable only when the **Link Capability** register *Clock Power Management Capable* bit is Set.		RsvdP	No	0
9	**Hardware-Autonomous Width Disable** ***Reserved***		RsvdP	No	0
10	***Reserved***	Port 0	RsvdP	No	0
	Link Bandwidth Management Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Bandwidth Management Status* bit (Downstream Ports, offset 78h[30]) has been Set	Downstream	RW	Yes	0
11	***Reserved***	Port 0	RsvdP	No	0
	Link Autonomous Bandwidth Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Autonomous Bandwidth Status* bit (Downstream Ports, offset 78h[31]) has been Set	Downstream	RW	Yes	0
15:12	***Reserved***		RsvdP	No	0h
Link Status					
19:16	**Current Link Speed** Indicates the current Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.		RO	No	0001b
25:20	**Negotiated Link Width** Dependent upon the physical Port configuration. Link width is determined by the negotiated value with the attached Lane/Port. 00_0001b = x1 or the Port is in the *DL_Down* state 00_0010b = x2 (Port 0 only) All other encodings are ***not supported***.		RO	No	00_0001b
26	***Reserved***		RsvdP	No	0
27	***Reserved***	Port 0	RsvdP	No	0
	Link Training 1 = Indicates that the corresponding PEX 8605 downstream Port requested Link training, and the Link training is in-progress or about to start	Downstream	RO	No	0

Register 11-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
28	**Slot Clock Configuration** 0 = Indicates that the PEX 8605 uses an independent clock 1 = Indicates that the PEX 8605 uses the same physical Reference Clock that the platform provides on the connector		HwInit	Yes	0
29	***Reserved***	Port 0	RsvdP	No	0
	Data Link Layer Link Active When Set, and the **Link Capability** register *Data Link Layer Link Active Reporting Capable* bit (Downstream Ports, offset 74h[20]) is also Set, indicates the following: • Data Link Layer (DLL) is in the *DL_Active* state • Link is operational • Flow Control (FC) Initialization has successfully completed	Downstream	RO	Yes	0
30	***Reserved***	Port 0	RsvdP	No	0
	Link Bandwidth Management Status Set by hardware to indicate that either of the following has occurred, without the Port transitioning through DL_Down status: • Link retraining has completed following a Write of 1 to the **Link Control** register *Retrain Link* bit (Downstream Ports, offset 78h[5]) • Hardware has changed Link speed or width, to attempt to correct unreliable Link operation, either through an Link Training and Status State Machine (LTSSM) timeout or higher-level process	Downstream	RW1C	Yes	0
31	***Reserved***	Port 0	RsvdP	No	0
	Link Autonomous Bandwidth Status Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.	Downstream	RW1C	Yes	0

a. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Register 11-30. 7Ch Slot Capability (Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**Attention Button Present** ***Not supported***		RsvdP	No	0
1	**Power Controller Present** ***Not supported***		RsvdP	No	0
2	**MRL Sensor Present** ***Not supported***		RsvdP	No	0
3	**Attention Indicator Present** ***Not supported***		RsvdP	No	0
4	**Power Indicator Present** ***Not supported***		RsvdP	No	0
5	***Reserved***	Port 0	RsvdP	No	0
	Hot Plug Surprise 0 = No device in the corresponding PEX 8605 downstream Port (with an I²C I/O Expander) slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8605 downstream Port slot can be removed from the system without prior notification	Downstream	RO	Yes	0
6	***Reserved***	Port 0	RsvdP	No	0
	Hot Plug Capable Set on the Port where HP_PRSNT# is currently assigned. The PEX 8605 reports Hot Plug capability on only one downstream Port. 0 = Corresponding PEX 8605 downstream Port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8605 Transparent downstream Port slot is capable of supporting Hot Plug operations	Downstream	RO	Yes	1
14:7	***Reserved***	Port 0	RsvdP	No	00h
	Slot Power Limit Value The maximum power supplied by the corresponding PEX 8605 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the field [16:15] (*Slot Power Limit Scale*) value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (Downstream Ports, offset 68h[24]) is Set (default). Serial EEPROM and/or I²C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	Downstream	RO	Yes	19h

Register 11-30. 7Ch Slot Capability (Downstream Ports) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Ports</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td rowspan="3">16:15</td><td>Reserved</td><td>Port 0</td><td>RsvdP</td><td>No</td><td>00b</td></tr>
<tr><td>Slot Power Limit Scale
The maximum power supplied by the corresponding PEX 8605 downstream slot is determined by multiplying the value in this field by the field [14:7] (Slot Power Limit Value) value.
This field must be implemented if the PCI Express Capability register Slot Implemented bit (Downstream Ports, offset 68h[24]) is Set (default).
Serial EEPROM and/or I²C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device’s upstream Port Device Capability register Captured Slot Power Limit Value and Captured Slot Power Limit Scale fields.
00b = 1.0x
01b = 0.1x
10b = 0.01x
11b = 0.001x</td><td>Downstream</td><td>RO</td><td>Yes</td><td>00b</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>17</td><td>Electromechanical Interlock Present
Not supported</td><td colspan="3"></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>18</td><td>No Command Completed Support
Reserved</td><td colspan="3"></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td rowspan="5">31:19</td><td>Reserved</td><td>Port 0</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td>Physical Slot Number
Indicates the physical Slot Number attached to this Port.
If the PCI Express Capability register Slot Implemented bit (Downstream Ports, offset 68h[24]) is Set (default), this field must be hardware-initialized to a value that assigns a Slot Number that is unique within the chassis, regardless of the form factor associated with the slot. Must be initialized to 0h for Ports connected to devices that are integrated on the system board.</td><td rowspan="4">Downstream</td><td rowspan="4">RO</td><td rowspan="4">Yes</td><td rowspan="4">0-0h</td></tr>
<tr><td><table><tr><th>Bit(s)</th><th>Description/Function</th></tr><tr><td>22:19</td><td>Port Numbers 1, 2, and 3</td></tr><tr><td>26:23</td><td>Loaded from I²C I/O Expander</td></tr><tr><td>31:27</td><td>Reserved</td></tr></table></td></tr>
</table>

Register 11-31. 80h Slot Status and Control (Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Slot Control					
0	**Attention Button Pressed Enable** ***Not supported/Not implemented***		RsvdP	No	0
1	**Power Fault Detector Enable** ***Not supported***		RsvdP	No	0
2	**MRL Sensor Changed Enable** ***Not supported***		RsvdP	No	0
3	***Not valid***	Port 0	RsvdP	No	0
	Presence Detect Changed Enable A Presence Detect Changed event is triggered by either the SerDes Receiver Detect (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, offset 200h[19:16])). 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 state (**PCI Power Management Status and Control** register *Power State* field (Downstream Ports, offset 44h[1:0]), is Cleared), or with a PME Message if the Port is in the D3hot state (Downstream Ports, offset 44h[1:0], are both Set), for a Presence Detect Changed event on the corresponding PEX 8605 downstream Port	Downstream	RW	Yes	0
4	**Command Completed Interrupt Enable** ***Not supported***		RsvdP	No	0
5	***Reserved***	Port 0	RsvdP	No	0
	Hot Plug Interrupt Enable 0 = Function is disabled 1 = Enables an interrupt on enabled Hot Plug events for the corresponding PEX 8605 downstream Port	Downstream	RW	Yes	0
7:6	**Attention Indicator Control** ***Not supported***		RsvdP	No	00b

Register 11-31. 80h Slot Status and Control (Downstream Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
9:8	**Power Indicator Control** ***Not supported***		RsvdP	No	00b
10	**Power Controller Control** ***Not supported***		RsvdP	No	0
11	**Electromechanical Interlock Control** ***Not supported***		RsvdP	No	0
12	***Not valid***	Port 0	RsvdP	No	0
	Data Link Layer State Changed Enable Enables software notification with an interrupt if the Port is in the D0 state (**PCI Power Management Status and Control** register *Power State* field (Downstream Ports, offset 44h[1:0]), is Cleared), or with a PME Message if the Port is in the D3hot state (the *Power State* field bits are both Set), when the **Link Status** register *Data Link Layer Link Active* bit (Downstream Ports, offset 78h[29]) is changed.	Downstream	RW	Yes	0
15:13	***Reserved***		RsvdP	No	000b
Slot Status					
16	**Attention Button Pressed** ***Not supported***		RsvdP	No	0
17	**Power Fault Detected** ***Not supported***		RsvdP	No	0
18	**MRL Sensor Changed** ***Not supported***		RsvdP	No	0
19	***Reserved***	Port 0	RsvdP	No	0
	Presence Detect Changed A Presence Detect Changed event is triggered by either the SerDes Receiver Detect (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, offset 200h[19:16])). Write 1 to Clear. 1 = Value reported in bit 22 (*Presence Detect State*) changed	Downstream	RW1C	Yes	0

Register 11-31. 80h Slot Status and Control (Downstream Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**Command Completed** ***Not supported***		RsvdP	No	0
21	**MRL Sensor State** ***Not supported***		RsvdP	No	0
22	***Not valid***	Port 0	RsvdP	No	0
	Presence Detect State For downstream Ports that implement slots, indicates the presence of an adapter in the slot, reflected by the logical OR of the corresponding downstream Port's SerDes Receiver Detect (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, offset 200h[19:16])). Hardwired to 1 when the **PCI Express Capability** register *Slot Implemented* bit (Downstream Ports, offset 68h[24]) value is 0. 0 = Slot is empty, or device is not present 1 = Slot is occupied, or device is present	Downstream, Offset 68h[24]=1	RO	No	0
		Downstream, Offset 68h[24]=0	RO	No	1
23	**Electromechanical Interlock Status** ***Not supported***		RsvdP	No	0
24	***Not valid***	Port 0	RsvdP	No	0
	Data Link Layer State Changed In response to a Data Link Layer State Changed event, software must read the **Link Status** register *Data Link Layer Link Active* bit (Downstream Ports, offset 78h[29]), to determine whether the Link is active before initiating Configuration Requests to the device. 1 = Value reported in the **Link Status** register *Data Link Layer Link Active* bit changed	Downstream	RW1C	Yes	0
31:25	***Reserved***		RsvdZ	No	0-0h

Register 11-32. 8Ch Device Capability 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Port 0	RsvdP	No	0
	ARI Forwarding Supported 0 = Alternative Routing-ID Interpretation (ARI) forwarding is not supported 1 = ARI forwarding is supported	Downstream	RO	Yes	1
31:6	***Reserved***		RsvdP	No	0-0h

Register 11-33. 90h Device Status and Control 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Device Control 2					
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Port 0	RsvdP	No	0
	ARI Forwarding Enable 0 = Disabled 1 = Enabled; Downstream Port disables its traditional Device Number field from being forced to 0 when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to extended functions in an ARI device immediately below the Port	Downstream	RW	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Status 2					
31:16	***Reserved***		RsvdP	No	0-0h

Register 11-34. 98h Link Status and Control 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Link Control 2					
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s Link speed is supported All other encodings are ***reserved***.		RWS	Yes	0010b
4	**Enter Compliance**		RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.		RsvdP	No	0
6	***Not valid***	Port 0	RsvdP	Yes	0
	Selectable De-Emphasis Selects the standard de-emphasis level when the Link is operating at 5.0 GT/s. When the Link is operating at 2.5 GT/s, the Setting of this bit has no effect (de-emphasis at 2.5 GT/s is -3.5 dB). 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)	Downstream	HwInit	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
9:7	**Transmit Margin** Intended for debug and compliance testing only.		RWS	Yes	000b
10	**Enter Modified Compliance** Intended for debug and compliance testing only. Valid only for Function 0 of Port 0.	Port 0	RWS	Yes	0
	Reserved	Downstream	RsvdP	No	0
11	**Compliance SOS** 1 = LTSSM must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern		RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* substate, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.		RWS	Yes	0
15:13	***Reserved***		RsvdP	No	000b
Link Status 2					
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)		RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***		RsvdP	No	0-0h

11.10 Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)

This section details the Subsystem ID and Subsystem Vendor ID Capability registers. Table 11-11 defines the register map.

Table 11-11. Subsystem ID and Subsystem Vendor ID Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Reserved	Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID		A8h
Reserved		ACh –	FCh

Register 11-35. A4h Subsystem Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**SSID/SSVID Capability ID** Detects the SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** 00h = This capability is the last capability in the PEX 8605 Port's Capabilities list The PEX 8605 Extended Capabilities list starts at offset 100h.	RO	Yes	00h
31:16	***Reserved***	RsvdP	No	0000h

Register 11-36. A8h Subsystem ID and Subsystem Vendor ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Subsystem Vendor ID** The Vendor ID (All Ports, offset 00h[15:0]) identifies the manufacturer of the PEX 8605, and the Subsystem Vendor ID optionally identifies the board or system vendor. As with the Vendor ID value, the Subsystem Vendor ID value must be a valid PCI-SIG-assigned Vendor ID. The value of this field is usually identical for all PEX 8605 Ports.	RO	Yes	10B5h
31:16	**Subsystem ID** The Device ID (All Ports, offset 00h[31:16]) identifies the PEX 8605, and optionally the Subsystem ID in combination with the Subsystem Vendor ID, uniquely identifies the board or system. The value of this field is usually identical for all PEX 8605 Ports, and is chosen or assigned only by the "owner" of the valid Vendor ID value used for the Subsystem Vendor ID. If the board or system vendor is not a PCI-SIG member, PLX can assign, free of charge, a unique Subsystem ID value, in which case the Subsystem Vendor ID remains the PLX default value, 10B5h.	RO	Yes	8605h

11.11 Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

This section details the Device Serial Number Extended Capability registers. Table 11-12 defines the register map.

Table 11-12. Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h) / Capability Version (1h)	PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Upper DW)		108h
Reserved	10Ch –	134h

Register 11-37. 100h Device Serial Number Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 0003h, as required by the *PCI Express Base r2.1*.	RO	Yes	0003h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.1*.	RO	Yes	1h
31:20	**Next Capability Offset** Program to FB4h, which addresses the **Advanced Error Reporting Extended Capability** structure.	RO	Yes	FB4h

Register 11-38. 104h Serial Number (Lower DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**PCI Express Device Serial Number (1st DW)** Lower half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.1*, all PEX 8605 Ports must contain the same value; therefore, one physical register is shared by all Ports. (Refer to Table 11-3.) The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64™), of which the upper 24 bits are the Company ID value (00_0EDFh) assigned by the IEEE Registration Authority, and the lower 40 bits are the Extension ID assigned by the identified Company (PLX). The most through least significant bytes are contained within the lowest through highest Byte addresses, respectively.	RO	Yes	B5DF_0E00h

Register 11-39. 108h Serial Number (Upper DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**PCI Express Device Serial Number (2nd DW)** Upper half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.1*, all PEX 8605 Ports must contain the same value; therefore, one physical register is shared by all Ports. (Refer to Table 11-3.) The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64), of which the upper 24 bits are the Company ID value (00_0EDFh) assigned by the IEEE Registration Authority, and the lower 40 bits are the Extension ID assigned by the identified Company (PLX). The most through least significant bytes are contained within the lowest through highest Byte addresses, respectively.	RO	Yes	Silicon Revision AA: AA86_0210h Silicon Revision AB: AB86_0210h

11.12 Power Budget Extended Capability Registers (Offsets 138h – 144h)

This section details the Power Budget Extended Capability registers. These registers work differently than the others, especially with respect to serial EEPROM Reads and Writes. *For example*, when writing to Index 5 of the **Power Budget Data** register (All Ports, offset 140h), write 5 into the **Data Select** register *Data Select* field (All Ports, offset 13Ch[7:0]), then write the value into the **Power Budget Data** register. Table 11-13 defines the register map.

Table 11-13. Power Budget Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h) / Capability Version (1h)	PCI Express Extended Capability ID (0004h)	138h
Reserved	Data Select	13Ch
Power Budget Data		140h
Power Budget Capability		144h

Register 11-40. 138h Power Budget Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID** Program to 0004h, as required by the *PCI Express Base r2.1*.	RO	Yes	0004h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.1*.	RO	Yes	1h
31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	RO	Yes	148h

Register 11-41. 13Ch Data Select (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Data Select** Indexes the Power Budget data reported, **Power Budget Data** registers, two per Port, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 0 to 1.	RW	Yes	00h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 11-42. 140h Power Budget Data (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *Two registers per Port can be programmed, through the serial EEPROM, I²C, and/or SMBus. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register Data Select field (All Ports, offset 13Ch[7:0]).*				
7:0	**Base Power** Two registers per Port. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (*Data Scale*) contents, to produce the actual power consumption value.	RO	Yes	00h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	Yes	00b
12:10	**PM Sub-State** 000b = Power Management substate of the operating condition being described	RO	Yes	000b
14:13	**PM State** Power Management state of the operating condition being described. 00b = D0 state 01b = D1 state 10b = D2 state 11b = D3 state	RO	Yes	00b
17:15	**Type** Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	RO	Yes	000b
20:18	**Power Rail** Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	RO	Yes	000b
31:21	***Reserved***	RsvdP	No	0-0h

Register 11-43. 144h Power Budget Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**System Allocated** 1 = Power budget for the device is included within the system power budget	HwInit	Yes	1
31:1	***Reserved***	RsvdP	No	0-0h

11.13 Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

This section details the Virtual Channel Extended Capability registers, which are duplicated for each Port. Table 11-14 defines the register map for one Port.

Table 11-14. Virtual Channel Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (950h or 520h) / Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status ***(Reserved)***	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
Reserved		164h – 1BCh

Register 11-44. 148h Virtual Channel Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.1*.		RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.1*.		RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	Port 0	RO	No	950h
	Next extended capability is the **ACS Extended Capability** structure, offset 520h.	Downstream	RO	No	520h

Register 11-45. 14Ch Port VC Capability 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
2:0	**Extended VC Counter** 000b = PEX 8605 Port supports only one Virtual Channel, VC0 All other encodings are ***reserved***.	RO	Yes	000b
3	***Reserved***	RsvdP	No	0
6:4	**Low-Priority Extended VC Counter** ***Not supported***	RO	Yes	000b
7	***Reserved***	RsvdP	No	0
9:8	**Reference Clock** ***Reserved***	RsvdP	No	00b
11:10	**Port Arbitration Table Entry Size** 00b = Port Arbitration Table entry size is 1 bit All other encodings are ***reserved***.	RO	Yes	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 11-46. 150h Port VC Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**VC Arbitration Capability** Indicates the type of VC arbitration supported by the device for the LPVC (Low-Priority Extended VC) group. 0 = Indicates that the Round-Robin (Hardware-Fixed) Arbitration scheme is not supported 1 = Indicates that the Round-Robin (Hardware-Fixed) Arbitration scheme is supported	RO	Yes	0
31:1	***Reserved***	RsvdP	No	0-0h

Register 11-47. 154h Port VC Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Port VC Control				
0	**Load VC Arbitration Table** ***Not supported*** Reads always return a value of 0.	RsvdP	No	0
3:1	**VC Arbitration Select** Selects the Port's VC arbitration type, as per the supported arbitration type indicated by the **Port VC Capability 2** register *VC Arbitration Capability* bit (All Ports, offset 150h[0]) value. 000b = Bit 0; Non-configurable (Hardware-Fixed) Arbitration All other encodings are ***reserved***.	RW	Yes	000b
15:4	***Reserved***	RsvdP	No	000h
Port VC Status				
16	**VC Arbitration Table Status** ***Reserved***	RsvdP	No	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 11-48. 158h VC0 Resource Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Port Arbitration Capability** Bit 0 = 1 – Non-configurable (Hardware-Fixed) Arbitration All other bits read 0.	RO	No	01h
14:8	***Reserved***	RsvdP	No	0-0h
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, this bit is Cleared.	RsvdP	No	0
22:16	**Maximum Time Slots** ***Reserved***	RsvdP	No	000_0000b
23	***Reserved***	RsvdP	No	0
31:24	**Port Arbitration Table Offset** Offset of the Port Arbitration Table, as the quantity of DQWords from the Base address of the **Virtual Channel Extended Capability** structure. 00h = Non-configurable (Hardware-Fixed) Arbitration All other encodings are ***reserved***.	RO	No	00h

Register 11-49. 15Ch VC0 Resource Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	No	1
7:1		RW	Yes	7Fh
23:8	***Reserved***	RsvdP	No	0000h
26:24	**VC0 ID** Defines the Port's VC0 ID code. 000b = VC0 (default; VC0 is the only/default VC) All other encodings are ***Reserved***.	RO	No	000b
30:27	***Reserved***	RsvdP	No	0h
31	**VC0 Enable** 0 = Not allowed 1 = Enables the Port's only/default VC, VC0	RO	No	1

Register 11-50. 160h VC0 Resource Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** The Port's Arbitration Table is ***not*** implemented; therefore, this bit has no function, and always reads 0.	RO	No	0
17	**VC0 Negotiation Pending** 0 = Port's VC0 negotiation is complete 1 = Port's VC0 initialization is not complete	RO	Yes	1
31:18	***Reserved***	RsvdP	No	0-0h

11.14 Device-Specific Registers (Offsets 1C0h – 444h)

This section details the Device-Specific registers located at offsets 1C0h through 444h. Device-Specific registers are unique to the PEX 8605 and not referenced in the *PCI Express Base r2.1*. Table 11-15 defines the register map.

Other Device-Specific registers are detailed in Section 11.16, "Device-Specific Registers (Offsets 530h – B88h)."

Note: It is recommended that these registers not be changed from their default values.

Table 11-15. Device-Specific Register Map (Offsets 1C0h – 444h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)		1C0h … 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)		200h … 25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)		260h … 26Ch
Factory Test Only/Reserved	270h –	28Ch
Device-Specific Registers – I2C and SMBus Slave Interfaces (Offsets 290h – 2C4h)		290h … 2C4h
Factory Test Only/Reserved	2C8h –	444h

11.14.1 Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)

This section details the Device-Specific Error Checking and Debug registers. Table 11-16 defines the register map.

Table 11-16. Device-Specific Error Checking and Debug Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Factory Test Only	1C0h –	1C4h
ECC Error Check Disable		1C8h
Factory Test Only	1CCh –	1D4h
Clock Enable		1D8h
Reserved	Debug Control	1DCh
Power Management Hot Plug User Configuration		1E0h
Egress Control and Status		1E4h
Bad TLP Counter		1E8h
Bad DLLP Counter		1ECh
Reserved		1F0h
Software Lane Status		1F4h
ACK Transmission Latency Limit		1F8h
Factory Test Only		1FCh

Register 11-51. 1C8h ECC Error Check Disable (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	***Factory Test Only***	RWS	Yes	0h
4	**Enable PEX_INTA# Interrupt Output(s) for Hot Plug Event-Triggered Interrupts** 0 = Hot Plug Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Hot Plug Event Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
5	***Factory Test Only***	RWS	Yes	0
6	**Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts** 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
9:7	***Factory Test Only***	RWS	Yes	000b
10	***Factory Test Only***	RW1CS	Yes	0
31:11	***Reserved***	RsvdP	No	0-0h

Register 11-52. 1D8h Clock Enable (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Ports are automatically enabled, according to the Port configuration defined by the STRAP_PORTCFG input, which can be overridden by programming the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0]). An enabled Port can be selectively disabled, however, by Clearing the Port's *PDA* and *INT Port x Clock Enable* bits in this register. Port 0 must always remain enabled. ***Note:*** *It is not possible to enable more Ports than the maximum specified for the device.*				
0	**PDA Port 0 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
1	**PDA Port 1 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
2	**PDA Port 2 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
3	**PDA Port 3 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
4	**INT Port 0 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
5	**INT Port 1 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
6	**INT Port 2 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
7	**INT Port 3 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])

Register 11-52. 1D8h Clock Enable (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**REFCLK 1 Enable** Used to enable/disable Reference Clock Pair 1, PEX_REFCLK_OUTn1/ PEX_REFCLK_OUTp1. 0 = Disables 1 = Enables	RWS	Yes	1
9	**REFCLK 2 Enable** Used to enable/disable Reference Clock Pair 2, PEX_REFCLK_OUTn2/ PEX_REFCLK_OUTp2. 0 = Disables 1 = Enables	RWS	Yes	1
10	**REFCLK 3 Enable** Used to enable/disable Reference Clock Pair 3, PEX_REFCLK_OUTn3/ PEX_REFCLK_OUTp3. 0 = Disables 1 = Enables	RWS	Yes	1
31:11	***Reserved***	RsvdP	No	0-0h

Register 11-53. 1DCh Debug Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *This register **must** be the first Configuration register programmed by the serial EEPROM, at serial EEPROM locations 4h through 9h, as listed in Table 6-1, "Serial EEPROM Data Format."*				
0	**STRAP_DEBUG_SEL# Pin State** Reflects the logical state of the STRAP_DEBUG_SEL# input. 0 = Selected function is enabled	RO	No	0 (STRAP_DEBUG_SEL#=L) 1 (STRAP_DEBUG_SEL#=H)
1	***Reserved***	RsvdP	No	0
2	**STRAP_PROBE_MODE# Pin State** Reflects the logical state of the STRAP_PROBE_MODE# input. 0 = Selected function is enabled	RO	No	0 (STRAP_PROBE_MODE#=L) 1 (STRAP_PROBE_MODE#=H)
3	***Reserved***	RsvdP	No	0
4	**STRAP_UPCFG_TIMER_EN# Pin State** Reflects the logical state of the STRAP_UPCFG_TIMER_EN# input at reset. This bit's state can be subsequently overwritten by serial EEPROM and/or I^2C. 0 = Selected function is enabled	RO	Yes	0 (STRAP_UPCFG_TIMER_EN#=L) 1 (STRAP_UPCFG_TIMER_EN#=H)
5	**STRAP_SMBUS_EN# Pin State** Reflects the logical state of the STRAP_SMBUS_EN# input. 0 = SMBus Slave interface is enabled for device configuration (SMBus mode is enabled) 1 = SMBus Slave interface is disabled for device configuration (I^2C mode is enabled)	RO	Yes	0 (STRAP_SMBUS_EN#=L) 1 (STRAP_SMBUS_EN#=H)
6	**Force PCI Express Gen 1 (2.5 GT/s) Operation** 0 = PCI Express Links are forced to operate at Gen 1 bit rates 1 = PCI Express Links are allowed to transition to Gen 2 bit rates (5.0 GT/s) ***Note:*** *The value read from this bit is invalid.*	RWS	Yes	1
7	***Factory Test Only***	RWS	Yes	1
11:8	***Reserved***	RsvdP	No	0h
13:12	***Factory Test Only***	RWS	Yes	00b
14	***Factory Test Only***	RWS	Yes	0
15	***Reserved***	RsvdP	No	0

Register 11-53. 1DCh Debug Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Upstream Hot Reset Control** 0 = Reset all logic, except Sticky bits and Device-Specific registers 1 = Reset only the Configuration Space registers of all Ports defined by the *PCI Express Base r2.1* ***Note:*** *Only a Fundamental Reset serial EEPROM load affects this bit.*	RWS	Yes	0
17	**Disable Serial EEPROM Load on Hot Reset** 0 = Enables serial EEPROM load upon Port 0 Hot Reset or *DL_Down* state 1 = Disables serial EEPROM load upon Port 0 Hot Reset or *DL_Down* state	RWS	Yes	0
19:18	***Reserved***	RsvdP	No	00b
20	**Upstream Port DL_Down Reset Propagation Disable** Setting this bit: • Enables Port 0 to ignore a Hot Reset training sequence, • Blocks the PEX 8605 from manifesting an internal reset due to a DL_Down event, and • Prevents the downstream Ports from issuing a Hot Reset to downstream devices when a Hot Reset or DL_Down event occurs on the upstream Link	RWS	Yes	0
21	**Cut-Thru Enable** 0 = Disables Cut-Thru support 1 = Enables Cut-Thru support	RWS	Yes	1
22	**LANE_GOOD*x*#/GPIO*x* Pin Function Select** 0 = LANE_GOOD[3:0]# pins function as GPIO[3:0] pins 1 = LANE_GOOD[3:0]# pins function as Lane Good status for Lanes [3-0], respectively	RWS	Yes	1
23	***Factory Test Only***	RWS	Yes	0
31:24	***Reserved***	RsvdP	No	00h

Register 11-54. 1E0h Power Management Hot Plug User Configuration (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *When programming this register, always* • *Preserve the default states of bits [5:3]* • *Write 1 to bit 6*					
0	**L0s Entry Idle Counter** Traffic idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs		RW	Yes	0
1	**ASPM L1 Disable**		RW	Yes	0
2	***Not enabled*** Functionality associated with this bit is enabled only on the downstream Ports.	Port 0	W1RZ	Yes	0
	HPC PME Turn-Off Enable 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	Downstream	W1RZ	Yes	0
3	***Factory Test Only*** ***Note:*** *When programming this register, always preserve the state of this bit.*		W1RZ	Yes	0
4	***Factory Test Only*** ***Note:*** *When programming this register, always preserve the state of this bit.*		RWS	Yes	1
5	***Factory Test Only*** ***Note:*** *When programming this register, always preserve the state of this bit.*		RW	Yes	0
6	***Factory Test Only*** ***Note:*** *When programming this register, always write 1 to this bit.*		RWS	Yes	1
7	**Disable PCI Express PM L1 Entry** 1 = Disables L1 Link PM state entry on Port 0, when Port 0 is placed into the D3hot state		RW	Yes	0
8	**DLLP Timeout Link Retrain Disable** Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 µs. 0 = Enables Link retraining when no DLLPs are received for more than 256 µs (default) 1 = DLLP Timeout is disabled		RW	Yes	0
9	***Factory Test Only***		RW	Yes	0
10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met		RW	Yes	0
11	***Factory Test Only***		RW	Yes	0

Register 11-54. 1E0h Power Management Hot Plug User Configuration (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
12	***Reserved***		RsvdP	No	0
15:13	***Factory Test Only***		RO	Yes	000b
17:16	**Present Pin Assignment Register** Selects the downstream Port to which the HP_PRSNT# input (Hot Plug capability) is assigned. 00b = ***Reserved*** 01b = Port 1 (default when STRAP_PORTCFG=0) 10b = Port 2 (default when STRAP_PORTCFG=1) 11b = Port 3 (serial EEPROM Write only)	Port 0	RO	Yes	PCFG
	Reserved	Downstream	RsvdP	No	00b
18	**HPC In-Band Presence Detect Disable** 1 = Disable Hot Plug Controller In-Band Presence Detect		RW	Yes	0
31:19	***Reserved***		RsvdP	No	0-0h

Register 11-55. 1E4h Egress Control and Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	***Reserved***	RW	Yes	00b
8:2	***Factory Test Only***	RW	Yes	20h
9	**Vendor-Specific Type 0 UR** 0 = Do not generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state 1 = Generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state	RW	Yes	0
10	**Egress Credit Timeout Enable** 0 = Egress Credit Timeout mechanism is disabled. 1 = Egress Credit Timeout mechanism is enabled. The timeout period is selected in bit 11 (*Egress Credit Timeout Value*). Status is reflected in bit 16 (*VC0 Egress Credit Timeout Status*). If the Egress Credit Timer is enabled and expires (due to lack of Flow Control credits from the connected device), the Port brings down its Link. This event generates a Surprise Down Uncorrectable error, for downstream Ports. For Port 0 Egress Credit Timeout, the connected upstream device detects the Surprise Down event.	RW	Yes	0
11	**Egress Credit Timeout Value** 0 = 384 to 512 ms 1 = 896 to 1,024 ms	RW	Yes	0
12	**Egress Credit Timeout Short** 0 = No Function 1 = Dependent upon the bit 11 (*Egress Credit Timeout Value*) value: • When bit 11 is Cleared, then timeout is 768 µs to 1 ms • When bit 11 is Set, then timeout is 1.792 ms to 2 ms	RW	Yes	0
15:13	***Reserved***	RsvdP	No	000b
16	**VC0 Egress Credit Timeout Status** 0 = No timeout 1 = Timeout	RW1C	No	0
18:17	**VC0 Egress Credit Timeout Type** 00b = Posted 01b = Non-Posted 10b = Completion 11b = ***Reserved***	RO	Yes	00b
31:19	***Reserved***	RsvdP	No	0-0h

Register 11-56. 1E8h Bad TLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad TLP Counter** Counts the quantity of TLPs received with bad Link Cyclic Redundancy Check (LCRC), or quantity of TLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 11-57. 1ECh Bad DLLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad DLLP Counter** Counts the quantity of DLLPs received with bad LCRC, or quantity of DLLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 11-58. 1F4h Software Lane Status (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Lane 0 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
1	**Lane 1 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
2	**Lane 2 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
3	**Lane 3 Up Status** 0 = Lane 3 is down 1 = Lane 3 is up	RO	No	1
31:4	***Reserved***	RsvdP	No	0000_000h

Register 11-59. 1F8h ACK Transmission Latency Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The value of this register should be valid after Link negotiation.				
11:0	**ACK Transmission Latency Limit** Acknowledge Control Packet (ACK) Transmission Latency Limit. The value of this field changes based upon Negotiated Link Width (All Ports, offset 78h[25:20]) encoding, after the Link is up. x1 Link width = FFh (STRAP_PORTCFG=L) x2 Link width = D9h (Port 0 only), (STRAP_PORTCFG=H)	RWS	Yes	Defined by STRAP_PORTCFG input state
15:12	***Reserved***	RsvdP	No	0h
23:16	**Upper 8 Bits of the Replay Timer Limit** If the serial EEPROM is not present, the value of this register changes based upon the negotiated Link width after the Link is up. The value in this register is a multiplier of the default internal timer values that are compliant to the *PCI Express Base r2.1*. These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	***Reserved***	RsvdP	No	00h
31	**ACK Transmission Latency Timer Status** Indicates the written status of field [11:0] (*ACK Transmission Latency Limit*). After the register is written, either by software and/or serial EEPROM, this bit is Set, and Cleared only by a Fundamental Reset.	RO	No	0

11.14.2 Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)

This section details the Device-Specific Physical Layer (PHY) registers. Table 11-17 defines the register map.

Another Device-Specific PHY register is detailed in Section 11.16.7, "Device-Specific Registers – Physical Layer (Offsets B80h – B88h)."

Table 11-17. Device-Specific PHY Register Map (Offsets 200h – 25Ch) (Port 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Physical Layer Receiver Detect Status	Physical Layer Electrical Idle for Compliance Mask	200h
Physical Layer Receiver Not Detected Mask	Physical Layer Electrical Idle Detect Mask	204h
Factory Test Only		208h – 20Ch
Physical Layer User Test Pattern, Bytes 0 through 3		210h
Physical Layer User Test Pattern, Bytes 4 through 7		214h
Physical Layer User Test Pattern, Bytes 8 through 11		218h
Physical Layer User Test Pattern, Bytes 12 through 15		21Ch
Physical Layer Command and Status		220h
Physical Layer Function Control		224h
Physical Layer Test		228h
Factory Test Only		22Ch
Reserved	Physical Layer Port Command	230h
SKIP Ordered-Set Interval, Port Control		234h
SerDes Diagnostic Data		238h
Reserved		23Ch – 244h
Port Receiver Error Counters		248h
Reserved	Target Link Width	24Ch
Factory Test Only		250h
Physical Layer Additional Status		254h
PRBS Control/Status		258h
Factory Test Only		25Ch

Register 11-60. 200h Physical Layer Receiver Detect Status/Electrical Idle for Compliance Mask (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register is used for specifying whether the Lanes detected a Receiver during an LTSSM *Detect* state, but never detected an exit from Electrical Idle. When multiple bits are Set, and they correspond to Lanes that both belong to Port 0, either Lane can cause entry into the LTSSM *Polling.Compliance* substate.				
Physical Layer Electrical Idle for Compliance Mask				
This register allows masking that specifies which Lanes must never exit Electrical Idle, for entry to the LTSSM *Polling.Compliance* substate to occur.				
0	**Electrical Idle on SerDes 0 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* substate cannot be entered, due to the Electrical Idle condition. 1 = Lane 0 must have detected a Receiver during the LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* substate, to cause entry to the *Polling.Compliance* substate	RWS	Yes	1
1	**Electrical Idle on SerDes 1 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* substate cannot be entered, due to the Electrical Idle condition. 1 = Lane 1 must have detected a Receiver during the LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* substate, to cause entry to the *Polling.Compliance* substate	RWS	Yes	1
2	**Electrical Idle on SerDes 2 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* substate cannot be entered, due to the Electrical Idle condition. 1 = Lane 2 must have detected a Receiver during the LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* substate, to cause entry to the *Polling.Compliance* substate	RWS	Yes	1
3	**Electrical Idle on SerDes 3 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* substate cannot be entered, due to the Electrical Idle condition. 1 = Lane 3 must have detected a Receiver during the LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* substate, to cause entry to the *Polling.Compliance* substate	RWS	Yes	1
15:4	***Reserved***	RsvdP	No	000h

Register 11-60. 200h Physical Layer Receiver Detect Status/Electrical Idle for Compliance Mask (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Physical Layer Receiver Detect Status				
This register returns the Receiver's LTSSM *Detect* state status for all Lanes.				
16	**Receiver Detected on Lane 0** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 0.	RO	No	Set by SerDes
17	**Receiver Detected on Lane 1** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 1.	RO	No	Set by SerDes
18	**Receiver Detected on Lane 2** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 2.	RO	No	Set by SerDes
19	**Receiver Detected on Lane 3** Returns the Receiver's LTSSM *Detect* state status, and reads back as 1 when a Receiver is detected on Lane 3.	RO	No	Set by SerDes
31:20	***Reserved***	RsvdP	No	000h

Register 11-61. 204h Physical Layer Electrical Idle Detect/Receiver Detect Mask (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register is used to mask Electrical Idle Detect and Receiver functions for debug purposes. It can also be used to mask SerDes problems with these circuits. ***Note:*** *Masking Electrical Idle detect does not affect the inferred Electrical Idle detection.* ***Use the SerDes x Mask Electrical Idle Detect bits with care.***				
Physical Layer Electrical Idle Detect Mask				
Never Detect Electrical Idle mask. This register allows masking of the Electrical Idle Detect function, on a per-SerDes basis. When the bits in this register are Set, the Lane's *Electrical Idle* condition flag does not assert, regardless of the actual presence of Electrical Idle. Masking Electrical Idle detect does not affect the inferred Electrical Idle detection.				
0	**SerDes 0 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for SerDes 0. 1 = Analog Electrical Idle detection is disabled for SerDes 0. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the **Physical Layer Function Control** register *Port 0 Electrical Idle Inference Disable* bit (Port 0, offset 224h[24]) is Cleared.	RWS	Yes	0
1	**SerDes 1 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for SerDes 1. 1 = Analog Electrical Idle detection is disabled for SerDes 1. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the Port's **Physical Layer Function Control** register *Port x Electrical Idle Inference Disable* bit(s) (Port 0, offset 224h[25:24]) associated with SerDes 1 is Cleared.	RWS	Yes	0
2	**SerDes 2 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for SerDes 2. 1 = Analog Electrical Idle detection is disabled for SerDes 2. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the **Physical Layer Function Control** register *Port 2 Electrical Idle Inference Disable* bit (Port 0, offset 224h[26]) is Cleared.	RWS	Yes	0
3	**SerDes 3 Mask Electrical Idle Detect** 0 = Analog Electrical Idle detection is enabled for SerDes 3. 1 = Analog Electrical Idle detection is disabled for SerDes 3. Electrical Idle entrance inference, however, can be enabled by one or more available methods only if this bit is Set, and the **Physical Layer Function Control** register *Port 3 Electrical Idle Inference Disable* bit (Port 0, offset 224h[27]) is Cleared.	RWS	Yes	0
15:4	***Reserved***	RsvdP	No	000h

Register 11-61. 204h Physical Layer Electrical Idle Detect/Receiver Detect Mask (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Physical Layer Receiver Not Detected Mask				
Always Detect a Receiver mask. This register allows masking of the Receiver Detect function, on a per-SerDes basis. When the bits in this register are Set, the PHY functions as if the Lane detected a Receiver, regardless of the actual presence of a Receiver.				
16	**SerDes 0 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for SerDes 0. Lane 0 will always detect a Receiver. The PHY functions as if a Receiver was detected on Lane 0, regardless of the actual presence of a Receiver.	RWS	Yes	0
17	**SerDes 1 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for SerDes 1. Lane 1 will always detect a Receiver. The PHY functions as if a Receiver was detected on Lane 1, regardless of the actual presence of a Receiver.	RWS	Yes	0
18	**SerDes 2 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for SerDes 2. Lane 2 will always detect a Receiver. The PHY functions as if a Receiver was detected on Lane 2, regardless of the actual presence of a Receiver.	RWS	Yes	0
19	**SerDes 3 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for SerDes 3. Lane 3 will always detect a Receiver. The PHY functions as if a Receiver was detected on Lane 3, regardless of the actual presence of a Receiver.	RWS	Yes	0
31:20	***Reserved***	RsvdP	No	000h

Register 11-62. 210h Physical Layer User Test Pattern, Bytes 0 through 3 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 12.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 0 of the UTP. This is the first byte transferred.	RW	Yes	00h
15:8	Byte 1 of the UTP.	RW	Yes	00h
23:16	Byte 2 of the UTP.	RW	Yes	00h
31:24	Byte 3 of the UTP.	RW	Yes	00h

Register 11-63. 214h Physical Layer User Test Pattern, Bytes 4 through 7 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 12.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 4 of the UTP. This is the fifth byte transferred.	RW	Yes	00h
15:8	Byte 5 of the UTP.	RW	Yes	00h
23:16	Byte 6 of the UTP.	RW	Yes	00h
31:24	Byte 7 of the UTP.	RW	Yes	00h

Register 11-64. 218h Physical Layer User Test Pattern, Bytes 8 through 11 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 12.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 8 of the UTP. This is the ninth byte transferred.	RW	Yes	00h
15:8	Byte 9 of the UTP.	RW	Yes	00h
23:16	Byte 10 of the UTP.	RW	Yes	00h
31:24	Byte 11 of the UTP.	RW	Yes	00h

Register 11-65. 21Ch Physical Layer User Test Pattern, Bytes 12 through 15 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 12.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 12 of the UTP. This is the thirteenth byte transferred.	RW	Yes	00h
15:8	Byte 13 of the UTP.	RW	Yes	00h
23:16	Byte 14 of the UTP.	RW	Yes	00h
31:24	Byte 15 of the UTP.	RW	Yes	00h

Register 11-66. 220h Physical Layer Command and Status (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides various Command and Status bits for Physical Layer operation.				
2:0	**Number of Ports Available** Returns the quantity of enabled Ports, based upon the selected Port configuration.	RO	No	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
3	**Upstream Cross-Link Enable** 0 = Disables upstream cross-link, Port 0 cannot be connected to another upstream Port 1 = Enables upstream cross-link, Port 0 can be connected to another upstream Port	RWS	Yes	1
4	**Downstream Cross-Link Enable** 0 = Disables downstream cross-link, downstream Ports cannot be connected to other downstream Ports 1 = Enables downstream cross-link, downstream Ports can be connected to other downstream Ports	RWS	Yes	1
5	**Lane Reversal Disable** 1 = Disables Lane reversal on Port 0 only, when Port 0 is configured as a x2 Link width	RWS	Yes	0
6	***Reserved***	RsvdP	No	0
7	***Factory Test Only***	RWS	Yes	0
15:8	***Reserved***	RsvdP	No	00h
31:16	**User Test Pattern K-Code Flag** The corresponding UTP byte is transmitted as a kcode. ***Notice: Use caution when turning on k-characters, because the transmit logic does not examine illegal codes for validity. Also, sequences of control codes that can be detected as legal SKIP Ordered-Sets in the middle of the data pattern can confuse the Receive data checking logic. Therefore, it is recommended to not turn on k-characters when testing with a UTP.***	RWS	Yes	0000h

Register 11-67. 224h Physical Layer Function Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register contains Port-based PHY Safety bits.				
3:0	**Configuration Fail Counter[3:0]** Specifies the quantity of times that the *Configuration* state must fail, before the Port toggles its *Gen 2 Feature Disable* flag. Writing 0000b to this field disables this Gen 1 compatibility function. The initial value of this field is determined by the STRAP_UPCFG_TIMER_EN# input state. If the input is Low when reset de-asserts, the initial value of this field is 0001b; otherwise, the initial value is 0000b.	RWS	Yes	0000b (STRAP_UPCFG_TIMER_EN#=H) 0001b (STRAP_UPCFG_TIMER_EN#=L)
6:4	**Electrical Idle Inference Time Select[2:0]** Selects the amount of time to wait until no SKIP Ordered-Sets are detected, for Electrical Idle to be inferred. Does not affect Electrical Idle inference during the *Recovery.Speed* substate. 000b = 4 µs 001b = 6 µs 010b = 8 µs 011b = 16 µs 100b = 32 µs 101b = 64 µs 110b = 128 µs (default) 111b = 256 µs	RWS	Yes	110b
7	***Reserved***	RsvdP	No	0

Register 11-67. 224h Physical Layer Function Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
9:8	**Recovery.Speed Electrical Idle Inference Time Divider Select[1:0]** Selects the amount of time that no TS1 nor TS2 Ordered-Sets are detected during the *Recovery.Speed* substate, for Electrical Idle to be inferred. (Refer to the *PCI Express Base r2.1*, Section 4.2.4.3, for the specific Unit Interval (UI) values.) 00b = *PCI Express Base r2.1* UI 01b = *PCI Express Base r2.1* UI/2 10b = *PCI Express Base r2.1* UI/4 11b = *PCI Express Base r2.1* UI/8	RWS	Yes	00b
11:10	**Detect.Quiet Wait Time Select Code[1:0]** Selects the amount of time to wait during the *Detect.Quiet* substate, before starting the Receiver Detect operation, when a break from Electrical Idle is detected. If Electrical Idle is detected on all Lanes, the wait time is 12 ms. 00b = 0 ms 01b = 4 ms 10b = 8 ms 11b = 12 ms	RWS	Yes	00b
15:12	**Unconditional SerDes Quad Disable**	RWS	Yes	0h
16	**Inferred Electrical Idle Inference Exit Type** Selects the method used to detect exit from Electrical Idle, after Electrical Idle has been inferred. 0 = **Fast Method** – Type 0 Exit mode is used, which uses conventional analog Electrical Idle Exit Detection circuitry 1 = **Slow Method** – Type 1 Exit mode is used, which uses the Symbol Framer Detection Time Select Code and Inferred Electrical Idle Exit Time Select Code Timers (fields [21:20 and 19:18], respectively)	RWS	Yes	0
17	***Reserved***	RsvdP	No	0

Register 11-67. 224h Physical Layer Function Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:18	**Inferred Electrical Idle Exit Time Select Code** When Electrical Idle has been inferred and the Electrical Idle Inference Exit Type is 1 (bit 16 is Set), this field selects the amount of time that the SerDes Receive Data path remains disabled. 00b = 2 µs 01b = 4 µs 10b = 8 µs 11b = 16 µs	RWS	Yes	00b
21:20	**Symbol Framer Detection Time Select Code** When Electrical Idle has been inferred and the Electrical Idle Inference Exit Type is 1 (bit 16 is Set), this field selects the amount of time that the symbol framer is allowed to obtain symbol lock. 00b = 128 ns 01b = 256 ns 10b = 512 ns 11b = 1 µs	RWS	Yes	00b
23:22	***Reserved***	RsvdP	No	00b

Register 11-67. 224h Physical Layer Function Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Port 0 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes x Mask Electrical Idle Detect* bit(s) (Port 0, offset 204h[1:0]) are Set, for the SerDes associated with Port 0. 1 = Overall Electrical Idle inference logic is disabled on Port 0. Electrical Idle inference during the *Recovery.Speed* substate is not affected and will continue to operate.	RWS	Yes	0
25	**Port 1 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes 1 Mask Electrical Idle Detect* bit (Port 0, offset 204h[1]) is Set. 1 = Overall Electrical Idle inference logic is disabled on Port 1. Electrical Idle inference during the *Recovery.Speed* substate is not affected and will continue to operate.	RWS	Yes	0
26	**Port 2 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes 2 Mask Electrical Idle Detect* bit (Port 0, offset 204h[2]) is Set. 1 = Overall Electrical Idle inference logic is disabled on Port 2. Electrical Idle inference during the *Recovery.Speed* substate is not affected and will continue to operate.	RWS	Yes	0
27	**Port 3 Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes 3 Mask Electrical Idle Detect* bit (Port 0, offset 204h[3]) is Set. 1 = Overall Electrical Idle inference logic is disabled on Port 3. Electrical Idle inference during the *Recovery.Speed* substate is not affected and will continue to operate.	RWS	Yes	0

Register 11-67. 224h Physical Layer Function Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**Port 0 Electrical Idle Inference on EIOS Receipt Enable** 0 = Electrical Idle inference is enabled upon Electrical Idle Ordered-Set (EIOS) receipt, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes x Mask Electrical Idle Detect* bit(s) (Port 0, offset 204h[1:0]) are Set, for the SerDes associated with Port 0 1 = Electrical Idle will be inferred as soon as an EIOS is received on any Lane associated with Port 0	RWS	Yes	0
29	**Port 1 Electrical Idle Inference on EIOS Receipt Enable** 0 = Electrical Idle inference is enabled upon EIOS receipt, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes 1 Mask Electrical Idle Detect* bit (Port 0, offset 204h[1]) is Set. 1 = Electrical Idle will be inferred as soon as an EIOS is received on Lane 1	RWS	Yes	0
30	**Port 2 Electrical Idle Inference on EIOS Receipt Enable** 0 = Electrical Idle inference is enabled upon EIOS receipt, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes 2 Mask Electrical Idle Detect* bit (Port 0, offset 204h[2]) is Set 1 = Electrical Idle will be inferred as soon as an EIOS is received on Lane 2	RWS	Yes	0
31	**Port 3 Electrical Idle Inference on EIOS Receipt Enable** 0 = Electrical Idle inference is enabled upon EIOS receipt, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes 3 Mask Electrical Idle Detect* bit (Port 0, offset 204h[3]) is Set 1 = Electrical Idle will be inferred as soon as an EIOS is received on Lane 3	RWS	Yes	0

Register 11-68. 228h Physical Layer Test (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides controls to enable various PHY test modes.				
0	**Port 0 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port 0 LTSSM are reduced to microsecond scale	RWS	Yes	0
1	**Port 1 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port 1 LTSSM are reduced to microsecond scale	RWS	Yes	0
2	**Port 2 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port 2 LTSSM are reduced to microsecond scale	RWS	Yes	0
3	**Port 3 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port 3 LTSSM are reduced to microsecond scale	RWS	Yes	0
4	**SKIP Timer Test Mode Enable**	RW	Yes	0
5	**Ignore Compliance Receive TCB**	RWS	Yes	0
6	**Analog Loopback Enable** 0 = PEX 8605 enters Digital Loopback Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loopback* bit exclusively Set in the TS1 Training Control symbol. The PEX 8605 then loops back data through the Elastic buffer, 8b/10b decoder, and 8b/10b encoder. 1 = Loopback point of all Ports is located before the Elastic buffer. This means that data recovered from the Serial data in the recovered Receive Clock domain is re-serialized, then re-transmitted in that same recovered clock domain. This allows the Loopback Master to transmit and receive a user test pattern (UTP) in an asynchronous clocking system. It is also the **required** mode for re-transmitting a PRBS pattern back to the Loopback Master. Overrides the Lane's Parallel "Digital" Loopback Setting bit(s) [27:24] (*Lane x Parallel Loopback Path Enable*).	RWS	Yes	0
7	***Reserved***	RsvdP	No	0
8	***Factory Test Only***	RW	Yes	0
9	***Factory Test Only***	RO	No	0
10	***Factory Test Only***	RW1C	Yes	0
11	***Reserved***	RsvdP	No	0

Register 11-68. 228h Physical Layer Test (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:12	***Factory Test Only***	RO	No	0h
19:16	***Factory Test Only***	RWS	Yes	0h
20	**Lane 0 Serial Loopback Path Enable** 0 = Disabled 1 = Lane 0 enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
21	**Lane 1 Serial Loopback Path Enable** 0 = Disabled 1 = Lane 1 enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
22	**Lane 2 Serial Loopback Path Enable** 0 = Disabled 1 = Lane 2 enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
23	**Lane 3 Serial Loopback Path Enable** 0 = Disabled 1 = Lane 3 enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0

Register 11-68. 228h Physical Layer Test (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Lane 0 Parallel Loopback Path Enable** It is recommended that Port 0 be placed into a *Port Disable* state, by Setting the **Port Control** register *Disable Port 0* bit (Port 0, offset 234h[16]), followed by a *Port Quiet* state, by Setting the *Port 0 Quiet* bit (Port 0, offset 234h[20]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for this Lane 1 = Lane manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active substate, as a Loopback Slave.*	RW	Yes	0
25	**Lane 1 Parallel Loopback Path Enable** It is recommended that the Port associated with this Lane (Port 0 or Port 1, as appropriate) be placed into a *Port Disable* state, by Setting the Port's **Port Control** register *Disable Port x* bit(s) (Port 0, offset 234h[17:16]), followed by a *Port Quiet* state, by Setting the Port's *Port x Quiet* bit (Port 0, offset 234h[21:20]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for this Lane 1 = Lane manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active substate, as a Loopback Slave.*	RW	Yes	0
26	**Lane 2 Parallel Loopback Path Enable** It is recommended that Port 2 be placed into a *Port Disable* state, by Setting the **Port Control** register *Disable Port 2* bit (Port 0, offset 234h[18]), followed by a *Port Quiet* state, by Setting the *Port 2 Quiet* bit (Port 0, offset 234h[22]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for this Lane 1 = Lane manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active substate, as a Loopback Slave.*	RW	Yes	0
27	**Lane 3 Parallel Loopback Path Enable** It is recommended that Port 3 be placed into a *Port Disable* state, by Setting the **Port Control** register *Disable Port 3* bit (Port 0, offset 234h[19]), followed by a *Port Quiet* state, by Setting the *Port 3 Quiet* bit (Port 0, offset 234h[23]), before Setting this bit. 0 = Parallel "Digital" *Loopback* (Slave) path is disabled for Lane 3 1 = Lane 3 manually enables the Parallel "Digital" *Loopback* (Slave) path, regardless of the LTSSM state ***Note:*** *This path is automatically enabled when the LTSSM enters the Loopback.Active substate, as a Loopback Slave.*	RW	Yes	0

Register 11-68. 228h Physical Layer Test (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**SerDes 0 User Test Pattern Enable** 0 = Disables user test pattern transmission 1 = Enables user test pattern transmission ***Notes: This bit and the SerDes Test register SerDes 0 BIST Generator/ Checker Enable bit (Port 0, offset B88h[16]) are mutually exclusive functions and must not be enabled together for SerDes 0. The logical result of both bits ANDed with one another must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port Control register Port 0 Quiet bit (Port 0, offset 234h[20]) is Set.***	RW	Yes	0
29	**SerDes 1 User Test Pattern Enable** 0 = Disables user test pattern transmission 1 = Enables user test pattern transmission ***Notes: This bit and the SerDes Test register SerDes 1 BIST Generator/ Checker Enable bit (Port 0, offset B88h[17]) are mutually exclusive functions and must not be enabled together for SerDes 1. The logical result of both bits ANDed with one another must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port's Port Control register Port x Quiet bit (Port 0, offset 234h[21:20]) is Set.***	RW	Yes	0
30	**SerDes 2 User Test Pattern Enable** 0 = Disables user test pattern transmission 1 = Enables user test pattern transmission ***Notes: This bit and the SerDes Test register SerDes 2 BIST Generator/ Checker Enable bit (Port 0, offset B88h[18]) are mutually exclusive functions and must not be enabled together for SerDes 2. The logical result of both bits ANDed with one another must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port Control register Port 2 Quiet bit (Port 0, offset 234h[22]) is Set.***	RW	Yes	0
31	**SerDes 3 User Test Pattern Enable** 0 = Disables user test pattern transmission 1 = Enables user test pattern transmission ***Notes: This bit and the SerDes Test register SerDes 3 BIST Generator/ Checker Enable bit (Port 0, offset B88h[19]) are mutually exclusive functions and must not be enabled together for SerDes 3. The logical result of both bits ANDed with one another must be 0.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port Control register Port 3 Quiet bit (Port 0, offset 234h[23]) is Set.***	RW	Yes	0

Register 11-69. 230h Physical Layer Port Command (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Port Loopback, Scrambler Disable, and Compliance Receive commands, and Ready as Loopback Master status.				
0	**Port 0 Loopback Command** 0 = Port 0 is not enabled to go to the *Loopback* Master state. 1 = Port 0 attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
1	**Port 0 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on either Lane associated with Port 0, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* substate. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port 0's scrambler is enabled 1 = Port 0's scrambler is disabled	RWS	Yes	0
2	**Port 0 Compliance Receive Command** 0 = When Port 0 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* substate 1 = When Port 0 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* substate	RWS	Yes	0
3	**Port 0 Ready as Loopback Master** Link Training and Status State Machine (LTSSM) established Loopback as a Master for Port 0. 0 = Port 0 is not in Loopback Master mode. 1 = Indicates that Port 0 has successfully transitioned to the *Loopback.Active* substate as a Loopback Master. The LTSSM remains in this substate, until bit 0 (*Port 0 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8605 exits the *Loopback.Active* substate.	RO	No	0

Register 11-69. 230h Physical Layer Port Command (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**Port 1 Loopback Command** 0 = Port 1 is not enabled to go to the *Loopback* Master state. 1 = Port 1 attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
5	**Port 1 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on Lane 1, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* substate. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port 1's scrambler is enabled 1 = Port 1's scrambler is disabled	RWS	Yes	0
6	**Port 1 Compliance Receive Command** 0 = When Port 1 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* substate 1 = When Port 1 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* substate	RWS	Yes	0
7	**Port 1 Ready as Loopback Master** LTSSM established Loopback as a Master for Port 1. 0 = Port 1 is not in Loopback Master mode. 1 = Indicates that Port 1 has successfully transitioned to the *Loopback.Active* substate as a Loopback Master. The LTSSM remains in this substate, until bit 4 (*Port 1 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8605 exits the *Loopback.Active* substate.	RO	No	0

Register 11-69. 230h Physical Layer Port Command (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Port 2 Loopback Command** 0 = Port 2 is not enabled to go to the *Loopback* Master state. 1 = Port 2 attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
9	**Port 2 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on Lane 2, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* substate. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port 2's scrambler is enabled 1 = Port 2's scrambler is disabled	RWS	Yes	0
10	**Port 2 Compliance Receive Command** 0 = When Port 2 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* substate 1 = When Port 2 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* substate	RWS	Yes	0
11	**Port 2 Ready as Loopback Master** LTSSM established Loopback as a Master for Port 2. 0 = Port 2 is not in Loopback Master mode. 1 = Indicates that Port 2 has successfully transitioned to the *Loopback.Active* substate as a Loopback Master. The LTSSM remains in this substate, until bit 8 (*Port 2 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8605 exits the *Loopback.Active* substate.	RO	No	0

Register 11-69. 230h Physical Layer Port Command (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
12	**Port 3 Loopback Command** 0 = Port 3 is not enabled to go to the *Loopback* Master state. 1 = Port 3 attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
13	**Port 3 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on Lane 3, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* substate. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Port 3's scrambler is enabled 1 = Port 3's scrambler is disabled	RWS	Yes	0
14	**Port 3 Compliance Receive Command** 0 = When Port 3 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* substate 1 = When Port 3 transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* substate	RWS	Yes	0
15	**Port 3 Ready as Loopback Master** LTSSM established Loopback as a Master for Port 3. 0 = Port 3 is not in Loopback Master mode. 1 = Indicates that Port 3 has successfully transitioned to the *Loopback.Active* substate as a Loopback Master. The LTSSM remains in this substate, until bit 12 (*Port 3 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8605 exits the *Loopback.Active* substate.	RO	No	0
31:16	***Reserved***	RsvdP	No	0000h

Register 11-70. 234h SKIP Ordered-Set Interval, Port Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The upper 16 bits of this register (also referred to as the ***Port Control*** *register*) are used to disable or enable the LTSSM within individual Ports. The bits are intended to be used in lieu of placing the Port into the *Loopback.Active* substate as a Loopback Master. These bits enable the test patterns to be transmitted, with or without a device attached at the far end. Recommended usage is as follows: **1.** Set the Port's *Disable Port x* and *Port x Quiet* bits. • Setting the Port's *Disable Port x* bit forces the Port into the *Detect.Quiet* substate. If no device is attached, it is not necessary to Set the Port's *Disable Port x* bit. • If 5.0 GT/s is needed, also Set the Port's *Test Pattern x Rate* bit. **2.** If Set, Clear the Port's *Disable Port x* bit. **3.** Load the UTP registers and enable UTP transmission, or just enable PRBS transmission.				
11:0	**SKIP Ordered-Set Interval** Specifies the SKIP Ordered-Set interval (in symbol times). When a value of 000h is written, SKIP Ordered-Set transmission is disabled. 000h = Disables SKIP Ordered-Set transmission 49Ch = Minimum interval (1,180 symbol times) 602h = Maximum interval (1,538 symbol times) ***Note:*** *A high value (such as FFFh) can cause the Link to fail.*	RWS	Yes	49Ch
15:12	***Reserved***	RsvdP	No	0h

Register 11-70. 234h SKIP Ordered-Set Interval, Port Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Disable Port 0** 0 = Enables Link Training operation on Port 0. 1 = LTSSM remains in the *Detect.Quiet* substate on Port 0, if it is currently in, or returns to, that substate. Unconditionally disables Port 0. This is different from the Link Training and Status State Machine (LTSSM) *Disabled* state, in that Port 0 does not attempt to enter this state. If Port 0 is idle, it ceases attempting to detect a Receiver. If Port 0 is up, it immediately returns to the *Detect.Quiet* substate and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 0 remains disabled until this bit is Cleared. While Port 0 is disabled, the SerDes that belong to Port 0 is (are) placed into the P1 SerDes Power state.	RWS	Yes	0
17	**Disable Port 1** 0 = Enables Link Training operation on Port 1. 1 = LTSSM remains in the *Detect.Quiet* substate on Port 1, if it is currently in, or returns to, that substate. Unconditionally disables Port 1. This is different from the LTSSM *Disabled* state, in that Port 1 does not attempt to enter this state. If Port 1 is idle, it ceases attempting to detect a Receiver. If Port 1 is up, it immediately returns to the *Detect.Quiet* substate and remains there. No EIOS is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 1 remains disabled until this bit is Cleared. While Port 1 is disabled, SerDes 1 is placed into the P1 SerDes Power state.	RWS	Yes	0
18	**Disable Port 2** 0 = Enables Link Training operation on Port 2. 1 = LTSSM remains in the *Detect.Quiet* substate on Port 2, if it is currently in, or returns to, that substate. Unconditionally disables Port 2. This is different from the LTSSM *Disabled* state, in that Port 2 does not attempt to enter this state. If Port 2 is idle, it ceases attempting to detect a Receiver. If Port 2 is up, it immediately returns to the *Detect.Quiet* substate and remains there. No EIOS is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 2 remains disabled until this bit is Cleared. While Port 2 is disabled, SerDes 2 is placed into the P1 SerDes Power state.	RWS	Yes	0
19	**Disable Port 3** 0 = Enables Link Training operation on Port 3. 1 = LTSSM remains in the *Detect.Quiet* substate on Port 3, if it is currently in, or returns to, that substate. Unconditionally disables Port 3. This is different from the LTSSM *Disabled* state, in that Port 3 does not attempt to enter this state. If Port 3 is idle, it ceases attempting to detect a Receiver. If Port 3 is up, it immediately returns to the *Detect.Quiet* substate and remains there. No EIOS is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. Port 3 remains disabled until this bit is Cleared. While Port 3 is disabled, SerDes 3 is placed into the P1 SerDes Power state.	RWS	Yes	0

Register 11-70. 234h SKIP Ordered-Set Interval, Port Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**Port 0 Quiet** Once in the *Detect.Quiet* substate, Receiver termination is enabled and the Transmitters are placed into the P0 SerDes Power state. Port 0 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* substate. 0 = LTSSM is allowed to exit the *Detect.Quiet* substate in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* substate on Port 0 if it is currently in, or returns to, that substate ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active substate as a Loopback Master.*	RWS	Yes	0
21	**Port 1 Quiet** Once in the *Detect.Quiet* substate, Receiver termination is enabled and the Transmitters are placed into the P0 SerDes Power state. Port 1 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* substate. 0 = LTSSM is allowed to exit the *Detect.Quiet* substate in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* substate on Port 1 if it is currently in, or returns to, that substate ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active substate as a Loopback Master.*	RWS	Yes	0
22	**Port 2 Quiet** Once in the *Detect.Quiet* substate, Receiver termination is enabled and the Transmitters are placed into the P0 SerDes Power state. Port 2 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* substate. 0 = LTSSM is allowed to exit the *Detect.Quiet* substate in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* substate on Port 2 if it is currently in, or returns to, that substate ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active substate as a Loopback Master.*	RWS	Yes	0
23	**Port 3 Quiet** Once in the *Detect.Quiet* substate, Receiver termination is enabled and the Transmitters are placed into the P0 SerDes Power state. Port 3 can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* substate. 0 = LTSSM is allowed to exit the *Detect.Quiet* substate in a normal manner (no effect on the LTSSM) 1 = LTSSM remains in the *Detect.Quiet* substate on Port 3 if it is currently in, or returns to, that substate ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active substate as a Loopback Master.*	RWS	Yes	0

Register 11-70. 234h SKIP Ordered-Set Interval, Port Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Port 0 Test Pattern *x* Rate** Port 0 transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 20 (*Port 0 Quiet*) is also Set (manual rate selection is enabled only when the *Quiet* bit is Set). 0 = Test pattern is transmitted at the Gen 1 Link rate (2.5 GT/s) 1 = Test pattern is transmitted at the Gen 2 Link (5.0 GT/s)	RWS	Yes	0
25	**Port 1 Test Pattern *x* Rate** Port 1 transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 21 (*Port 1 Quiet*) is also Set (manual rate selection is enabled only when the *Quiet* bit is Set). 0 = Test pattern is transmitted at a rate of 2.5 GT/s 1 = Test pattern is transmitted at a rate of 5.0 GT/s	RWS	Yes	0
26	**Port 2 Test Pattern *x* Rate** Port 2 transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 22 (*Port 2 Quiet*) is also Set (manual rate selection is enabled only when the *Quiet* bit is Set). 0 = Test pattern is transmitted at a rate of 2.5 GT/s 1 = Test pattern is transmitted at a rate of 5.0 GT/s	RWS	Yes	0
27	**Port 3 Test Pattern *x* Rate** Port 3 transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if bit 23 (*Port 3 Quiet*) is also Set (manual rate selection is enabled only when the *Quiet* bit is Set). 0 = Test pattern is transmitted at a rate of 2.5 GT/s 1 = Test pattern is transmitted at a rate of 5.0 GT/s	RWS	Yes	0

Register 11-70. 234h SKIP Ordered-Set Interval, Port Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
28	**Port 0 Bypass UTP Alignment Pattern** Must be Set if the following conditions exist: • Port 0 is a Loopback Master transmitting the User Test Pattern, and • Loopback Slave is in a different clock domain 0 = UTP Transmitter continuously transmits the alignment pattern until any UTP checker in either SerDes associated with Port 0 indicates that it has received the alignment pattern. The UTP Transmitter will then transmit one sync pattern, followed by the programmed user test pattern. 1 = Programmed user test pattern will be preceded by one alignment pattern (D3.2 D18.2 D13.2 D17.1) and one sync pattern (K28.5 D3.2 D18.2 D13.2).	RWS	Yes	0
29	**Port 1 Bypass UTP Alignment Pattern** Must be Set if the following conditions exist: • Port 1 is a Loopback Master transmitting the User Test Pattern, and • Loopback Slave is in a different clock domain 0 = UTP Transmitter continuously transmits the alignment pattern until any UTP checker in SerDes 1 indicates that it has received the alignment pattern. The UTP Transmitter will then transmit one sync pattern, followed by the programmed user test pattern. 1 = Programmed user test pattern will be preceded by one alignment pattern (D3.2 D18.2 D13.2 D17.1) and one sync pattern (K28.5 D3.2 D18.2 D13.2).	RWS	Yes	0
30	**Port 2 Bypass UTP Alignment Pattern** Must be Set if the following conditions exist: • Port 2 is a Loopback Master transmitting the User Test Pattern, and • Loopback Slave is in a different clock domain 0 = UTP Transmitter continuously transmits the alignment pattern until any UTP checker in SerDes 2 indicates that it has received the alignment pattern. The UTP Transmitter will then transmit one sync pattern, followed by the programmed user test pattern. 1 = Programmed user test pattern will be preceded by one alignment pattern (D3.2 D18.2 D13.2 D17.1) and one sync pattern (K28.5 D3.2 D18.2 D13.2).	RWS	Yes	0
31	**Port 3 Bypass UTP Alignment Pattern** Must be Set if the following conditions exist: • Port 3 is a Loopback Master transmitting the User Test Pattern, and • Loopback Slave is in a different clock domain 0 = UTP Transmitter continuously transmits the alignment pattern until any UTP checker in SerDes 3 indicates that it has received the alignment pattern. The UTP Transmitter will then transmit one sync pattern, followed by the programmed user test pattern. 1 = Programmed user test pattern will be preceded by one alignment pattern (D3.2 D18.2 D13.2 D17.1) and one sync pattern (K28.5 D3.2 D18.2 D13.2).	RWS	Yes	0

Register 11-71. 238h SerDes Diagnostic Data (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register is used to retrieve Diagnostic Test results for SerDes[0-3].				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the quantity of errors detected by the UTP (bit 30 is Cleared) or PRBS (bit 30 is Set) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing one or more of the **Physical Layer Test** register *SerDes x User Test Pattern Enable* bit(s) (Port 0, offset 228h[31:28]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing one or more of the **SerDes Test** register *SerDes x BIST Generator/Checker Enable* bit(s) (Port 0, offset B88h[19:16]).	RO	No	00h
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes[0-3] to which the diagnostic data in this register pertains. Status selection code for the fields representing RO bits [30, 23:0] of this register. The binary code represents a status selection for one of the Lanes. The test results for physical device Lanes [0-3] are selected with corresponding binary codes from 0-3, respectively. ***Note:*** *To obtain diagnostic data on all SerDes, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RsvdP	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 11-72. 248h Port Receiver Error Counters (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Port 0 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by Port 0. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
15:8	**Port 1 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by Port 1. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
23:16	**Port 2 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by Port 2. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
31:24	**Port 3 Receiver Error Counter** When read, returns the quantity of Receiver errors detected by Port 3. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h

Register 11-73. 24Ch Target Link Width (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register contains Controls and Status for Link width re-configuration on x2-capable Port 0, in the PHY partition. Link width fields in this register are provided, to enable software to direct Link width Up/Down configuration. The Link width field is loaded with the Target Link width, which should not exceed the originally negotiated Link width, and afterward, the **Link Control** register *Retrain Link* bit (All Ports, offset 78h[5]) is Set. If the Target Link width is not equal to the current Link width, the LTSSM transitions from *Recovery* to *Configuration*, then re-negotiates the Link width.				
1:0	**Port 0 Target Link Width** Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, *such as* to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Target Link width for Port 0, to support Link Width Upconfiguration. The initial value of this field is the Port's Negotiated Link Width (All Ports, offset 78h[25:20]).	RWS	No	Defined by STRAP_PORTCFG input state, or programmed by serial EEPROM value for the **Port Configuration** register *Port Configuration* bit (Port 0, offset 574h[0])
6:2	***Reserved***	RsvdP	No	0-0h
7	**Port 0 Upconfigure Capability Received** Set during Link training, if Port 0 received an Upconfigure Capability notification from the connected device. 0 = Device connected to the Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's **Link Control** register *Retrain Link* bit (All Ports, offset 78h[5]).	RO	No	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 11-74. 254h Physical Layer Additional Status (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Port 0 Loopback Master Entry Failed** 1 = Indicates that Port 0 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the **Physical Layer Port Command** register Port 0 Ready as Loopback Master bit (Port 0, offset 230h[3]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
1	**Port 1 Loopback Master Entry Failed** 1 = Indicates that Port 1 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the **Physical Layer Port Command** register Port 1 Ready as Loopback Master bit (Port 0, offset 230h[7]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
2	**Port 2 Loopback Master Entry Failed** 1 = Indicates that Port 2 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the **Physical Layer Port Command** register Port 2 Ready as Loopback Master bit (Port 0, offset 230h[11]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
3	**Port 3 Loopback Master Entry Failed** 1 = Indicates that Port 3 failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the **Physical Layer Port Command** register Port 3 Ready as Loopback Master bit (Port 0, offset 230h[15]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
7:4	**PhyStatus** PIPE interface PhyStatus.	RO	No	PCFG
14:8	**Received Modified Compliance Error Counter**	RO	No	0-0h
15	**Received Modified Compliance Pattern Lock**	RO	No	0

Register 11-74. 254h Physical Layer Additional Status (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
16	**Port 0 External Loopback Enable** 1 = Allows Port 0 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port 0 Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
17	**Port 1 External Loopback Enable** 1 = Allows Port 1 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port 1 Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
18	**Port 2 External Loopback Enable** 1 = Allows Port 2 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port 2 Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
19	**Port 3 External Loopback Enable** 1 = Allows Port 3 to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when the Port 3 Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
23:20	**2nd Receiver Detect Disable**	RWS	Yes	0h
25:24	**Received Modified Compliance Lane Select**	RW	Yes	00b
27:26	***Reserved***	RsvdP	No	00b
28	***Factory Test Only***	RW	Yes	0
31:29	***Reserved***	RsvdP	No	000b

Register 11-75. 258h PRBS Control/Status (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**PRBS Pattern Sync Status Device Lane 0** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that either Lane associated with Port 0's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
1	**PRBS Pattern Sync Status Device Lane 1** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that Lane 1's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
2	**PRBS Pattern Sync Status Device Lane 2** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that Lane 2's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
3	**PRBS Pattern Sync Status Device Lane 3** Diagnoses broken Loopback wiring, because no errors can be detected and counted until pattern sync is detected. Sync achieved is Active-High. 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that Lane 3's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
15:4	***Reserved***	RsvdP	No	000h
16	**PRBS Pattern Invert Enable** 1 = Causes the PRBS pattern generator to output the one's complement of the PRBS7 sequence	RW	Yes	0
31:17	***Reserved***	RsvdP	No	0-0h

11.14.3 Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)

This section details the Device-Specific Serial EEPROM registers. Table 11-18 defines the register map.

Table 11-18. Device-Specific Serial EEPROM Register Map (Port 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Status Data from Serial EEPROM	Serial EEPROM Status / Serial EEPROM Control	260h
Serial EEPROM Buffer		264h
Serial EEPROM Clock Frequency		268h
Reserved	Serial EEPROM 3rd Address Byte	26Ch

Register 11-76. 260h Serial EEPROM Status and Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Serial EEPROM Control				
12:0	**EepBlkAddr** Serial EEPROM Block Address for 32 KB.	RW	Yes	000h
15:13	**EepCmd[2:0]** Commands to the Serial EEPROM Controller. 000b = ***Reserved*** 001b = Data from bits [31:24] (**Status Data from Serial EEPROM** register) is written to the serial EEPROM's internal **Status** register 010b = Write four bytes of data from the EepBuf into the memory location pointed to by field [12:0] (*EepBlkAddr*) 011b = Read four bytes of data from the memory location pointed to by field [12:0] (*EepBlkAddr*) into the EepBuf 100b = Reset Write Enable latch 101b = Data from the serial EEPROM's internal **Status** register is written to bits [31:24] (**Status Data from Serial EEPROM** register) 110b = Set Write Enable latch 111b = ***Reserved*** ***Note:*** *For value of 001b, only bits [31, 27:26] can be written into the serial EEPROM's internal **Status** register.*	RW	Yes	000b

Register 11-76. 260h Serial EEPROM Status and Control (Port 0) *(Cont.)*

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Serial EEPROM Status					
17:16	**EepPrsnt[1:0]** Serial EEPROM Present status. 00b = Not present 01b = Serial EEPROM is present – Validation Signature is verified 10b = ***Reserved*** 11b = Serial EEPROM is present – Validation Signature is not verified		HwInit	No	00b
18	**EepCmdStatus** Serial EEPROM Command status. 0 = Serial EEPROM Command is complete 1 = Serial EEPROM Command is not complete		RO	No	0
19	***Reserved***		RsvdP	No	0
20	**EepBlkAddr Upper Bit** Serial EEPROM Block Address upper bit 13. Extends the serial EEPROM to 64 KB.		RW	Yes	0
21	**EepAddrWidth Override** 0 = Field [23:22] (*EepAddrWidth*) is RO 1 = Field [23:22] (*EepAddrWidth*) is software-writable		RW	Yes	0
23:22	**EepAddrWidth** Serial EEPROM Address width. If the addressing width cannot be determined, 00b is returned. A non-zero value is reported only if the validation signature (5Ah) is successfully read from the first serial EEPROM location. This field is usually HwInit; however, it is RW if bit 21 (*EepAddrWidth Override*) is Set. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes	Bit 21 = 0	HwInit	No	00b
		Bit 21 = 1	RW	No	00b

Register 11-76. 260h Serial EEPROM Status and Control (Port 0) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">Status Data from Serial EEPROM[a]</td></tr>
<tr><td>24</td><td>EepRdy
Serial EEPROM RDY#.
0 = Serial EEPROM is ready to transmit data
1 = Write cycle is in progress</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>25</td><td>EepWen
Serial EEPROM Write enable.
0 = Serial EEPROM Write is disabled
1 = Serial EEPROM Write is enabled</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>27:26</td><td>EepBp[1:0]
Serial EEPROM Block-Write Protect bits. Block Protection options protect the top ¼, top ½, or the entire serial EEPROM. PEX 8605 Configuration data is stored in the lower addresses; therefore, when using Block Protection, the entire serial EEPROM should be protected with BP[1:0]=11b.
<table>
<tr><th rowspan="2">BP[1:0]</th><th rowspan="2">Level</th><th colspan="4">Array Addresses Protected, by Device Size</th></tr>
<tr><th>8 KB</th><th>16 KB</th><th>32 KB</th><th>64 KB</th></tr>
<tr><td>00b</td><td>0</td><td>None</td><td>None</td><td>None</td><td>None</td></tr>
<tr><td>01b</td><td>1 (top ¼)</td><td>1800h – 1FFFh</td><td>3000h – 3FFFh</td><td>6000h – 7FFFh</td><td>–</td></tr>
<tr><td>10b</td><td>2 (top ½)</td><td>1000h – 1FFFh</td><td>2000h – 3FFFh</td><td>4000h – 7FFFh</td><td>–</td></tr>
<tr><td>11b</td><td>3 (All)</td><td>0000h – 1FFFh</td><td>0000h – 3FFFh</td><td>0000h – 7FFFh</td><td>–</td></tr>
</table></td><td>RW</td><td>Yes</td><td>00b</td></tr>
</table>

Register 11-76. 260h Serial EEPROM Status and Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
30:28	**EepWrStatus** Serial EEPROM Write status. Value is 000b when the serial EEPROM is not in an internal Write cycle. ***Note:*** *The definition of this field varies among serial EEPROM manufacturers. Reads of the serial EEPROM's internal* ***Status*** *register can return a value of 000b or 111b, depending upon the serial EEPROM that is used.*	RO	No	000b
31	**EepWpen** Serial EEPROM Write Protect enable. Overrides the internal serial EEPROM Write Protect WP# input and enables/disables Writes to the **Serial EEPROM Status** register (bits [23:16] of this register): • When WP#=H or this bit is Cleared, and bit 25 (*EepWen*) is Set, the **Serial EEPROM Status** register is writable • When WP#=L and this bit is Set, or bit 25 (*EepWen*) is Cleared, the **Serial EEPROM Status** register is write-protected ***Notes:*** *If the internal serial EEPROM Write Protect WP# input is Low, after software Sets the EepWen bit to write-protect the* ***Serial EEPROM Status*** *register, the EepWen value cannot be Cleared, nor can the EepBp[1:0] field be Cleared to disable Block Protection, until the WP# input is High.* *This bit is* ***not*** *implemented in certain serial EEPROMs. Refer to the serial EEPROM manufacturer's data sheet.*	RW	Yes	0

a. Within the serial EEPROM's internal ***Status*** *register, only bits [31, 27:26] can be written.*

Register 11-77. 264h Serial EEPROM Buffer (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**EepBuf** Serial EEPROM RW buffer. Read/Write command to the **Serial EEPROM Control** register (Port 0, offset 260h) results in a 4-byte Read/Write to/from the serial EEPROM device.	RW	Yes	0000_0000h

Register 11-78. 268h Serial EEPROM Clock Frequency (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
2:0	**EepFreq[2:0]** Serial EEPROM clock (EE_SK) frequency control. 000b = 1 MHz (default) 001b = 1.98 MHz 010b = 5 MHz 011b = 9.62 MHz 100b = 12.5 MHz 101b = 15.6 MHz 110b = 17.86 MHz 111b = ***Reserved***	RW	Yes	000b
7:3	***Reserved***	RsvdP	No	0-0h
10:8	**EepCsStHld[2:0]** CS to SCLK setup and hold timing to the serial EEPROM, between EE_CS# active and EE_SK active, and between EE_SK inactive and EE_CS# inactive. Time increases in ½ EE_SK Clock cycle increments, from a minimum of ½, to a maximum of 4. 000b = ½ EE_SK clocks (minimum time) 001b = 1 EE_SK clock (+ ½ clock) 010b = 1 ½ EE_SK clocks 011b = 2 EE_SK clocks 100b = 2 ½ EE_SK clocks 101b = 3 EE_SK clocks 110b = 3 ½ EE_SK clocks 111b = 4 EE_SK clocks (maximum time)	RW	Yes	010b
31:11	***Reserved***	RsvdP	No	0-0h

Register 11-79. 26Ch Serial EEPROM 3rd Address Byte (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Serial EEPROM 3rd Address Byte**	RW	Yes	00h
31:8	***Reserved***	RsvdP	No	0000_00h

11.14.4 Device-Specific Registers – I2C and SMBus Slave Interfaces (Offsets 290h – 2C4h)

This section details the Device-Specific I2C Slave and SMBus Interface registers. Table 11-19 defines the register map.

The I2C and SMBus Slave Interfaces are described, in detail, in Chapter 7, "I2C/SMBus Slave Interface Operation."

Table 11-19. Device-Specific I2C and SMBus Slave Interfaces Register Map (Port 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Factory Test Only		290h
I2C Configuration		294h
Factory Test Only	298h –	2A8h
SMBus Configuration		2ACh
Factory Test Only/Reserved	2B0h –	2C4h

Register 11-80. 294h I²C Configuration (Port 0)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th colspan="2">Default</th></tr>
<tr><td>2:0</td><td rowspan="2">Slave Address
Bits [6:0] comprise the I²C Slave/SMBus Device address, 5Fh. The value is determined by bits [2:0] (which reflect the I2C_ADDR[2:0] input states, and default to 111b, by virtue of weak internal pull-up resistors), combined with the value of bits [6:3] (which default to 1011b).
When I2C_ADDR2=H, Address Resolution Protocol (ARP) is disabled and bit 2 defaults to a value of 1.
The following table lists the pin and register bit values associated with the I²C Slave and SMBus Device addresses. Other values can be programmed as well, by serial EEPROM or Memory Write.
<table>
<tr><th>I2C_ADDR [2:0] Values</th><th>Offset 294h[2:0] Value</th><th>Offset 294h[6:3] Value</th><th>I²C Slave Address</th><th>SMBus Device Address</th></tr>
<tr><td>000</td><td>000b</td><td rowspan="8">1011b</td><td>1011_000b</td><td>ARP</td></tr>
<tr><td>001</td><td>001b</td><td>1011_001b</td><td>ARP</td></tr>
<tr><td>010</td><td>010b</td><td>1011_010b</td><td>ARP</td></tr>
<tr><td>011</td><td>011b</td><td>1011_011b</td><td>ARP</td></tr>
<tr><td>100</td><td>100b</td><td>1011_100b</td><td>1011_100b</td></tr>
<tr><td>101</td><td>101b</td><td>1011_101b</td><td>1011_101b</td></tr>
<tr><td>110</td><td>110b</td><td>1011_110b</td><td>1011_110b</td></tr>
<tr><td>111</td><td>111b</td><td>1011_111b</td><td>1011_111b</td></tr>
</table>
Note: The I²C Slave/SMBus Device address must not be changed by an I²C/SMBus Write command.</td><td>HwInit</td><td>Yes</td><td>111b</td><td rowspan="2">5Fh</td></tr>
<tr><td>6:3</td><td>RWS</td><td>Yes</td><td>1011b</td></tr>
<tr><td>9:7</td><td>Reserved</td><td>RsvdP</td><td>No</td><td colspan="2">000b</td></tr>
<tr><td>10</td><td>Factory Test Only</td><td>RWS</td><td>Yes</td><td colspan="2">0</td></tr>
<tr><td>31:11</td><td>Reserved</td><td>RsvdP</td><td>No</td><td colspan="2">0000_00h</td></tr>
</table>

Register 11-81. 2ACh SMBus Configuration (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default
0	**SMBus Enable** Initially loaded from the STRAP_SMBUS_EN# input state. The value can later be changed by serial EEPROM and/or Configuration Space register Read Write. 0 = Disables SMBus for device configuration (I2C mode is enabled) 1 = Enables SMBus for device configuration (SMBus mode is enabled)	RWS	Yes	0 (STRAP_SMBUS_EN#=H) 1 (STRAP_SMBUS_EN#=L)
7:1	**SMBus Device Address** Defined by the Address Resolution Protocol (ARP) Master, if ARP is enabled. Defaults to 38h if ARP is disabled (I2C_ADDR2=H), with Address bit [1:0] values loaded from the I2C_ADDR[1:0] inputs.	RWS	Yes	00h (I2C_ADDR2=L) 38h (I2C_ADDR2=H)
8	**ARP Disable** 0 = Device under test is able to respond to ARP commands 1 = Device under test is unable to respond to ARP commands	RWS	Yes	0 (I2C_ADDR2=L) 1 (I2C_ADDR2=H)
9	**PEC Check Disable** 0 = Enable PEC checking on all packets 1 = Disables Packet Error Checks (PECs) checking on all packets; packets with the wrong PECs are accepted	RWS	Yes	0
10	**AV Flag** *Address Valid* (*AV*) flag. Set, by default, when ARP is disabled (I2C_ADDR2=H).	RWS	Yes	0 (I2C_ADDR2=L) 1 (I2C_ADDR2=H)
11	**AR Flag** *Address Resolved* (*AR*) flag.	RWS	Yes	0
13:12	**UDID Address Type** Unique Device Identifier (UDID) Address type. 00b = I2C_ADDR2=H (ARP is disabled) 10b = I2C_ADDR2=L (ARP is enabled) All other encodings are ***reserved***.	RWS	Yes	00b (I2C_ADDR2=H) 10b (I2C_ADDR2=L)
14	**UDID PEC Support** 1 = Sets the *PEC Support* bit in the UDID	RWS	Yes	1
15	**SMBus Parameter Re-Load** Set this bit if bits [10, 8, or 7:1] (*AV Flag*, *ARP Disable*, or *SMBus Device Address*, respectively) are changed after a serial EEPROM load. Effective only when bit 28 (*SMBus Command In-Progress*) is Cleared.	ROS	No	0

Register 11-81. 2ACh SMBus Configuration (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
23:16	**UDID Vendor-Specific ID** Sets the MSB of the UDID Vendor-Specific ID. Bits [23:20] of this field are programmed by the I2C_ADDR[1:0] inputs. The four combinations provide the following ID values: 00b = 7000_0000h 01b = B000_0000h 10b = D000_0000h 11b = E000_0000h	RWS	Yes	Defined by I2C_ADDR[1:0] input states
26:24	**UDID Version** UDID version defined for the *SMBus v2.0*.	RWS	Yes	001b
27	***Factory Test Only***	RWS	Yes	0
28	**SMBus Command In-Progress** 0 = SMBus state machine is idle 1 = SMBus state machine is active (not idle)	ROS	No	0
29	**PEC Check Failed** 0 = PEC check successfully completed when receiving a packet 1 = PEC check failed when receiving a packet	RW1CS	No	0
30	**Unsupported SMBus Command** 0 = Command received from SMBus is a supported command 1 = Command received from SMBus is an unsupported command	RW1CS	No	0
31	***Factory Test Only***	RW1CS	No	0

11.15 ACS Extended Capability Registers (Offsets 520h – 52Ch)

This section details the ACS Extended Capability registers. Table 11-20 defines the register map.

Table 11-20. ACS Extended Capability Register Map (Downstream Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved (Port 0)			520h
Next Capability Offset (950h) (Downstream)	Capability Version (1h) (Downstream)	PCI Express Extended Capability ID (000Dh) (Downstream)	
Reserved (Port 0)			524h
ACS Control (Downstream)		ACS Capability (Downstream)	
Reserved (Port 0)			528h
Reserved (Downstream)		Egress Control Vector (Downstream)	
Reserved			52Ch

Register 11-82. 520h ACS Extended Capability Header (Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *Because this register is implemented as one physical register common to all Ports, Port 0's register (which is* ***reserved****) has the same value as the downstream Ports' registers. However, in Port 0, the ACS Extended Capability is excluded from the Linked List of PCI Express Extended Capabilities; therefore, Port 0's register is effectively hidden from system software, and the non-zero value has no significant consequence.*					
15:0	***Reserved***	Port 0	RsvdP	No	0000h
	PCI Express Extended Capability ID	Downstream	RO	Yes	000Dh
19:16	***Reserved***	Port 0	RsvdP	No	0h
	Capability Version	Downstream	RO	Yes	1h
31:20	***Reserved***	Port 0	RsvdP	No	000h
	Next Capability Offset Program to 950h, which addresses the **Vendor-Specific Extended Capability 2** structure.	Downstream	RO	Yes	950h

Register 11-83. 524h ACS Control and Capability (Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Capability					
0	***Reserved***	Port 0	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Port 0	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Port 0	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Port 0	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Port 0	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Port 0	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress control.	Downstream	RO	Yes	1
6	***Reserved***	Port 0	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
10:8	***Reserved***	Port 0	RsvdP	No	0
	Egress Control Vector Size Encodings 001b through 111b directly indicate the number of each downstream Port's **Egress Control Vector** register *Peer-to-Peer Port x Control* bit (Downstream Ports, offset 528h[3:0]). ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	HwInit	Yes	100b
15:11	***Reserved***		RsvdP	No	000b

Register 11-83. 524h ACS Control and Capability (Downstream Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Control					
16	***Reserved***	Port 0	RsvdP	No	0
	ACS Source Validation Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
17	***Reserved***	Port 0	RsvdP	No	0
	ACS Translation Blocking Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
18	***Reserved***	Port 0	RsvdP	No	0
	ACS P2P Request Redirect Enable Enables or disables ACS Peer-to-Peer Request redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
19	***Reserved***	Port 0	RsvdP	No	0
	ACS P2P Completion Redirect Enable Enables or disables ACS Peer-to-Peer Completion redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
20	***Reserved***	Port 0	RsvdP	No	0
	ACS Upstream Forwarding Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Port 0	RsvdP	No	0
	ACS P2P Egress Control Enable Enables or disables ACS Peer-to-Peer Egress control. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Port 0	RsvdP	No	0
	ACS Direct Translated P2P Enable Enables or disables ACS Direct Translated Peer-to-Peer. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 11-84. 528h Egress Control Vector (Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
*Note: The Peer-to-Peer Port x Control bits are valid when the **ACS Control** register ACS P2P Egress Control Enable bit (Downstream Ports, offset 524h[21]) is Set.*					
0	***Reserved***	Port 0	RsvdP	No	0
	Peer-to-Peer Port 0 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
1	***Reserved***	Port 0	RsvdP	No	0
	Peer-to-Peer Port 1 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
2	***Reserved***	Port 0	RsvdP	No	0
	Peer-to-Peer Port 2 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
3	***Reserved***	Port 0	RsvdP	No	0
	Peer-to-Peer Port 3 Control 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
31:4	***Reserved***		RsvdP	No	0000_000h

11.16 Device-Specific Registers (Offsets 530h – B88h)

This section details the Device-Specific registers located at offsets 530h through B88h. Device-Specific registers are unique to the PEX 8605 and not referenced in the *PCI Express Base r2.1*. Table 11-21 defines the register map.

Other Device-Specific registers are detailed in Section 11.14, "Device-Specific Registers (Offsets 1C0h – 444h)."

Note: It is recommended that these registers not be changed from their default values.

Table 11-21. Device-Specific Register Map (Offsets 530h – B88h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Factory Test Only/Reserved	530h –	570h
Device-Specific Registers – Port Configuration (Offset 574h)		574h
Device-Specific Registers – General-Purpose Input/Output Control (Offsets 62Ch – 63Ch)		62Ch … 63Ch
Factory Test Only/Reserved	640h –	65Ch
Device-Specific Registers – Negotiated Link Width (Offsets 660h – 67Ch)		660h … 67Ch
Reserved	680h –	94Ch
Next Capability Offset 2 (000h) / 1h / PCI Express Extended Capability ID 2 (000Bh)		950h … 95Ch
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		
Factory Test Only/Reserved	960h –	9ECh
Device-Specific Registers – Ingress Credit Handler Control and Status (Offsets 9F0h – 9FCh)		9F0h … 9FCh
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – A2Ch)		A00h … A2Ch
Factory Test Only/Reserved	A30h –	B7Ch
Device-Specific Registers – Physical Layer (Offsets B80h – B88h)		B80h … B88h

11.16.1 Device-Specific Registers – Port Configuration (Offset 574h)

This section details the Device-Specific Port Configuration register. Table 11-22 defines the register map.

Table 11-22. Device-Specific Port Configuration Register Map (Port 0)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Port Configuration				574h

Register 11-85. 574h Port Configuration (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The Port configurations are listed in Table 11-10.*				
0	**Port Configuration** Port Configuration Link width, per Port. The serial EEPROM bit values always override the STRAP_PORTCFG input (if the serial EEPROM values are loaded; refer to Table 11-10). This register is reset only by a Fundamental Reset (PEX_PERST# assertion). 0 = x1x1x1x1 (Ports 0, 1, 2, and 3) 1 = x2x1x1 (Ports 0, 2, and 3)	RO	Yes	Defined by STRAP_PORTCFG input state
31:1	***Reserved***	RsvdP	No	0-0h

11.16.2 Device-Specific Registers – General-Purpose Input/Output Control (Offsets 62Ch – 63Ch)

General-Purpose Input/Output (GPIO) functions are selected when the **Debug Control** register *LANE_GOODx#/GPIOx Pin Function Select* bit (Port 0, offset 1DCh[22]) is Cleared. Each GPIO*x* pin is then individually programmable through a set of **GPIO Control** registers, which includes the pulse-width-modulated (PWM) registers. Table 11-23 defines the register map.

Note: *These registers are **reserved** (have no function) when the **Debug Control** register LANE_GOODx#/GPIOx Pin Function Select bit (Port 0, offset 1DCh[22]) is Set.*

Table 11-23. Device-Specific GPIO Control Register Map (Port 0)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
GPIO Control				62Ch
GPIO Interrupt Status				630h
GPIO PWM Value				634h
GPIO PWM Ramp Control				638h
Reserved			GPIO PWM Clock Frequency	63Ch

Register 11-86. 62Ch GPIO Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
*Notes: This register is **reserved** (has no function) when the **Debug Control** register LANE_GOODx#/GPIOx Pin Function Select bit (Port 0, offset 1DCh[22]) is Set.* *Bits [11:8] can be used to mask their respective **GPIO Interrupt Status** register GPIOx Interrupt bit (Port 0, offset 630h[3:0], respectively).*				
0	**GPIO0 Data** When the GPIO0 pin is programmed as an input (bit 4 is Cleared), reading this bit returns the value present on the GPIO0 pin. When the GPIO0 pin is programmed as an output (bit 4 is Set), values written to this bit appear on the GPIO0 pin. Reading this bit returns the previously written value.	RWU	Yes	0
1	**GPIO1 Data** When the GPIO1 pin is programmed as an input (bit 5 is Cleared), reading this bit returns the value present on the GPIO1 pin. When the GPIO1 pin is programmed as an output (bit 5 is Set), values written to this bit appear on the GPIO1 pin. Reading this bit returns the previously written value.	RWU	Yes	0
2	**GPIO2 Data** When the GPIO2 pin is programmed as an input (bit 6 is Cleared), reading this bit returns the value present on the GPIO2 pin. When the GPIO2 pin is programmed as an output (bit 6 is Set), values written to this bit appear on the GPIO2 pin. Reading this bit returns the previously written value.	RWU	Yes	0
3	**GPIO3 Data** When the GPIO3 pin is programmed as an input (bit 7 is Cleared), reading this bit returns the value present on the GPIO3 pin. When the GPIO3 pin is programmed as an output (bit 7 is Set), values written to this bit appear on the GPIO3 pin. Reading this bit returns the previously written value.	RWU	Yes	0
4	**GPIO0 Output Enable** 0 = GPIO0 pin is an input 1 = GPIO0 pin is an output	RWS	Yes	1
5	**GPIO1 Output Enable** 0 = GPIO1 pin is an input 1 = GPIO1 pin is an output	RWS	Yes	1
6	**GPIO2 Output Enable** 0 = GPIO2 pin is an input 1 = GPIO2 pin is an output	RWS	Yes	0
7	**GPIO3 Output Enable** 0 = GPIO3 pin is an input 1 = GPIO3 pin is an output	RWS	Yes	0

Register 11-86. 62Ch GPIO Control (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**GPIO0 Interrupt Enable** 0 = Masks ability for the GPIO0 input to generate an interrupt 1 = When the GPIO0 pin is programmed as an input (bit 4 is Cleared), changes on the GPIO0 pin are enabled to generate an interrupt	RW	Yes	0
9	**GPIO1 Interrupt Enable** 0 = Masks ability for the GPIO1 input to generate an interrupt 1 = When the GPIO1 pin is programmed as an input (bit 5 is Cleared), changes on the GPIO1 pin are enabled to generate an interrupt	RW	Yes	0
10	**GPIO2 Interrupt Enable** 0 = Masks ability for the GPIO2 input to generate an interrupt 1 = When the GPIO2 pin is programmed as an input (bit 6 is Cleared), changes on the GPIO2 pin are enabled to generate an interrupt	RW	Yes	0
11	**GPIO3 Interrupt Enable** 0 = Masks ability for the GPIO3 input to generate an interrupt 1 = When the GPIO3 pin is programmed as an input (bit 7 is Cleared), changes on the GPIO3 pin are enabled to generate an interrupt	RW	Yes	0
15:12	***Reserved***	RsvdP	No	0h
16	**GPIO0 Input De-Bounce Enable** 1 = When the GPIO0 pin is programmed as an input (bit 4 is Cleared), turns On the de-bounce circuit at GPIO0. The de-bounce time is 1.0 to 1.3 ms.	RW	Yes	0
17	**GPIO1 Input De-Bounce Enable** 1 = When the GPIO1 pin is programmed as an input (bit 5 is Cleared), turns On the de-bounce circuit at GPIO1. The de-bounce time is 1.0 to 1.3 ms.	RW	Yes	0
18	**GPIO2 Input De-Bounce Enable** 1 = When the GPIO2 pin is programmed as an input (bit 6 is Cleared), turns On the de-bounce circuit at GPIO2. The de-bounce time is 1.0 to 1.3 ms.	RW	Yes	0
19	**GPIO3 Input De-Bounce Enable** 1 = When the GPIO3 pin is programmed as an input (bit 7 is Cleared), turns On the de-bounce circuit at GPIO3. The de-bounce time is 1.0 to 1.3 ms.	RW	Yes	0
23:20	***Reserved***	RsvdP	No	0h
24	**GPIO0 PWM Enable** 1 = When the GPIO0 pin is programmed as an output (bit 4 is Set), turns On the pulse-width-modulated (PWM) output at GPIO0	RW	Yes	0
25	**GPIO1 PWM Enable** 1 = When the GPIO1 pin is programmed as an output (bit 5 is Set), turns On the PWM output at GPIO1	RW	Yes	0
26	**GPIO2 PWM Enable** 1 = When the GPIO2 pin is programmed as an output (bit 6 is Set), turns On the PWM output at GPIO2	RW	Yes	0
27	**GPIO3 PWM Enable** 1 = When the GPIO3 pin is programmed as an output (bit 7 is Set), turns On the PWM output at GPIO3	RW	Yes	0
31:28	***Reserved***	RsvdP	No	0h

Register 11-87. 630h GPIO Interrupt Status (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Notes: *This register is* ***reserved*** *(has no function) when the* ***Debug Control*** *register LANE_GOODx#/GPIOx Pin Function Select bit (Port 0, offset 1DCh[22]) is Set.* *Bits [3:0] can be masked by their respective* ***GPIO Control*** *register GPIOx Interrupt Enable bit (Port 0, offset 62Ch[11:8], respectively).*				
0	**GPIO0 Interrupt** Writing 1 Clears this bit. De-bounce delays Setting of this bit when the **GPIO Control** register *GPIO0 Input De-Bounce Enable* bit (Port 0, offset 62Ch[16]) is Set. 1 = GPIO0 pin state changed from input, to output (**GPIO Control** register *GPIO0 Output Enable* bit (Port 0, offset 62Ch[4]) is Set after being programmed as input (Cleared))	RW1C	Yes	PCFG
1	**GPIO1 Interrupt** Writing 1 Clears this bit. De-bounce delays Setting of this bit when the **GPIO Control** register *GPIO1 Input De-Bounce Enable* bit (Port 0, offset 62Ch[17]) is Set. 1 = GPIO1 pin state changed from input, to output (**GPIO Control** register *GPIO1 Output Enable* bit (Port 0, offset 62Ch[5]) is Set after being programmed as input (Cleared))	RW1C	Yes	PCFG
2	**GPIO2 Interrupt** Writing 1 Clears this bit. De-bounce delays Setting of this bit when the **GPIO Control** register *GPIO2 Input De-Bounce Enable* bit (Port 0, offset 62Ch[18]) is Set. 1 = GPIO2 pin state changed from input, to output (**GPIO Control** register *GPIO2 Output Enable* bit (Port 0, offset 62Ch[6]) is Set after being programmed as input (Cleared))	RW1C	Yes	PCFG
3	**GPIO3 Interrupt** Writing 1 Clears this bit. De-bounce delays Setting of this bit when the **GPIO Control** register *GPIO3 Input De-Bounce Enable* bit (Port 0, offset 62Ch[19]) is Set. 1 = GPIO3 pin state changed from input, to output (**GPIO Control** register *GPIO3 Output Enable* bit (Port 0, offset 62Ch[7]) is Set after being programmed as input (Cleared))	RW1C	Yes	PCFG
31:4	***Reserved***	RsvdP	No	0000_000h

Register 11-88. 634h GPIO PWM Value (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Values programmed into this register determine the quantity of steps (out of 256) that the output is driven High. For the remaining steps in the PWM cycle, the output is driven Low. The PWM value for each GPIO can be incremented or decremented by one step every *n* PWM cycles, where *n* is the value programmed into the **GPIO PWM Ramp Control** register (Port 0, offset 638h). ***Note:*** *This register is **reserved** (has no function) when the **Debug Control** register LANE_GOODx#/GPIOx Pin Function Select bit (Port 0, offset 1DCh[22]) is Set.*				
7:0	**GPIO0 PWM Value** Programming *n* outputs a waveform with *n*/255 cycles High and (255-*n*)/255 steps Low. Writes of 0 to the **GPIO Control** register *GPIO0 Output Enable* bit (Port 0, offset 62Ch[4]) program the value of this field to 00h. Writes of 1 to the *GPIO0 Output Enable* bit program the value of this field to FFh.	RWU	Yes	00h
15:8	**GPIO1 PWM Value** Programming *n* outputs a waveform with *n*/255 cycles High and (255-*n*)/255 steps Low. Writes of 0 to the **GPIO Control** register *GPIO1 Output Enable* bit (Port 0, offset 62Ch[5]) program the value of this field to 00h. Writes of 1 to the *GPIO1 Output Enable* bit program the value of this field to FFh.	RWU	Yes	00h
23:16	**GPIO2 PWM Value** Programming *n* outputs a waveform with *n*/255 cycles High and (255-*n*)/255 steps Low. Writes of 0 to the **GPIO Control** register *GPIO2 Output Enable* bit (Port 0, offset 62Ch[6]) program the value of this field to 00h. Writes of 1 to the *GPIO2 Output Enable* bit program the value of this field to FFh.	RWU	Yes	00h
31:24	**GPIO3 PWM Value** Programming *n* outputs a waveform with *n*/255 cycles High and (255-*n*)/255 steps Low. Writes of 0 to the **GPIO Control** register *GPIO3 Output Enable* bit (Port 0, offset 62Ch[7]) program the value of this field to 00h. Writes of 1 to the *GPIO3 Output Enable* bit program the value of this field to FFh.	RWU	Yes	00h

Register 11-89. 638h GPIO PWM Ramp Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PWM ramping starts when a value of *n*=1 to 255 is programmed, and ends when the PWM value reaches 255 or 0. The *n* value is used as input to the **GPIO PWM Value** register (Port 0, offset 634h). ***Note:*** *This register is **reserved** (has no function) when the **Debug Control** register LANE_GOODx#/GPIOx Pin Function Select bit (Port 0, offset 1DCh[22]) is Set.*				
6:0	**GPIO0 PWM Ramp Period** For every Ramp Period (RP) of complete PWM cycles, the GPIO0 PWM value is increased/decreased by 1. 00h = PWM ramp is disabled	RW	Yes	00h
7	**GPIO0 PWM Ramp Sign Bit** The value of 0/1 controls that the GPIO0 PWM value is incremented/ decremented after every "RP of complete PWM cycles."	RW	Yes	0
14:8	**GPIO1 PWM Ramp Period** For every RP of complete PWM cycles, the GPIO1 PWM value is increased/ decreased by 1. 00h = PWM ramp is disabled	RW	Yes	00h
15	**GPIO1 PWM Ramp Sign Bit** The value of 0/1 controls that the GPIO1 PWM value is incremented/ decremented after every "RP of complete PWM cycles."	RW	Yes	0
22:16	**GPIO2 PWM Ramp Period** For every RP of complete PWM cycles, the GPIO2 PWM value is increased/ decreased by 1. 00h = PWM ramp is disabled	RW	Yes	00h
23	**GPIO2 PWM Ramp Sign Bit** The value of 0/1 controls that the GPIO2 PWM value is incremented/ decremented after every "RP of complete PWM cycles."	RW	Yes	0
30:24	**GPIO3 PWM Ramp Period** For every RP of complete PWM cycles, the GPIO3 PWM value is increased/ decreased by 1. 00h = PWM ramp is disabled	RW	Yes	00h
31	**GPIO3 PWM Ramp Sign Bit** The value of 0/1 controls that the GPIO3 PWM value is incremented/ decremented after every "RP of complete PWM cycles."	RW	Yes	0

Register 11-90. 63Ch GPIO PWM Clock Frequency (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *This register is* ***reserved*** *(has no function) when the* ***Debug Control*** *register LANE_GOODx#/GPIOx Pin Function Select bit (Port 0, offset 1DCh[22]) is Set.*				
7:0	**PWM Clock Divider** Controls the PWM step frequency (duration of each step). PWM functions repeat in cycles of 256 steps. The value in this register divides an input clock of 62.5 MHz by a programmed value of 1 to 256 (where 0 = 256). Because every PWM cycle has 256 steps, the fastest/slowest PWM base frequency is 245.1 KHz/1.908 KHz, respectively. 00h = 1.908 KHz (slowest) 01h = 245.1KHz (fastest)	RW	Yes	00h
31:8	***Reserved***	RsvdP	No	0000_00h

11.16.3 Device-Specific Registers – Negotiated Link Width (Offsets 660h – 67Ch)

This section details the Device-Specific Negotiated Link Width register. Table 11-24 defines the register map.

Table 11-24. Device-Specific Negotiated Link Width Register Map (Port 0)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Factory Test Only			660h –	668h
Reserved			Negotiated Link Width for Ports 0, 1, 2, 3	66Ch
Reserved				670h
Factory Test Only			674h –	67Ch

Register 11-91. 66Ch Negotiated Link Width for Ports 0, 1, 2, 3 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *Downstream Ports are always x1 Link width.*				
0	**Negotiated Link Width for Port 0** 0 = x1 1 = x2	RO	No	Defined by STRAP_PORTCFG input state
1	**Link Speed for Port 0** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
2	**Negotiated Link Width for Port 1** 0 = x1 1 = ***Reserved***	RO	No	0
3	**Link Speed for Port 1** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
4	**Negotiated Link Width for Port 2** 0 = x1 1 = ***Reserved***	RO	No	0
5	**Valid Negotiated Link Width for Port 2** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
6	**Negotiated Link Width for Port 3** 0 = x1 1 = ***Reserved***	RO	No	0
7	**Valid Negotiated Link Width for Port 3** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
31:8	***Reserved***	RsvdP	No	0000_00h

11.16.4 Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)

This section details the Device-Specific, Vendor-Specific Extended Capability 2 registers. Table 11-25 defines the register map.

Table 11-25. Device-Specific, Vendor-Specific Extended Capability 2 Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (000h) / Capability Version 2 (1h)	PCI Express Extended Capability ID 2 (000Bh)	950h
Vendor-Specific Header 2		954h
Hardwired Device ID	Hardwired Vendor ID	958h
Reserved	Hardwired Revision ID	95Ch

Register 11-92. 950h Vendor-Specific Extended Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID 2** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** 000h = This extended capability is the last capability in the PEX 8605 Extended Capabilities list	RO	Yes	000h

Register 11-93. 954h Vendor-Specific Header 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Vendor-Specific ID 2** ID Number of this Extended Capability structure.	RO	Yes	0001h
19:16	**Vendor-Specific Rev 2** Version Number of this structure.	RO	Yes	0h
31:20	**Vendor-Specific Length 2** Quantity of bytes in the entire structure.	RO	Yes	028h

Register 11-94. 958h PLX Hardwired Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Hardwired Vendor ID** Always returns the PLX PCI-SIG-assigned Vendor ID value, 10B5h.	RO	No	10B5h
31:16	**Hardwired Device ID** Always returns the PEX 8605 default Device ID value, 8605h.	RO	No	8605h

Register 11-95. 95Ch PLX Hardwired Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Hardwired Revision ID** Always returns the PEX 8605 default PCI Revision ID value, AAh or ABh.	RO	No	Current Rev # (AAh or ABh)
31:8	***Reserved***	RsvdP	No	0000_00h

11.16.5 Device-Specific Registers – Ingress Credit Handler Control and Status (Offsets 9F0h – 9FCh)

This section details the Device-Specific Ingress Credit Handler (INCH) Control and Status registers. Table 11-26 defines the register map.

Table 11-26. Device-Specific INCH Control and Status Register Map (Port 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Factory Test Only	INCH Status Control for Ports 0 and 1	9F0h
INCH Status Read for Ports 0 and 1		9F4h
INCH Status Control for Ports 2 and 3		9F8h
INCH Status Read for Ports 2 and 3		9FCh

Register 11-96. 9F0h INCH Status Control for Ports 0 and 1 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**Credit Available Select** Write the value here to specify which of the twelve Credit Available registers to read. This value is used as input to the **INCH Status Read for Ports 0 and 1** register *Read Credit Available Value* field (Port 0, offset 9F4h[19:0]). 0h = INCH Threshold Port 0 VC0 Posted credits available 1h = INCH Threshold Port 0 VC0 Non-Posted credits available 2h = INCH Threshold Port 0 VC0 Completion credits available 3h = INCH Threshold Port 1 VC0 Posted credits available 4h = INCH Threshold Port 1 VC0 Non-Posted credits available 5h = INCH Threshold Port 1 VC0 Completion credits available 8h = **INCH Threshold Port 0 VC0 Posted** register (Port 0, offset A00h) 9h = **INCH Threshold Port 0 VC0 Non-Posted** register (Port 0, offset A04h) Ah = **INCH Threshold Port 0 VC0 Completion** register (Port 0, offset A08h) Bh = **INCH Threshold Port 1 VC0 Posted** register (Port 0, offset A0Ch) Ch = **INCH Threshold Port 1 VC0 Non-Posted** register (Port 0, offset A10h) Dh = **INCH Threshold Port 1 VC0 Completion** register (Port 0, offset A14h) All other encodings are ***reserved***.	RWS	Yes	0h
23:4	***Reserved***	RsvdP	No	0h
31:24	***Factory Test Only***	RWS	Yes	00h

Register 11-97. 9F4h INCH Status Read for Ports 0 and 1 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	**Read Credit Available Value** Read register selected in the **INCH Status Control for Ports 0 and 1** register *Credit Available Select* field (Port 0, offset 9F0h[3:0]). The value returns the selected Credit Available register.	RWS	Yes	0_0000h
31:20	***Reserved***	RsvdP	No	000h

Register 11-98. 9F8h INCH Status Control for Ports 2 and 3 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**Credit Available Select** Write the value here to specify which of the 12 Credit Available registers to read. This value is used as input to the **INCH Status Read for Ports 2 and 3** register *Read Credit Available Value* field (Port 0, offset 9FCh[19:0]). 0h = INCH Threshold Port 2 VC0 Posted credits available (default) 1h = INCH Threshold Port 2 VC0 Non-Posted credits available 2h = INCH Threshold Port 2 VC0 Completion credits available 3h = INCH Threshold Port 3 VC0 Posted credits available 4h = INCH Threshold Port 3 VC0 Non-Posted credits available 5h = INCH Threshold Port 3 VC0 Completion credits available 8h = **INCH Threshold Port 2 VC0 Posted** register (Port 0, offset A18h) 9h = **INCH Threshold Port 2 VC0 Non-Posted** register (Port 0, offset A1Ch) Ah = **INCH Threshold Port 2 VC0 Completion** register (Port 0, offset A20h) Bh = **INCH Threshold Port 3 VC0 Posted** register (Port 0, offset A24h) Ch = **INCH Threshold Port 3 VC0 Non-Posted** register (Port 0, offset A28h) Dh = **INCH Threshold Port 3 VC0 Completion** register (Port 0, offset A2Ch) All other encodings are ***reserved***.	RWS	Yes	0h
25:4	***Reserved***	RsvdP	No	0-0h
29:26	***Factory Test Only***	RWS	Yes	0h
31:30	***Reserved***	RsvdP	No	00b

Register 11-99. 9FCh INCH Status Read for Ports 2 and 3 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	**Read Credit Available Value** Read register selected in the **INCH Status Control for Ports 2 and 3** register *Credit Available Select* field (Port 0, offset 9F8h[3:0]). The value returns the selected Credit Available register.	RWS	Yes	0_0000h
31:20	***Reserved***	RsvdP	No	000h

11.16.6 Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – A2Ch)

This section details the Device-Specific Ingress Credit Handler (INCH) Threshold registers. **Changing credit values from default register values must be done carefully; otherwise, the PEX 8605 will not properly function.** Table 11-27 defines the register map.

Table 11-27. Device-Specific INCH Threshold Register Map (Port 0)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
INCH Threshold Port 0 VC0 Posted				A00h
Factory Test Only/Reserved	INCH Threshold Port 0 VC0 Non-Posted			A04h
INCH Threshold Port 0 VC0 Completion				A08h
INCH Threshold Port 1 VC0 Posted				A0Ch
Factory Test Only/Reserved	INCH Threshold Port 1 VC0 Non-Posted			A10h
INCH Threshold Port 1 VC0 Completion				A14h
INCH Threshold Port 2 VC0 Posted				A18h
Factory Test Only/Reserved	INCH Threshold Port 2 VC0 Non-Posted			A1Ch
INCH Threshold Port 2 VC0 Completion				A20h
INCH Threshold Port 3 VC0 Posted				A24h
Factory Test Only/Reserved	INCH Threshold Port 3 VC0 Non-Posted			A28h
INCH Threshold Port 3 VC0 Completion				A2Ch

Register 11-100. A00h, A0Ch, A18h, A24h INCH Threshold Port *x* VC0 Posted (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Posted credits are used for VC0 Memory Write and Message transactions. Port *x* is Ports 0, 1, 2, and 3. These Ports are associated with register offsets A00h, A0Ch, A18h, and A24h, respectively.				
2:0	***Reserved***	RsvdP	No	000b
7:3	**Posted Payload Credit** Default advertised Posted Payload credit. Bit resolution is in units of 8. Each increment provides 8 Posted Payload credits (*for example*, Ah = 80 Posted Payload credits). Each credit means that 16 bytes of storage are reserved for Posted TLP Payload data. Port 0 = 32 Payload Credits Downstream Port = 128 Payload Credits	RWS	Yes	Refer to Description
13:8	**Posted Header Credit** Default advertised Posted Header credit. Bit resolution is 1 for 1. Each increment provides 1 Posted Header credit (*for example*, Ah = 10 Posted Header credits). Each credit means that storage is reserved for the entire Header of a Posted TLP. Port 0 = 16 Header Credits Downstream Port = 22 Header Credits	RWS	Yes	Refer to Description
31:14	***Reserved***	RsvdP	No	0-0h

Register 11-101. A04h, A10h, A1Ch, A28h INCH Threshold Port *x* VC0 Non-Posted (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Non-Posted credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions. Port *x* is Ports 0, 1, 2, and 3. These Ports are associated with register offsets A04h, A10h, A1Ch, and A28h, respectively.				
7:0	**Non-Posted Payload Credit** The Non-Posted Payload is stored with the Non-Posted Header; therefore Non-Posted Payload credit is always available. Because of this, the PEX 8605 hardwires this field to 00h (infinite credits).	RsvdP	Yes	00h
13:8	**Non-Posted Header Credit** Default advertised Non-Posted Header credit. Bit resolution is 1 for 1. Each increment provides 1 Non-Posted Header credit (*for example*, Ah = 10 Non-Posted Header credits). Each credit means that storage is reserved for the entire Header of a Non-Posted TLP. Port 0 = 10 Header Credits Downstream Port = 16 Header Credits	RWS	Yes	Refer to Description
23:14	***Reserved***	RsvdP	No	0-0h
25:24	***Factory Test Only***	RWS	Yes	00b
27:26	***Reserved***	RsvdP	No	00b
31:28	***Factory Test Only***	RW	Yes	0h

Register 11-102. A08h, A14h, A20h, A2Ch INCH Threshold Port *x* VC0 Completion (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Completion credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions. Port *x* is Ports 0, 1, 2, and 3. These Ports are associated with register offsets A08h, A14h, A20h, and A2Ch, respectively.				
2:0	***Reserved***	RsvdP	No	000b
7:3	**Completion Payload Credit** Default advertised Completion Payload credit. Bit resolution is in units of 8. Each increment provides 8 Completion Payload Credits (*for example*, Ah = 80 Completion Payload credits). Each Credit means that 16 bytes of storage are reserved for Completion TLP Payload data. Port 0 = 224 Payload Credits Downstream Port = 128 Payload Credits	RWS	Yes	Refer to Description
13:8	**Completion Header Credit** Default advertised Completion Header credit. Bit resolution is 1 for 1. Each increment provides 1 Completion Header credit (*for example*, Ah = 10 Completion Header credits). Each credit means that storage is reserved for the entire Header of a Completion TLP. Port 0 = 28 Header Credits Downstream Port = 16 Header Credits	RWS	Yes	Refer to Description
31:14	***Reserved***	RsvdP	No	0-0h

11.16.7 Device-Specific Registers – Physical Layer (Offsets B80h – B88h)

This section details the Device-Specific Physical Layer (PHY) **Advertised N_FTS** register, located at offset B84h; the remaining register within this structure are ***Factory Test Only***. Table 11-28 defines the register map.

Other Device-Specific PHY registers are detailed in Section 11.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)."

Table 11-28. Device-Specific PHY Register Map (Offsets B80h – B88h) (Port 0)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Factory Test Only				B80h
Reserved		Advertised N_FTS		B84h
SerDes Test				B88h

Register 11-103. B84h Advertised N_FTS (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Advertised N_FTS** Advertised Number of Fast Training Sets (N_FTS) value to transmit for all Ports (in Training Sets). Used, along with Link speed, for determining the L1 Exit Latency (**Link Capability** register *L1 Exit Latency* field (All Ports, offset 74h[14:12])).	RWS	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 11-104. B88h SerDes Test (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Bit Error Checker**	RW	Yes	0
1	***Factory Test Only***	RW	Yes	0
2	**Data Bus Width Select**	RW	Yes	0
3	**Packet Length Select**	RW	Yes	0
4	***Factory Test Only***	RW	Yes	0
5	**Comma Detection Enable**	RW	Yes	1
6	**Comma Pattern Generator Enable**	RW	Yes	0
7	**TSEQ Pattern G Enable**	RW	Yes	0
9:8	**PRBS Number Select**	RW	Yes	00b
15:10	***Factory Test Only***	RW	Yes	0-0h
16	**SerDes 0 BIST Generator/Checker Enable** SerDes 0 PRBS Enable. Bits SMB_RX_BISTEN_U and SMB_TX_BISTEN_U of L0_PREG_AD20_IN. 0 = Disables PRBS sequence generation/checking on SerDes 0 1 = Enables PRBS sequence generation/checking on SerDes 0 ***Notes: This bit and the Physical Layer Test register SerDes 0 User Test Pattern Enable bit (Port 0, offset 228h[28]) are mutually exclusive functions and must not be enabled together for SerDes 0. The logical result of both bits ANDed with one another must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port Control register Port 0 Quiet bit (Port 0, offset 234h[20]) is Set.***	RW	Yes	0
17	**SerDes 1 BIST Generator/Checker Enable** SerDes 1 PRBS Enable. Bits SMB_RX_BISTEN_U and SMB_TX_BISTEN_U of L1_PREG_AD20_IN. 0 = Disables PRBS sequence generation/checking on SerDes 1 1 = Enables PRBS sequence generation/checking on SerDes 1 ***Notes: This bit and the Physical Layer Test register SerDes 1 User Test Pattern Enable bit (Port 0, offset 228h[29]) are mutually exclusive functions and must not be enabled together for SerDes 1. The logical result of both bits ANDed with one another must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port's Port Control register Port x Quiet bit (Port 0, offset 234h[21:20]) is Set.***	RW	Yes	0

Register 11-104. B88h SerDes Test (Port 0) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
18	**SerDes 2 BIST Generator/Checker Enable** SerDes 2 PRBS Enable. Bits SMB_RX_BISTEN_U and SMB_TX_BISTEN_U of L2_PREG_AD20_IN. 0 = Disables PRBS sequence generation/checking on SerDes 2 1 = Enables PRBS sequence generation/checking on SerDes 2 ***Notes: This bit and the Physical Layer Test register SerDes 2 User Test Pattern Enable bit (Port 0, offset 228h[30]) are mutually exclusive functions and must not be enabled together for SerDes 2. The logical result of both bits ANDed with one another must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port Control register Port 2 Quiet bit (Port 0, offset 234h[22]) is Set.***	RW	Yes	0
19	**SerDes 3 BIST Generator/Checker Enable** SerDes 3 PRBS Enable. Bits SMB_RX_BISTEN_U and SMB_TX_BISTEN_U of L3_PREG_AD20_IN. 0 = Disables PRBS sequence generation/checking on SerDes 2 1 = Enables PRBS sequence generation/checking on SerDes 2 ***Notes: This bit and the Physical Layer Test register SerDes 3 User Test Pattern Enable bit (Port 0, offset 228h[31]) are mutually exclusive functions and must not be enabled together for SerDes 3. The logical result of both bits ANDed with one another must be 0.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port Control register Port 3 Quiet bit (Port 0, offset 234h[23]) is Set.***	RW	Yes	0
27:20	***Reserved***	RsvdP	No	00h
31:28	**SerDes RESET_B** Writing 1 to these bits causes the RESET_B and RESET_B_U inputs to the corresponding SerDes to assert for 128 µs. This reset also causes the corresponding LTSSM to return to its initial state. These bits always return a value of 0 when read.	RW1C	Yes	0h

11.17 Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

This section details the Advanced Error Reporting Extended Capability registers. Table 11-29 defines the register map.

Table 11-29. Advanced Error Reporting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h or 148h) / Capability Version (1h)	PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Reserved	Correctable Error Status	FC4h
Reserved	Correctable Error Mask	FC8h
Advanced Error Capabilities and Control		FCCh
Header Log 0		FD0h
Header Log 1		FD4h
Header Log 2		FD8h
Header Log 3		FDCh

Register 11-105. FB4h Advanced Error Reporting Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID**		RO	Yes	0001h
19:16	**Capability Version**		RO	Yes	1h
31:20	**Next Capability Offset** Program to 138h, which addresses the **Power Budget Extended Capability** structure.	Port 0	RO	Yes	138h
	Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	Downstream	RO	Yes	148h

Register 11-106. FB8h Uncorrectable Error Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *If an individual error is masked (corresponding bit in the* ***Uncorrectable Error Mask*** *register (offset FBCh) is Set) when the error is detected, its Error Status bit is still updated; however, an error reporting Message (ERR_FATAL or ERR_NONFATAL) is* ***not*** *sent to the Root Complex, and the* ***Advanced Error Capabilities and Control*** *register First Error Pointer field (offset FCCh[4:0]) and* ***Header Log x*** *registers (offsets FD0h through FDCh) remain unchanged.*					
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
5	***Reserved***	Port 0	RsvdP	No	0
	Surprise Down Error Status 0 = No error is detected 1 = Error is detected	Downstream	RW1CS	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
13	**Flow Control Protocol Error Status** ***Reserved/Not supported***		RO	No	1
14	**Completion Timeout Status** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Status**		RW1CS	Yes	0
16	**Unexpected Completion Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
17	**Receiver Overflow Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
18	**Malformed TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
19	**ECRC Error Status** ***Not supported***		RsvdP	No	0

Register 11-106. FB8h Uncorrectable Error Status (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**Unsupported Request Error Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
21	***Reserved***	Port 0	RsvdP	No	0
	ACS Violation Error Status 0 = No violation detected 1 = Violation is detected	Downstream	RW1CS	Yes	0
22	**Uncorrectable Internal Error Status** 0 = No error is detected 1 = Error is detected	0	RW1CS	Yes	0
	Reserved	Otherwise	RsvdP	No	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 11-107. FBCh Uncorrectable Error Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Uncorrectable Error Status*** *register bits (All Ports, offset FB8h).*					
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
5	***Reserved***	Port 0	RsvdP	No	0
	Surprise Down Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
13	**Flow Control Protocol Error Mask** ***Reserved/Not supported***		RsvdP	No	0
14	**Completion Timeout Mask** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Mask**		RWS	Yes	0
16	**Unexpected Completion Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
19	**ECRC Error Mask** ***Not supported***		RsvdP	No	0

Register 11-107. FBCh Uncorrectable Error Mask (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**Unsupported Request Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
21	***Reserved***	Port 0	RsvdP	No	0
	ACS Violation Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
22	**Uncorrectable Internal Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	0	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
31:23	***Reserved***		RsvdP	No	0-0h

Register 11-108. FC0h Uncorrectable Error Severity (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
5	**Surprise Down Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	Port 0	RO	No	1
		Downstream	RWS	Yes	1
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
13	**Flow Control Protocol Error Severity**		RO	No	1
14	**Completion Timeout Severity** ***Not applicable to switches.*** Because the Status and Mask are both ***reserved*** for this bit, Severity can be ignored.		RsvdP	No	0
15	**Completer Abort Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error reported as fatal		RWS	Yes	0
16	**Unexpected Completion Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
17	**Receiver Overflow Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
18	**Malformed TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
19	**ECRC Error Severity** ***Not supported***		RsvdP	No	0

Register 11-108. FC0h Uncorrectable Error Severity (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**Unsupported Request Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
21	***Reserved***	Port 0	RsvdP	No	0
	ACS Violation Error Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	Downstream	RWS	Yes	0
22	**Uncorrectable Internal Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	0	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
31:23	***Reserved***		RsvdP	No	0-0h

Register 11-109. FC4h Correctable Error Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective* ***Correctable Error Mask*** *register bits (All Ports, offset FC8h).*					
0	**Receiver Error Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
5:1	***Reserved***		RsvdP	No	0-0h
6	**Bad TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
7	**Bad DLLP Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
8	**REPLAY NUM Rollover Status** Replay Number Rollover status. 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
11:9	***Reserved***		RsvdP	No	000b
12	**Replay Timer Timeout Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
13	**Advisory Non-Fatal Error Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
14	**Corrected Internal Error Status** 0 = No error is detected 1 = Error is detected	0	RW1CS	Yes	0
	Reserved	Otherwise	RsvdP	No	0
15	**Header Log Overflow Status** 0 = No error is detected 1 = Error is detected		RW1CS	Yes	0
31:16	***Reserved***		RsvdP	No	0000h

Register 11-110. FC8h Correctable Error Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *The bits in this register can be used to mask their respective* ***Correctable Error Status*** *register bits (All Ports, offset FC4h).*					
0	**Receiver Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
5:1	***Reserved***		RsvdP	No	0-0h
6	**Bad TLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
8	**REPLAY NUM Rollover Mask** Replay Number Rollover mask. 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
11:9	***Reserved***		RsvdP	No	000b
12	**Replay Timer Timeout Mask** 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
13	**Advisory Non-Fatal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	1
14	**Corrected Internal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	0	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
15	**Header Log Overflow Mask** 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	1
31:16	***Reserved***		RsvdP	No	0000h

Register 11-111. FCCh Advanced Error Capabilities and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**First Error Pointer** Identifies the bit position of the first error reported in the **Uncorrectable Error Status** register (All Ports, offset FB8h).	ROS	No	1Fh
5	**ECRC Generation Capable** ***Not supported***	RsvdP	No	0
6	**ECRC Generation Enable** ***Not supported***	RsvdP	No	0
7	**ECRC Check Capable** ***Not supported***	RsvdP	No	0
8	**ECRC Check Enable** ***Not supported***	RsvdP	No	0
31:9	***Reserved***	RsvdP	No	0-0h

Register 11-112. FD0h Header Log 0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 0** First DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 11-113. FD4h Header Log 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 1** Second DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 11-114. FD8h Header Log 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 2** Third DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 11-115. FDCh Header Log 3 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 3** Fourth DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

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Chapter 12 Test and Debug

12.1 Introduction

This chapter describes the following test- and debug-related information:

- Physical Layer Loopback Operation
- User Test Pattern
- Pseudo-Random Bit Sequence
- Using the SerDes Diagnostic Data Register
- PHY Testability Features
- JTAG Interface
- Lane Good Status LEDs

12.2 Physical Layer Loopback Operation

12.2.1 Overview

Physical Layer (PHY) Loopback functions are used to test the SerDes in the PEX 8605, connections between devices, and SerDes of external devices, as well as various PEX 8605 and external digital logic. The PEX 8605 supports three types of Loopback operations, as described in Table 12-1. Additional information regarding each type is provided in the sections that follow.

Table 12-1. Loopback Operations

Operation	Description
Analog Loopback Master Mode	This mode depends upon an external device or passive connection (*such as* a cable) to loopback the transmitted data to the PEX 8605, without SKIP Ordered-Set clock compensation. If an external device is used, it must not include its Elastic buffer in the Slave Loopback data path, so that SKIP Ordered-Sets are not inserted. A device's re-transmitted Receive data must be sent back to the Master, synchronous to the Master's Transmit Reference Clock. *That is*, the Slave device re-serializes the Transmit data, using the recovered clock from the received data. In that mode, the PRBS generator and checker should be used to create and check the data pattern.
Digital Loopback Master Mode	This mode depends upon an external device to loopback the transmitted data that includes at least its Elastic buffer in the Loopback data path, allowing for reliable loopback testing, in case the two devices have asynchronous Reference Clock sources with Parts per Million (PPM) offsets. The Master's pattern generator inserts SKIP Ordered-Sets at regular intervals, and its received data checker can handle PPM offset clock compensation, by way of SKIP symbol addition or deletion. The PEX 8605 provides a User Test Pattern generator and checker that can be used for Digital loopback testing.
Digital Loopback Slave Mode	The PEX 8605 enters this mode when an external device transmits Training Sets with the *Loopback* Training Control Bit Set and the **SKIP Ordered-Set Interval** register *Analog Loopback Enable* bit (Port 0, offset 234h[6]) is Cleared. This is the default Loopback mode for the LTSSM Slave *Loopback.Active* substate. In this mode, the data is looped back at the 8-bit level, which includes the PEX 8605's Elastic buffer in the Slave Loopback data path. Asynchronous clock compensation can occur in the Elastic buffer through SKIP symbol addition or deletion, depending upon clock PPM offsets and fill threshold decoding. The Master data pattern checker must be able to handle the presence of SKIP Ordered-Sets and variations in their contents, when SKIP Ordered-Sets are transmitted.

12.2.2 Analog Loopback Master Mode

Analog Loopback Master mode is typically used for Analog Far-End testing (refer to Figure 12-1), with a shallow Loopback path Slave device, to determine overall Bit Error rates. However, it can also be used for passive external serial loopback with a cable. Looping back with a cable includes the internal circuitry, package connections to bond pads, package pins, board traces, and any connectors that might be in the test data path, as illustrated in Figure 12-2. A PRBS pattern is typically used for this mode, because it is appropriate for bit error rate testing. A User Test Pattern (UTP) is ***not*** recommended for this application – refer to Section 12.3 for details.

Figure 12-1. Analog Far-End Loopback

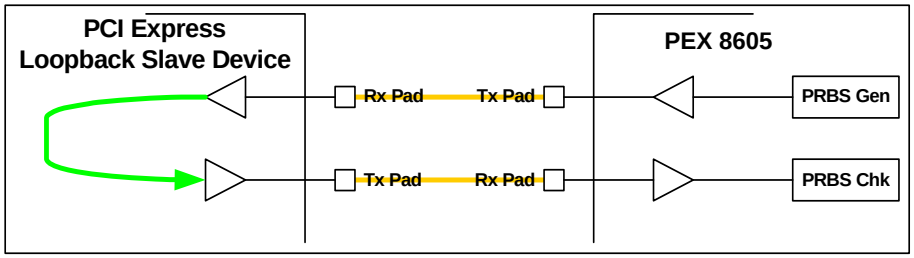
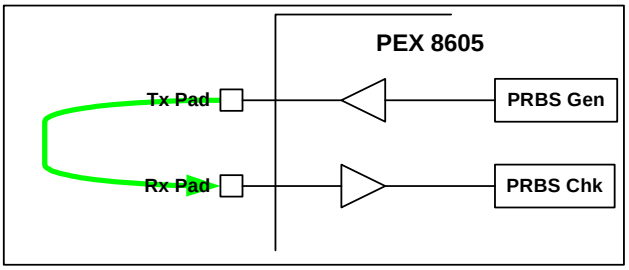


Figure 12-2. Cable Loopback



12.2.2.1 Initiating Far-End Analog Operations in PEX 8605 Master Devices

Note: *Initiating a Master Loopback operation on Port 0 can cause a Deadlock condition to occur, unless an I^2C Slave interface is used to write and read Configuration Space register bits instead of writing them through Port 0 Configuration transactions. Therefore, it is recommended to restrict Analog Master loopback testing to downstream Ports when external devices are used.*

One way to test Master Analog loopback with passive cables is to have Port 0 connected to a Root Complex, for Configuration Read/Write transactions that are used to Set and monitor the key device register bits. In that case, only downstream Ports would be test-capable, to avoid potential Deadlock conditions on Port 0. Alternatively, an I^2C Slave interface and Rapid Development Kit (RDK) software could be used to write or read the registers. This makes any Port testable. The user has the option of attaching one or more cables to the appropriate high-speed Tx and Rx differential pairs that belong to the Ports being tested.

Loopback cables can be attached before or after a standard power-up initialization sequence. If the cables are attached before power-up, use a serial EEPROM to program the Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Port 0, offset 230h[12, 8, 4, 0]). The bit arms the Port to enter the Master *Loopback.Entry* substate. When written from a serial EEPROM, the bit's assertion is present before the Ports begin Link training. In that case, the Ports directly transition to the LTSSM *Loopback* state from the LTSSM *Configuration* state. The LTSSM exits the *Polling* state and enters the *Configuration.LinkWidth.Start* substate, then immediately transitions to the Master *Loopback.Entry* substate.

At this point, users can sample the Port's **Physical Layer Port Command** register *Port x Ready as Loopback Master* bit (Port 0, offset 230h[15, 11, 7, 3]), to determine whether the bit is Set, which indicates that the Master has reached the LTSSM *Loopback.Active* substate. At this time, the PRBS engine can be enabled, by writing the **SerDes Test** register *SerDes x BIST Generator/Checker Enable* (PRBS Enable) bit(s) (Port 0, offset B88h[19:16]), for the SerDes associated with the Port being tested, with the sequences listed in Table 12-2.

Table 12-2. Sequence to Enable PRBS Transmission on Lanes 1, 2, and 3 (SerDes Test Register (Port 0, offset B88h)

Data	Description
0000_3074h	Select 8/16-bit PRBS
000E_3034h	Disable comma pattern generator, enable error checker
000E_3035h	Reset error checker
000E_3034h	Clear reset

The PRBS Receive data checker first synchronizes the de-serialized parallel data words from the returned pattern with a reference PRBS pattern generator. Once synchronized, the PRBS checker looks for errors, on a continuous basis. Any errors detected are logged in one or more of the **SerDes Diagnostic Data** register RO bits (Port 0, offset 238h[30 and 23:0]). The errors can be retrieved, by reading the appropriate bit.

If the *Port x Loopback Command* bits are not Set through the serial EEPROM, the Ports' Loopback Training Sets can be used to cause the Ports to linkup, by way of a Configuration cross-link track, resulting with the Ports being in the L0 Link PM state. This linkup of a Port, in response to its own Training Sets, works only if the Port's **Physical Layer Additional Status** register *Port x External Loopback Enable* bit (Port 0, offset 254h[19:16]) is Set by serial EEPROM. After the Port is in the L0 Link PM state, Configuration Space register programming can then be performed manually, to invoke a Master Loopback operation.

After the Ports linkup, users can direct the Ports linkup into an Analog Loopback Master condition, by writing the **Physical Layer Port Command** register *Port x Loopback Command* bit(s), (Port 0, offset 230h[12, 8, 4, 0]), through Port 0 and/or the I^2C Slave interface. However, this is not sufficient to initiate the LTSSM transition from the L0 Link PM state, to the *Loopback* state. The Link must pass through a *Recovery* substate, before the *Port x Loopback Command* bits can be sampled and allow the LTSSM to pass through the *Recovery* state to the *Loopback* state. To cause the Port to enter the *Recovery* state, users must Set the Port's **Link Control** register *Retrain Link* bit (Downstream Ports, offset 78h[5]). At this point, users should monitor the Port's *Port x Ready as Loopback Master* bit(s), and when Set, the PRBS engine(s) can be enabled, as previously described.

If loopback cables are attached after the device powers up, those Ports whose Lanes are floating unconnected did not detect Receivers. Therefore, those Ports are not trained up to the L0 Link PM state.

If the Port's *Port x Loopback Command* and *External Loopback Enable* bits for the downstream Ports to be tested are written ***before*** the cables are attached, then once cabled, there is Receiver detection, the Port(s) go through Link training, and then exit the LTSSM *Configuration* state and directly enter the *Loopback* state.

However, if the Port's *Port x Loopback Command* and *External Loopback Enable* bits are Set ***after*** the cables are attached, the Ports do not recognize their own Training Sets and will likely cycle back and forth between *Configuration* and *Detect*. Therefore, users must at least Set the *Port x External Loopback Enable* bit for the Port being tested, by way of serial EEPROM, if the PEX 8605 is powered up before the cables are attached. Users can then program the Port's *Port x Loopback Command* bit(s). In addition to this, a forced retrain is also needed, to enter into the *Loopback* state through the *Recovery* state, as previously described.

12.2.3 Digital Loopback Master Mode

The only difference between Analog and Digital Loopback Master modes is that the external device is assumed to have at least an Elastic buffer in the Loopback data path. Because of this, SKIP Ordered-Sets must be included in the test data pattern, if system clocking is asynchronous, which precludes use of the PRBS engine.

Figure 12-3 illustrates a Far-End Digital Loopback Master connection and data path.

The PEX 8605 provides a User Test Pattern engine on a per-Lane basis, for Digital Far-End Loopback testing. The user pattern itself, however, is common to all Lanes where it is enabled. Details on the use of the User Test Pattern registers and controls are described later in Section 12.5.

What is important to note about the data path (not shown in Figure 12-3) is that the pattern generators and checkers in the PEX 8605 Digital Loopback Master have 8b/10b encode, 10b/8b decode, and Elastic buffers included in the Tx/Rx path. The scramblers and de-scramblers are disabled. Therefore, the Digital Loopback Slave device must not scramble the returning data. The 10-bit data can be decoded to 8-bit, and encoded back to 10-bit as an option, and will not affect the UTP pattern checker in the PEX 8605, unless there is a coding error.

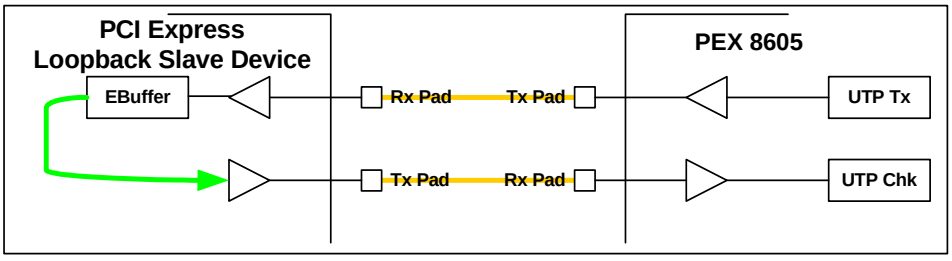
Digital Loopback Master mode is established by either programming method previously described in Section 12.2.2 for Analog Loopback Master mode. The Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Port 0, offset 230h[12, 8, 4, 0]) can be Set with a serial EEPROM, causing Loopback to be entered directly from the LTSSM *Configuration* state. Otherwise, the Port's *Port x Loopback Command* bit can be Set after linkup, and then the Port's **Link Control** register *Retrain Link* bit (Downstream Ports, offset 78h[5]) can be used to move the Port to the *Loopback* state, through the LTSSM *Recovery* state.

After Digital Loopback Master mode is established, Configuration Space register Writes are used to establish a User Test Pattern transmission, as well as error checking, which are described later in Section 12.3.

The UTP is multiplexed, unconditionally, onto the Transmit data path, upon Setting one or more of the **Physical Layer Test** register *SerDes x User Test Pattern Enable* bit(s) (Port 0, offset 228h[31:28]).

Note: *It is important to verify that the LTSSM is in a Master Loopback.Active substate, before writing 1 to the SerDes x User Test Pattern Enable bits. Therefore, do not use the serial EEPROM to Set the SerDes x User Test Pattern Enable bits. (Refer to Section 12.4 for details.)*

Figure 12-3. Digital Far-End Loopback



12.2.4 Digital Loopback Slave Mode

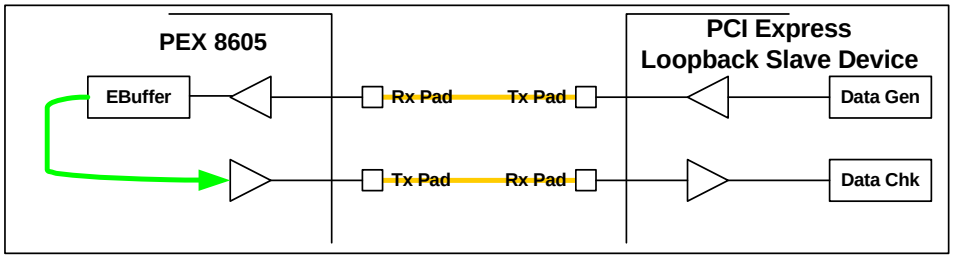
When a Port is in the LTSSM Slave *Loopback.Active* substate, it automatically becomes a Digital Loopback Slave, by default. The Port enters this state after it receives Training Sets with the *Loopback* Training Control Bit Set.

When a Port is a Digital Loopback Slave, it includes the Elastic buffer in the Slave Loopback data path. The Loopback Master must provide the test data pattern and data pattern checker (*such as* a PEX 8605 User Test Pattern). The Loopback Master must also transmit SKIP Ordered-Sets with the data pattern. Depending upon the PEX 8605 Reference Clock source's PPM offset, the PEX 8605 Digital Loopback Slave's Elastic buffers can compensate for the offset, by returning more or fewer SKIP symbols than the PEX 8605 received from the Master. Therefore, the Master's data pattern checker must make provisions for this when decoding for errors.

This mode is ***not*** suitable for a PRBS pattern as transmitted from the Master, because neither device can compensate for Reference Clock offset differences, should they exist.

To force the Loopback path into Digital Loopback Slave mode, the Slave must be brought into the mode by a Master-connected device, through standard LTSSM tracks.

Figure 12-4. Digital Loopback Slave Mode



12.3 User Test Pattern

The PEX 8605 provides a User Test Pattern (UTP) Transmit and Receive data checker, for Digital Far-End Loopback testing. (Refer to Figure 12-3.) After LTSSM Loopback Master mode is established, Configuration Writes are used to fill the Test Data Pattern registers.One or more **Physical Layer Test** register *SerDes x User Test Pattern Enable* bit(s) (Port 0, offset 228h[31:28]) are used to start the UTP transmission, on the Lanes assigned to each bit. SKIP Ordered-Sets are inserted into the user's test data pattern, at the nearest data pattern boundary according to the programmed SKIP interval. That interval is determined by the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (Port 0, offset 234h[11:0]). The default interval is 1,180 symbol times.

The Test Pattern checker ignores SKIP Ordered-Sets returned by the Loopback Slave, because the quantity of SKIP symbols received can be different from the quantity transmitted. All other data is compared to the transmitted data, and errors are logged in the **SerDes Diagnostic Data** register (Port 0, offset 238h).

The 16-byte UTP is loaded into the **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, offsets 210h through 21Ch). The pattern is common to all Lanes. Prior to transmission, the 8b/10b encoder converts the unscrambled 16 bytes to 10-bit encoded data. Pattern bytes only go out as control symbols (k-bit set), if their corresponding **Physical Layer Command and Status** register *User Test Pattern K-Code Flag* bit (Port 0, offset 220h[31:16]) is Set.

Notice: ***Use care when Setting User Test Pattern K-Code Flag bits, because UTP logic does not check the validity of Control characters.***

The UTP Transmitter logic does not immediately transmit the UTP bytes upon being enabled – a fixed, 8-byte sync pattern (314D_5243h) is transmitted first. The sync word detection validates the physical Loopback wiring and connected device Loopback path, to qualify the UTP transmission's initiation. The sync DWord allows the Pattern Checking logic to determine the starting boundary of the received pattern byte sequence. Sync detection also enables Received Data error checking and logging. There are no sync-acquired status bits in the Physical Layer (PHY) registers; however, the UTP Error Counter saturates at 255d, if the UTP checker does not receive the synchronization word.

Notes: *The **SerDes Diagnostic Data** register UTP/PRBS Error Counter field (Port 0, offset 238h[23:16]) is the UTP Error Counter, when the register's PRBS Counter/-UTP Counter bit (bit 30) is Cleared.*

There are no explicit Control bits for deliberately injecting UTP errors into the transmission, to test the error checking ability. However, one way of testing the ability is to write a test pattern byte to a different value after the transmission has started. That usually causes a temporary unequal boundary condition, which will log an error. While not guaranteed to inject an error, this method is useful for testing error checking ability.

A UTP is not recommended for Master mode far-end cable testing, especially when initiated by way of serial EEPROM from a power-up sequence. If a UTP is enabled and looped back before Link training begins, the symbol framers will not have seen any COM symbols, and the true 10-bit symbol boundaries are unknown. The framer requires three COMs in a row, in the same bit position, to achieve symbol lock. Neither the sync pattern, nor the user pattern, would be detected in this case, and the test is certain to fail.

In addition to the 16-byte pattern registers, the UTP is enabled on a per-Lane basis, by Setting one or more of the **Physical Layer Test** register *SerDes x User Test Pattern Enable* bit(s) (Port 0, offset 228h[31:28]), for the SerDes associated with the Port being tested.

Note: *The UTP is unconditionally multiplexed onto the Transmit data path, upon setting the SerDes x User Test Pattern Enable bits. Therefore, it is necessary to verify that the LTSSM is in an LTSSM Master Loopback.Active substate* ***before*** *writing those Enable bits to a value of 1.* ***Do not use a serial EEPROM to Set the SerDes x User Test Pattern Enable bits.***

UTP testing results can be monitored in the **SerDes Diagnostic Data** register (Port 0, offset 238h). The register can be used to examine the Error Count in the *UTP/PRBS Error Counter* field [23:16], and expected/actual data of the first failing byte (fields [7:0 and 15:8], respectively). The *Status* bits are on a per-Lane basis. **The important field in this register is field [25:24] (*SerDes Diagnostic Data Select*).** When the Lane code is written to that field, the UTP status for that Lane appears in the *Status* fields. Bit 30 of the register (*PRBS Counter/-UTP Counter*) is a pattern type indicator, and is Cleared when UTP is enabled for a Lane.

Notes: *Any errors detected are logged in the* ***SerDes Diagnostic Data*** *register (Port 0, offset 238h). Use of this register is explained in Section 12.5.*

The UTP and PRBS Enables (refer to Section 12.4) are mutually exclusive, and must not be concurrently Set. *If both Enables are concurrently Set, the resulting operation is undefined. The UTP/PRBS Error Counter field continues to count, until it saturates at 255d. To Clear the Counter and allow it to begin logging errors again, write all zeros (0) to that field. Alternatively, the Counter status is Cleared if the SerDes x User Test Pattern Enable bit for that Lane is Cleared, and then Set again.*

12.4 Pseudo-Random Bit Sequence

A Pseudo-Random Bit Sequence (PRBS) generator and checker are useful as a diagnostic/debugging tool, and for measuring short- or long-term bit error rates in PCI Express systems. The PEX 8605 also uses a specially enabled power-up self-test that runs after reset, as a wafer sort test for use on automated test equipment. PRBS pattern generators and checkers reside within the SerDes_rclk_blk modules, because they transmit and receive 10- or 20-bit data directly to/from the SerDes modules. Locating them in the modules helps ensure tight timing and short trace length on SerDes Tx and Rx parallel data.

The PEX 8605 PRBS engine can be enabled, by writing the **SerDes Test** register *SerDes x BIST Generator/Checker Enable* (PRBS Enable) bit(s) (Port 0, offset B88h[19:16]), for the SerDes associated with the Port being tested, with the sequences listed in Table 12-2. Prior to enabling PRBS, an externally connected PCI Express device must be in an LTSSM Slave *Loopback.Active* substate. Furthermore, the reference clocking between the two devices must be synchronous. (*That is*, the returning PRBS pattern must have its transmission clock source synchronous to the PEX 8605 Reference Clock.) The PEX 8605 PRBS pattern generator does not insert any SKIP Ordered-Sets, and, if the Slave device inserts SKIP Ordered-Sets into the returning pattern, they cannot be ignored by the PRBS checker (it causes an error). Alternatively, the PRBS pattern can be used to test an external cable Loopback, after the correct LTSSM Master *Loopback.Active* substate is reached, as described in Section 12.2.2.

After a Lane's PRBS engine is enabled, the PRBS engine immediately begins to transmit the PRBS pattern on that Lane. No 8b/10b encoding is performed. The PRBS pattern generator produces 10- or 20-bit symbols on every Clock cycle, depending upon the current Link speed. The symbols are written directly into the SerDes Tx data Port, for immediate transmission.

The PRBS Receive Data Checking logic first synchronizes the de-serialized 10- or 20-bit Parallel Data symbols from the SerDes Rx data Port, using a reference PRBS pattern generator. After pattern synchronization is achieved, the Receive data checker begins comparing the Rx data symbols on a continuous basis, to discover any mismatch between a symbol's expected and received values.

PRBS testing results can be monitored in the **SerDes Diagnostic Data** register (Port 0, offset 238h). The register can be used to examine the Error Count in the *UTP/PRBS Error Counter* field [23:16]. Expected and actual data is not available when PRBS is used. The *Status* bits are on a per-Lane basis. **The important field in this register is field [25:24] (*SerDes Diagnostic Data Select*).** When the Lane code is written to that field, the PRBS status for that Lane appears in the *Status* fields. Bit 30 of the register (*PRBS Counter/-UTP Counter*) is a pattern type indicator, and is Set when PRBS is enabled for a Lane.

Note: *Any errors detected are logged in the **SerDes Diagnostic Data** register (Port 0, offset 238h). Use of this register is explained in Section 12.5.*

The PRBS and UTP (refer to Section 12.3) Enables are mutually exclusive, and must not be concurrently Set. *If both Enables are concurrently Set, the resulting operation is undefined. The UTP/PRBS Error Counter field continues to count, until it saturates at 255d. To Clear the Counter and allow it to begin logging errors again, write all zeros (0) to that field. Alternatively, the Counter status is Cleared if the SerDes x User Test Pattern Enable bit for that Lane is Cleared, and then Set again.*

The PRBS Error Count does not necessarily represent a true Bit Error rate. The PRBS checker detects one or more mismatched bits in each examined symbol, on a symbol-per-core-clock basis. Therefore, the Error Counter advances one count for every symbol mismatch, regardless of how many bits are in error for that failing symbol.

12.5 Using the SerDes Diagnostic Data Register

The **SerDes Diagnostic Data** register (Port 0, offset 238h) contents reflect the performance of the SerDes selected by the register's *SerDes Diagnostic Data Select* field [25:24], as defined in Table 12-3. This control is specific to this register, which reports results of UTP and PRBS tests.

Table 12-3. SerDes Register Contents (Port 0, offset 238h)

***SerDes Diagnostic Data Select* Field [25:24] Value**			
00b	**01b**	**10b**	**11b**
SerDes 0	SerDes 1	SerDes 2	SerDes 3

12.6 PHY Testability Features

The PEX 8605 includes several Configuration bits to ease PHY testability. Features include:

- Full support of the standard and modified compliance patterns
- Register controllability of the common block and Lane-specific inputs of the SerDes

Table 12-4 describes the Configuration bits.

Table 12-4. Configuration Bits to Ease PHY Testability

Register Bit(s)	Description
SerDes x Mask Electrical Idle Detect **Physical Layer Electrical Idle Detect Mask** register (Port 0, offset 204h[3:0])	**Never Detect Electrical Idle Mask.** When any one of these bits is Set, the Lane's *Electrical Idle* condition flag does not assert, regardless of the actual presence of Electrical Idle.
SerDes x Mask Receiver Not Detected **Physical Layer Receiver Not Detected Mask** register (Port 0, offset 204h[19:16])	**Always Detect a Receiver Mask.** When any one of these bits is Set, the PHY functions as if the Lane detected a Receiver, regardless of the actual presence of a Receiver.
Test Pattern x **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, offsets 210h through 21Ch)	A 16-byte test pattern can be written to these four registers. When UTP transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 12.2.3 for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.
Port x Scrambler Disable Command **Physical Layer Port Command** register (Port 0, offset 230h[13, 9, 5, 1])	Unconditionally disables the data scramblers on the Lanes of the corresponding Port, and causes the *Scrambler Disable* Training Control Bit to be Set in transmitted Training Sets. There is one bit for each Port.
Disable Port x **Port Control** register (Port 0, offset 234h[19:16])	When Set, unconditionally disables the Port. This is different from the LTSSM *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* substate and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, the SerDes that belong to the disabled Port are placed into the P1 SerDes Power state.
Port x Quiet **Port Control** register (Port 0, offset 234h[23:20])	When Set, the LTSSM remains in the *Detect.Quiet* substate on the Port if it is currently in, or returns to, that substate. Once in the *Detect.Quiet* substate, Receiver termination is enabled and the Transmitters are placed into the P0 SerDes Power state. The Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* substate.
Port x Test Pattern x Rate **Port Control** register (Port 0, offset 234h[27:24])	The Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if the Port's *Port x* bit is also Set (manual rate selection is enabled only when the *Port x* bit is Set).
Port x Receiver Error Counter **Port Receiver Error Counters** register (Port 0, offset 248h)	Contains four 8-bit fields that, when read, return the quantity of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this register is RO.

12.7 JTAG Interface

The PEX 8605 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is used to debug board connectivity for each pin.

12.7.1 *IEEE 1149.1* and *IEEE 1149.6* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly called the *JTAG Debug Port*, is an architectural standard described in the *IEEE Standard 1149.1-1990*. The *IEEE Standard 1149.6-2003* defines extensions to *1149.1* to support PCI Express SerDes testing. These standards describe methods for accessing internal device facilities, using a four- or five-signal interface.

The JTAG Debug Port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals** – JTAG Debug Port implements the four required JTAG signals – JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS – and optional JTAG_TRST# signal
- **Clock Requirements** – JTAG_TCK signal frequency ranges from 0 to 20 MHz
- **JTAG Reset Requirements** – Refer to Section 12.7.4

12.7.2 JTAG Instructions

The JTAG Debug Port provides the *IEEE Standard 1149.1-1990* BYPASS, EXTEST, SAMPLE, PRELOAD, CLAMP, and IDCODE instructions. *IEEE Standard 1149.6-2003* EXTEST_PULSE and EXTEST_TRAIN instructions are also supported. Table 12-5 lists the JTAG instructions, along with their input codes.

The PEX 8605 returns the JTAG IDCODE values listed in Table 12-6.

Table 12-5. JTAG Instructions

Instruction	Input Code	Comments
BYPASS	Fh	*IEEE Standard 1149.1-1990*
EXTEST	2h	
SAMPLE	3h	
PRELOAD	3h	
EXTEST_PULSE	9h	*IEEE Standard 1149.6-2003*
EXTEST_TRAIN	8h	
CLAMP	6h	*IEEE Standard 1149.1-1990*
IDCODE	Dh	

Table 12-6. JTAG IDCODE Values

Silicon Revision	Units	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
AA	Bits	0000b	1000_0110_0000_0101b	001_1100_1101b	1
	Hex	0h	8605h	1CDh	1h
	Decimal	0	34309	461	1
AB	Bits	0001b	1000_0110_0000_0101b	001_1100_1101b	1
	Hex	1h	8605h	1CDh	1h
	Decimal	1	34309	461	1

12.7.3 JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE Standard 1149.1-1994, is a supplement to the *IEEE Standard 1149.1-1990* and *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*. BSDL, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, allows a rigorous description of testability features in components which comply with the standard. This standard is used by automated test pattern generation tools for package interconnect tests, and Electronic Design Automation (EDA) tools for synthesized Test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical Port description, physical pin map, instruction set, and **Boundary** register description.

The logical Port description assigns symbolic names to the device's signal pins. Each pin includes a logical type of *in*, *out*, *in out*, *buffer*, or *linkage* that defines the logical direction of signal flow.

The physical pin map correlates the device's logical Ports to the physical pins of a specific package. A BSDL description can include several physical pin maps, and maps are provided with a unique name.

Instruction Set statements describe the bit patterns that must be shifted into the **Instruction** register to place the device in the various test modes defined by the standard. Instruction Set statements also support descriptions of instructions that are unique to the PEX 8605.

The **Boundary** register description lists each cell or shift stage of the **Boundary** register. Each cell has a unique number, the cell numbered 0 is the closest to the Test Data Out (JTAG_TDO) pin and the cell with the highest number is closest to the Test Data In (JTAG_TDI) pin. Each cell includes additional information, *such as*:

- Cell type
- Logical Port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

12.7.4 JTAG Reset Input – JTAG_TRST#

The JTAG_TRST# input is the asynchronous JTAG logic reset. When JTAG_TRST# is Low, it causes the PEX 8605's JTAG TAP Controller to initialize. In addition, when the JTAG TAP Controller is initialized, it selects the PEX 8605 standard logic path (core-to-I/O). It is recommended to take the following into consideration when implementing the asynchronous JTAG logic reset on a board:

- If JTAG functionality is required, consider one of the following:
  - JTAG_TRST# Input signal to use a Low-to-High transition once during PEX 8605 boot-up, along with the system PEX_PERST# signal
  - Hold the JTAG_TMS pin High while clocking the JTAG_TCK pin five times
- If JTAG functionality is not required, the JTAG_TRST# signal must be directly connected to VSS (Ground), to hold the JTAG TAP Controller inactive
- If the PEX 8605's JTAG TAP Controller is not intended to be used by the design, it is recommended that a 1.5KΩ pull-down resistor be connected to the JTAG_TRST# pin, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation

12.8 Lane Good Status LEDs

The PEX 8605 provides Lane Good outputs, LANE_GOOD[3:0]#, that can be used to control external circuitry, *such as* LEDs, to provide visual indication that the PHY of each Lane's Link is trained to at least x1 width.

Software can determine:

- Which Lanes have completed PHY linkup, by performing a Memory Read of the **Software Lane Status** register *Lane x Up Status* bits (Port 0, offset 1F4h[3:0, which correspond to Lanes [3-0], respectively).
- Whether the Port's Link has trained, by reading either the **Link Status** register *Data Link Layer Link Active* bit (Downstream Ports, offset 78h[29]) or **VC0 Resource Status** register *VC0 Negotiation Pending* bit (All Ports, offset 160h[17]). If the *Data Link Layer Link Active* bit is Set, or the *VC0 Negotiation Pending* bit is Cleared, the Link has completed Flow Control (FC) initialization.

  The **Link Status** register can be read by either a PCI Express Configuration Request or Memory Read. The **VC0 Resource Status** register can be read by either a PCI Express Enhanced Configuration access or Memory Read.
- The negotiated Link width, by reading the **Link Status** register *Negotiated Link Width* field (All Ports, offset 78h[25:20]). This register can be read by either a Configuration Request or Memory Read.

Table 12-7 describes the relationship of the LED On/Off patterns, as they relate to the Lane status indicated by LANE_GOOD[3:0]#.

Table 12-7. LANE_GOOD[3:0]# LED On/Off Patterns, by State

State	LED Pattern
Lane is disabled	Solid Off
Lane is enabled, 5.0 GT/s	Solid On
Lane is enabled, 2.5 GT/s, reduced Lanes are up[a]	0.5 seconds On, 0.5 seconds Off

a. "Reduced Lanes are up" applies only to Port 0, when Port 0's Link width is x2.

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Chapter 13 Electrical Specifications

13.1 Introduction

This chapter provides the PEX 8605 electrical specifications.

13.2 Power-Up/Power-Down Sequence

The PEX 8605 does not have power-sequencing requirements. The power rails can be powered up and powered down, in any sequence.

13.3 Absolute Maximum Ratings

Notice: ***Maximum limits indicate the temperatures and voltages above which permanent damage can occur. Proper operation at these conditions is not guaranteed, and continuous operation of the PEX 8605 at these limits is not recommended.***

Table 13-1. Absolute Maximum Rating (All Voltages Referenced to VSS System Ground)

Item	Symbol	Absolute Maximum Rating	Units
SerDes Analog Supply Voltage	PEX_VDDA_P3 PEX_VDDA_P2 PEX_VDDA_P1 PEX_VDDA_P0	-0.5 to +4.6	V
SerDes Digital Supply Voltage	PEX_VDDD0_P3 PEX_VDDD0_P2 PEX_VDDD0_P1 PEX_VDDD0_P0 PEX_VDDD1_P3 PEX_VDDD1_P2 PEX_VDDD1_P1 PEX_VDDD1_P0	-0.5 to +1.4	V
PLL Supply Voltage	PLL_AVDD	-0.5 to +1.4	V
Auxiliary Core (Logic) Supply Voltage	VAUX_CORE	-0.5 to +1.4	V
Auxiliary I/O (Logic) Supply Voltage	VAUX_IO	-0.5 to +4.6	V
Core (Logic) Supply Voltage	VDD_CORE	-0.5 to +1.4	V
I/O Interface Supply Voltage, 2.5 or 3.3V	VDD_IO	-0.5 to +4.6	V
Input Voltage (2.5 or 3.3V Interface)	V_I	-0.5 to +4.6	V
Operating Ambient Temperature (Industrial)	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C

13.4 Power Characteristics

Table 13-2. Operating Condition Power Supply Rails

Symbol	Parameter	Min	Typ	Max	Units
PEX_VDDA_P3 PEX_VDDA_P2 PEX_VDDA_P1 PEX_VDDA_P0	Analog SerDes Supply[a]	2.30	2.50 to 3.30	3.60	V
PEX_VDDD0_P3 PEX_VDDD0_P2 PEX_VDDD0_P1 PEX_VDDD0_P0 PEX_VDDD1_P3 PEX_VDDD1_P2 PEX_VDDD1_P1 PEX_VDDD1_P0	Digital SerDes Supply	0.95	1.00	1.10	V
PLL_AVDD	Analog PLL Supply	0.95	1.00	1.10	V
VAUX_CORE	Auxiliary Digital Core Supply	0.95	1.00	1.10	V
VAUX_IO	Auxiliary I/O Supply[a]	2.30	2.50 to 3.30	3.60	V
VDD_CORE	Digital Core Supply	0.95	1.00	1.10	V
VDD_IO	I/O Supply	2.30	2.50 to 3.30	3.60	V

a. Must be the same voltage as VDD_IO.

13.5 Power Consumption Estimates

Table 13-3. Power Consumption Estimates

Lanes	Ports	Core Logic[a]		SerDes Analog[b]		SerDes Digital[c]		I/O[d]		Total	
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ[e]	Max[f]
		(milliWatts)									
4	4	234	374	132	185	436	624	128	174	930	1,357
		(milliAmps)									
		234	374	40	56	436	624	39	53	–	–

a. Core Logic supply consists of VDD_CORE.

b. SerDes Analog supply consists of PEX_VDDA_P3, PEX_VDDA_P2, PEX_VDDA_P1, and PEX_VDDA_P0.

c. SerDes Digital supply consists of PEX_VDDD0_P3, PEX_VDDD0_P2, PEX_VDDD0_P1, PEX_VDDD0_P0, PEX_VDDD1_P3, PEX_VDDD1_P2, PEX_VDDD1_P1, PEX_VDDD1_P0, and PLL_AVDD.

d. I/O supply consists of VDD_IO.

e. Typical power based upon all Lanes active (L0 Link PM state), 100% traffic, typical voltages (1.00V, 3.30V), and room temperature (25°C).

f. Maximum power based upon all Lanes active (L0 Link PM state), maximum traffic, maximum voltages (1.10V, 3.60V), maximum temperature (85°C) and Fast-Fast (FF) process corner silicon.

13.6 I/O Interface Signal Groupings

Table 13-4. Signal Group PCI Express Analog Interface

Signal Group	Signal Type	Signals	Notes
(a)	PCI Express Output (Transmit)	PEX_PETn[3:0], PEX_PETp[3:0]	Refer to Table 13-6 and Table 13-7
(b)	PCI Express Input (Receive)	PEX_PERn[3:0], PEX_PERp[3:0]	Refer to Table 13-6 and Table 13-8
(c)	PCI Express Differential Clock Input	PEX_REFCLKn, PEX_REFCLKp	Refer to Table 13-6 and Table 13-9

Table 13-5. Signal Group Digital Interface

Signal Group	Signal Type	Signals	Note
(d)	Digital Output	EE_DI, FATAL_ERR#, JTAG_TDO, PROCMON	Refer to Table 13-6
(e)	Digital Input with Internal 50KΩ Pull-Up Resistor[a]	I2C_ADDR[2:0], JTAG_TCK, JTAG_TDI, JTAG_TMS, JTAG_TRST#, PEX_PERST#, PWRON_RST#, STRAP_DEBUG_SEL#, STRAP_FAST_BRINGUP#, STRAP_LEGACY, STRAP_PLL_BYPASS#, STRAP_PROBE_MODE#, STRAP_SERDES_MODE_EN#, STRAP_SMBUS_EN#, STRAP_SSC_CENTER#, STRAP_TESTMODE[3, 1], STRAP_UPCFG_TIMER_EN#, XTAL_IN	Refer to Table 13-6
(f)	Digital Input with Internal 50KΩ Pull-Down Resistor	STRAP_PORTCFG, STRAP_RC_MODE, STRAP_TESTMODE[2, 0]	Refer to Table 13-6
(g)	Bidirectional I/O Buffer, 2.5 or 3.3V, with Internal 50KΩ Pull-Up Resistor	EE_CS#, EE_DO, EE_SK, HP_PRSNT#, LANE_GOOD[3:0]#	Refer to Table 13-6
(h)	Bidirectional (Open Drain) with Internal 50KΩ Pull-Up Resistor	PEX_INTA#, WAKE#	Refer to Table 13-6
(i)	Bidirectional (Open Drain) I/O Buffer, 2.5 or 3.3V, with Schmitt-Trigger Input	I2C_SCL, I2C_SDA	Refer to Table 13-6
(j)	Manufacturing Test Input with Internal Pull-Down Resistor	MFG_AMC, MFG_TAPEN, MFG_TMC1, MFG_TMC2	Refer to Table 13-6

a. These signals must be pulled High to VDD_IO or Low to Ground, per the instructions provided in Section 3.4, "Signal Pin Descriptions."

Table 13-6. Analog and Digital Interfaces (All Signal Groups) – DC Electrical Characteristics

Symbol	Signal Group(s)	Parameter	Min	Typ	Max	Unit	Conditions
I_{OL}	d, g, i	Output Low Current at 2.5V	5.0	9.2	12.8	mA	@ V_{OL} = 0.4V
		Output Low Current at 3.3V	6.0	11.1	14.9	mA	@ V_{OL} = 0.4V
I_{OH}	d, g, i	Output High Current at 2.5V	5.0	12.1	19.1	mA	@ V_{OH} = 1.7V
		Output High Current at 3.3V	6.0	17.3	28.2	mA	@ V_{OH} = 2.4V
V_{IL}	e, f, g, h, j	Input Low Voltage at 2.5V	-0.3		0.7	V	
		Input Low Voltage at 3.3V	-0.3		0.8	V	
V_{IH}	e, f, g, h, j	Input High Voltage at 2.5V	1.7		VDD_IO + 0.3	V	
		Input High Voltage at 3.3V	2.0		VDD_IO + 0.3	V	
V_N	i	Schmitt Input at 2.5V	0.6		0.9	V	
		Schmitt Input at 3.3V	0.6		1.1	V	
V_P	i	Schmitt Input at 2.5V	0.9		1.8	V	
		Schmitt Input at 3.3V	1.2		2.1	V	
V_H	i	Schmitt Input at 2.5V	0.2		1.0	V	
		Schmitt Input at 3.3V	0.3		1.5	V	
C_{PIN}		Ball Capacitance			5	pF	
$I_{LEAKAGE}$		Input Leakage			±10	µA	
R_{PU}	g	Pull-Up Impedance	33.6K	50K	69.3K	Ω	
R_{PD}	g	Pull-Down Impedance	33.5K	50K	69.4K	Ω	

Table 13-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm. UI does not account for variations caused by Spread-Spectrum Clock (SSC). Refer to Note 1.
$V_{TX-DIFF-PP}$	Differential Peak-to-Peak Output Voltage	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Measured with compliance test load. $V_{TX-DIFF-PP} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
$V_{TX-DIFF-PP-LOW}$	Low Power Differential Peak-to-Peak Output Voltage	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Measured with compliance test load. $V_{TX-DIFF-PP-LOW} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ Must be implemented with no de-emphasis.
$V_{TX-DE-RATIO-3.5dB}$	Tx De-Emphasis Level Ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB	Ratio of the $V_{TX-DIFF-PP}$ of the 2nd and following bits after a transition, divided by the $V_{TX-DIFF-PP}$ of the 1st bit after a transition. Refer to Note 2.
$V_{TX-DE-RATIO-6dB}$	Tx De-Emphasis Level Ratio	N/A	5.5 (min) 6.5 (max)	dB	Ratio of the $V_{TX-DIFF-PP}$ of the 2nd and following bits after a transition, divided by the $V_{TX-DIFF-PP}$ of the 1st bit after a transition. Refer to Note 2.
$T_{MIN-PULSE}$	Instantaneous Pulse Width (including all jitter sources)	Not specified	0.9 (min)	UI	Measured relative to rising/falling pulse. Refer to Note 3.
T_{TX-EYE}	Minimum Tx Eye Width	0.75 (min)	0.75 (min)	UI	Does not include SSC nor REFCLK jitter. Includes Rj at 10^{-12}. Refer to Notes 3 and 4.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	0.125 (max)	Not specified	UI	Measured differentially at zero crossing points, after applying the 2.5 GT/s Clock Recovery function. Refer to Note 3.
$T_{TX-HF-DJ-DD}$	Tx Deterministic Jitter > 1.5 MHz	Not specified	0.15 (max)	UI	Deterministic jitter only. Refer to Note 3.
$T_{TX-LF-RMS}$	Tx RMS Jitter < 1.5 MHz	Not specified	3.0	ps RMS	Total energy measured over a 10-kHz to 1.5-MHz range.
$T_{TX-RISE-FALL}$	Tx Rise and Fall Time	0.125 (min)	0.15 (min)	UI	Measured differentially from 20 to 80% of swing. Refer to Note 3.
$T_{RF-MISMATCH}$	Tx Rise/Fall Mismatch	Not specified	0.1 (max)	UI	Measured from 20 to 80% differentially. Refer to Note 3.

Table 13-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
BW_{TX-PLL}	Maximum Tx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 5.
$BW_{TX-PLL-LO-3DB}$	Minimum Tx PLL Bandwidth for 3-dB Peaking	1.5 (min)	8 (min)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Notes 5 and 7.
$BW_{TX-PLL-LO-1DB}$	Minimum Tx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{TX-PLL1}$	TX PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0 (max)	dB	
$PKG_{TX-PLL2}$	TX PLL peaking with 5-MHz Minimum Bandwidth	Not specified	1.0 (max)	dB	Refer to Note 7.
$RL_{TX-DIFF}$	TX Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	
RL_{TX-CM}	TX Common Mode Return Loss (Package + Silicon)	6 (min)	6 (min)	dB	S_{11} parameter. **2.5 GT/s** – Measured over 0.05- to 1.25-GHz range. **5.0 GT/s** – Measured over 0.05- to 2.5-GHz range.
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80 (min) 120 (max)	120 (max)	Ω	Tx DC Differential mode low impedance. Parameter is captured for 5.0 GHz by $RL_{TX-DIFF}$.
$V_{TX-CM-AC-PP}$	Tx AC Common Mode Voltage (5.0 GT/s)	Not specified	100 (max)	mVPP	Refer to Note 6.
$V_{TX-CM-AC-P}$	Tx AC Common Mode Voltage (2.5 GT/s)	20 (max)	Not specified	mVPP	Refer to Note 6.
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	90 (max)	90 (max)	mA	Total current the Transmitter can provide when shorted to its ground.
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0 (min) 3.6 (max)	0 (min) 3.6 (max)	V	Allowed DC common mode voltage, under any conditions.

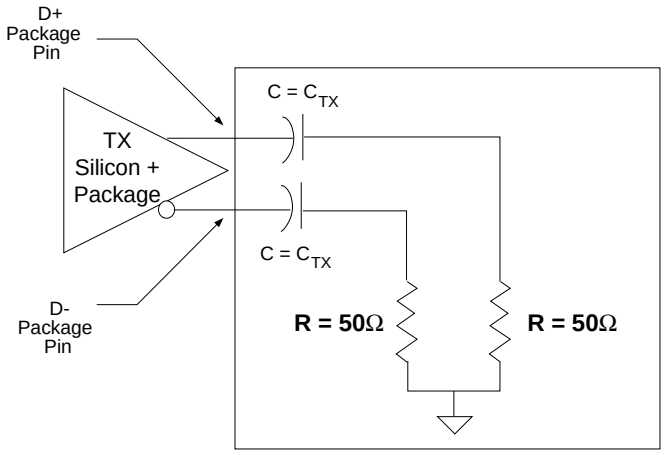
Table 13-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 Link PM state and Electrical Idle	0 (min) 100 (max)	0 (min) 100 (max)	mV	$\lvert V_{TX-CM-DC}$ [during L0] – $V_{TX-CM-Idle-DC}$ [during Electrical Idle]$\rvert \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert$ / 2 [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert$ / 2 [Electrical Idle]
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25 (max)	0 (min) 25 (max)	mV	$\lvert V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\rvert \leq 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\lvert V_{TX-D+}\rvert$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\lvert V_{TX-D-}\rvert$
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0 (min) 20 (max)	0 (min) 20 (max)	mV	$V_{TX-IDLE-DIFFp} = \lvert V_{TX-Idle-D+} - V_{TX-Idle-D-}\rvert \leq 20$ mV Voltage must be high-pass filtered, to remove any DC component.
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Peak Output Voltage	Not specified	0 (min) 5 (max)	mV	$V_{TX-IDLE-DIFF-DC} = \lvert V_{TX-Idle-D+} - V_{TX-Idle-D-}\rvert \leq 5$ mV Voltage must be high-pass filtered, to remove any AC component.
$V_{TX-RCV-DETECT}$	Amount of Voltage Change Allowed during Receiver Detection	600 (max)	600 (max)	mV	Total amount of voltage change that a Transmitter can apply, to sense whether a Low-Impedance Receiver is present.
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	20 (min)	20 (min)	ns	Minimum time a Transmitter must be in Electrical Idle. Used by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle Ordered-Set (EIOS).
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered-Set	8 (max)	8 (max)	ns	After sending the required EIOS, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Tx in Electrical Idle.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum Time to Transition to Valid Differential Signaling after Leaving Electrical Idle	8 (max)	8 (max)	ns	Maximum time to transition to valid differential signaling, after leaving Electrical Idle. This is considered a de-bounce time to the Tx.
$T_{CROSSLINK}$	Cross-Link Random Timeout	1.0 (max)	1.0 (max)	ms	Random timeout that helps resolve potential conflicts in the cross-link configuration.
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	500 ps + 2 UI (max)	500 ps + 4 UI (max)	ps	Static skew between any two Lanes within a single Transmitter.
C_{TX}	AC-Coupling Capacitor	75 (min) 200 (max)	75 (min) 200 (max)	nF	All Transmitters shall be AC-coupled. The AC coupling is required either within the media, or within the transmitting component itself.

Notes:

1. *SSC permits a +0, -5,000 ppm modulation of the clock frequency, at a modulation rate not to exceed 33 kHz.*
2. *Specified at the measurement point into a timing and voltage compliance test load, as illustrated in Figure 13-1.*

Figure 13-1. Compliance Test/Measurement Load



3. *Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurements at 5.0 GT/s must de-convolve effects of the compliance test board, to yield an effective measurement at the Tx balls. 2.5 GT/s can be measured within 200 mils of the Tx device's balls; however, de-convolution is recommended. At least 10^6 UI of data must be acquired.*
4. *Transmitter jitter is measured by driving the Tx under test with a low jitter "ideal" clock and connecting the device under test (DUT) to a reference load.*
5. *The Tx PLL bandwidth must lie between the minimum and maximum ranges listed in Table 13-7. PLL peaking must lie below the values listed in Table 13-7.*

   The PLL bandwidth extends from zero (0) up to the value(s) specified in Table 13-7.
6. *Measurement is made over at least 10^6 UI.*
7. *A single combination of PLL bandwidth and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two 20 combinations of PLL bandwidth and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the maximum PLL bandwidth is 16 MHz.*

Table 13-8. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	UI does not account for variations caused by SSC.
$V_{RX-DIFF-PP-CC}$	Differential Rx Peak-to-Peak Voltage for Common REFCLK Rx Architecture	0.175 (min) 1.2 (max)	0.125 (min) 1.2 (max)	V	$V_{RX-DIFF-PP} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$
T_{RX-EYE}	Receiver Eye Time Opening	0.40 (min)	N/A	UI	Minimum eye time at Rx pins to yield a 10^{-12} Bit Error Rate. Receiver eye margins are defined into a 2 x 50Ω reference load.
$T_{RX-TJ-CC}$	Maximum Rx Inherent Timing Error	N/A	0.40 (max)	UI	Maximum Rx inherent total timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-DJ-DD-CC}$	Maximum Rx Inherent Deterministic Timing Error	N/A	0.30 (max)	UI	Maximum Rx inherent deterministic timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Delta between the Median and Deviation from the Median	0.3 (max)	Not specified	UI	
$T_{RX-MIN-PULSE}$	Minimum Width Pulse at Rx	Not specified	0.6 (min)	UI	Measured to account for worst Tj at 10^{-12} Bit Error Rate.
$V_{RX-MAX-MIN-RATIO}$	Minimum/ Maximum Pulse Voltage on Consecutive UI	Not specified	5 (max)	Ratio	Rx eye must simultaneously meet V_{RX-EYE} limits.
$BW_{RX-PLL-HI}$	Maximum Rx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 2.
$BW_{RX-PLL-LO-3DB}$	Minimum Rx PLL Bandwidth for 3-dB Peaking	1.5 min	8 (min)	MHz	
$BW_{RX-PLL-LO-1DB}$	Minimum Rx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{RX-PLL1}$	Rx PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0	dB	
$PKG_{RX-PLL2}$	Rx PLL Peaking with 5-MHz Minimum Bandwidth	Not specified	1.0	dB	

Table 13-8. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$RL_{RX-DIFF}$	Rx Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	Refer to Note 3.
RL_{RX-CM}	Common Mode Return Loss	6 (min)	6 (min)	dB	Refer to Note 3.
Z_{RX-DC}	Rx DC Single-Ended Impedance	40 (min) 60 (max)	40 (min) 60 (max)	Ω	Required Rx D+ and D- DC impedance (50Ω ±20% tolerance). Refer to Note 4.
$Z_{RX-DIFF-DC}$	DC Differential Rx Impedance	80 (min) 120 (max)	Not specified	Ω	Rx DC Differential mode impedance. Parameter is captured for 5.0 GHz by $RL_{RX-DIFF}$. Refer to Note 4.
$V_{RX-CM-AC-P}$	Rx AC Common Mode Voltage	150 (max)	150 (max)	mVP	Measured at Rx pins, into a pair of 50Ω terminations into Ground. Refer to Note 5.
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input Common Mode Input Impedance for Voltage >0 during Reset or Power-Down	50K (min)	50K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range 0 to 200 mV (with respect to Ground). Refer to Note 6.
$Z_{RX-HIGH-IMP-DC-NEG}$	DC Input Common Mode Input Impedance for Voltage <0 during Reset or Power-Down	1.0K (min)	1.0K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range -150 to 0 mV (with respect to Ground). Refer to Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65 (min) 175 (max)	65 (min) 175 (max)	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the Receiver's package pins.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Idle Detect Threshold Integration Time	10 (max)	10 (max)	ms	An un-expected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Lane-to-Lane Skew	20 (max)	8 (max)	ns	Across all Lanes on a Port. Includes variation in the length of a SKIP Ordered-Set at the Rx, as well as any delay differences arising from the interconnect itself. Refer to Note 7.

Notes:

1. *The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.*

2. *Two combinations of PLL bandwidth and peaking are specified at 5.0 GT/s, to permit designers to make trade-offs between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met.*

   A PLL bandwidth extends from zero up to the value(s) defined as the minimum or maximum in Table 13-8. For 2.5 GT/s, a single PLL bandwidth and peaking value of 1.5 to 22 MHz and 3.0 dB are defined.

3. *Measurements must be made for both common mode and differential return loss. In both cases, the DUT must be powered up and DC-isolated, and its D+/D- inputs must be in the low-Z state.*

4. *The Rx DC single-ended impedance must be present when the Receiver terminations are first enabled, to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately, and the Rx single-ended impedance (constrained by $RL_{RX\text{-}CM}$ to 50Ω ±20%) must be within the specified range by the time Detect is entered.*

5. *Common mode peak voltage is defined by the expression:*

   $max\{|(Vd+ - Vd-) - V\text{-}CMDC|\}$

6. *$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}NEG}$ and $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ are defined, respectively, for negative and positive voltages at the input of the Receiver. Transmitter designers must comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.*

7. *The $L_{RX\text{-}SKEW}$ parameter exists to handle repeaters that re-generate REFCLK and introduce differing numbers of skips on different Lanes.*

Table 13-9. PCI Express Differential Clock Input (Signal Group c) – AC and DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{REFCLK}	Reference Clock Frequency			100	MHz	1
V_{SW}	Differential Voltage Swing (Peak-to-Peak)	125		1,200	mV	
DC_{REFCLK}	Input Clock Duty Cycle	40		60	%	
R_{TERM}	Input Parallel Termination (Differential)		100		Ω	
V_I	Input Voltage Range	-0.3		VDDA	V	
V_{IH}	Input High-Level Voltage	0.3		VDDA	V	
V_{IL}	Input Low-Level Voltage	-0.3		VDDA - 0.30	V	
V_{ID}	Input Differential Voltage	0.2		2.2	V_{PP}	
V_{CM}	Common Mode Voltage	0.25		VDDA - 0.25	V	
Z_{IN}	Differential Input Impedance	80		120	Ω	

Notes:

1. *PEX_REFCLKn/p do not require AC coupling capacitors, when driven from a High-Speed Current Steering Logic (HCSL) source. Use with other Clock driver types (such as LVDS or LVPECL) has not been characterized.*

Table 13-10. PEX_REFCLKOUT – DC Electrical Characteristics

Parameter	Parameter	Min	Typ	Max	Unit	Notes
I_{OH}	Output High-Level Current	11	14	20	mA	
I_{OL}	Output Low-Level Current	-11	-14	-20	mA	
I_{OZH}	Output High Leakage Current	-10	–	10	µA	
I_{OZL}	Output Low Leakage Current	-10	–	10	µA	

Table 13-11. PEX_REFCLKOUT – AC Electrical Characteristics

Parameter	Parameter	Min	Typ	Max	Unit	Notes
V_{OH}	High-Level Output Voltage (Single-Ended)	0.44	0.7 V	1.1	V	
V_{OL}	Low-Level Output Voltage (Single-Ended)	-0.06	0.0 V	0.04	V	
V_{CROSS}	Output Cross-Point Voltage	0.25	0.35	0.55	V	
T_{OR}	Output Rising Edge Rate	0.58	2.5	4.0	V/ns	
T_{OF}	Output Falling Edge Rate	0.58	2.5	4.0	V/ns	
V_{MAX}	Absolute Maximum Output Voltage, Including Overshoot	–	–	1.15	V	
V_{MIN}	Absolute Minimum Output Voltage, Including Undershoot	-0.3	–	–	V	

Chapter 14 Thermal and Mechanical Specifications

14.1 Thermal Characteristics

Table 14-1 lists sample thermal data for the PEX 8605 at Industrial temperature (ambient temperature from -40 to +85°C).

Table 14-1. Sample Thermal Data[a]

Package Type	Θ_{JA} (°C/W)			Psi_{jt}[b] (°C/W)	Θ_{JC} (°C/W)
	0 m/s	1 m/s	2 m/s		
Dual-Row aQFN	27.8	23.0	21.7	0.09	5.3
Exposed Pad TQFP	25.4	20.3	19.1	0.41	10.0

a. Heat flow path (estimated):
- *Heat dissipated from PCB – 80%*
- *Heat dissipated from package top – 8%*
- *Heat dissipated from others – 12%*

b. Junction-to-top-bottom thermal characterization parameter. Used for estimating the junction temperature, by measuring TT in an actual environment.

$Psi_{jt} = (TJ - TT) / PH$

where:

- *TT = Temperature at the bottom-center of the package*
- *PH = Power dissipation*
- *TJ = Junction temperature*

14.2 General Package Specifications

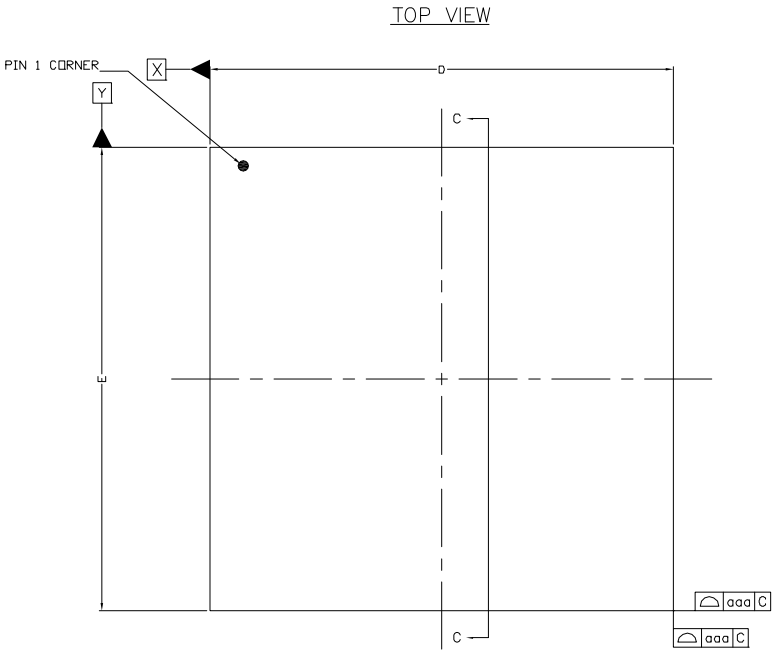
Table 14-2 lists general package specifications. For a more complete list, refer to Figure 14-1 and Figure 14-2.

Table 14-2. General Package Specifications

Parameter	Specification, by Package Type	
	Dual-Row aQFN	Exposed Pad TQFP
Pin Quantity	136 (staggered pins, including un-connected pins)	128
Package Dimensions	10 x 10 mm^2	14 x 14 mm^2
Package Dimensions Overall (includes pins)	–	16 x 16 mm^2
Thermal Ground	4.940 x 4.940 mm^2 ±0.50 mm Center pad	6.600 x 6.350 mm^2 Center pad
Package Height	0.85 mm	1.20 mm
Package Thickness	0.675 mm ±0.35 mm	1.00 mm ±0.05 mm
Ball Pitch	0.50 mm	–
Lead Pitch	–	0.40 mm
Lead Width	–	0.16 mm -0.03/+0.07 mm
Lead Length	–	1.00 mm
Foot Length	–	0.60 mm ±0.15 mm
Foot Angle	–	3.5° ±3.5°

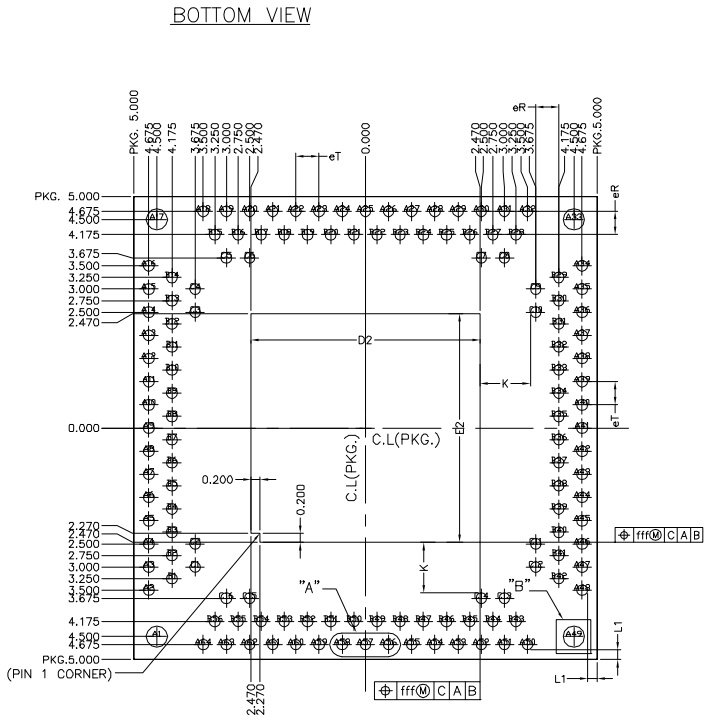
14.3 Mechanical Dimensions

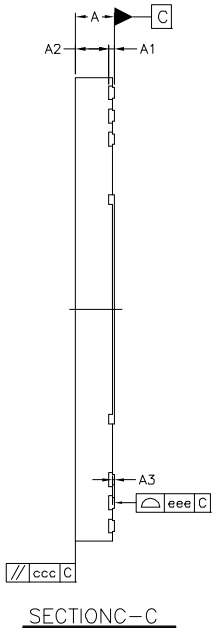
Figure 14-1. Mechanical Dimensions (10 x 10 mm^2 Dual-Row aQFN Package)

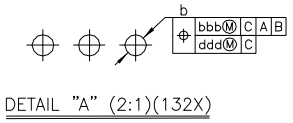


* CONTROLLING DIMENSION : MM

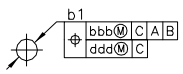
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.85	---	---	0.033
A3	0.020	0.050	0.080	0.0008	0.002	0.003
A2	0.640	0.675	0.710	0.025	0.027	0.028
A1	0.120	0.130	0.140	0.005	0.005	0.006
b	0.180	0.230	0.280	0.007	0.009	0.011
b1	0.410	0.460	0.510	0.016	0.018	0.020
D	10.00 BSC.			0.394 BSC.		
D2	4.890	4.940	4.990	0.193	0.194	0.196
E	10.00 BSC.			0.394 BSC.		
E2	4.890	4.940	4.990	0.193	0.194	0.196
eT	0.500			0.020		
eR	0.500			0.020		
K	1.040	1.090	1.140	0.041	0.043	0.045
L1	0.160	0.210	0.260	0.006	0.008	0.010
TOLERANCES OF FORM AND POSITION						
aaa	0.150			0.006		
bbb	0.100			0.004		
ddd	0.050			0.002		
ccc	0.100			0.004		
eee	0.080			0.003		
fff	0.100			0.004		





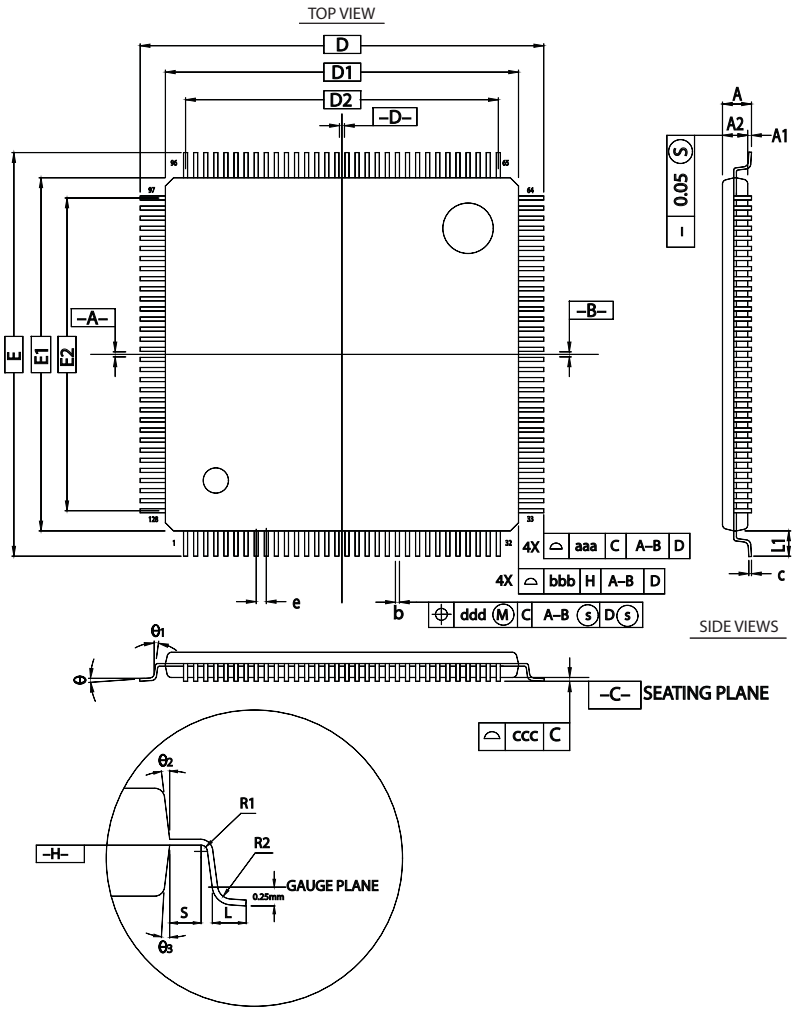


DETAIL "A" (2:1)(132X)



DETAIL "B" (1:1)(4X)

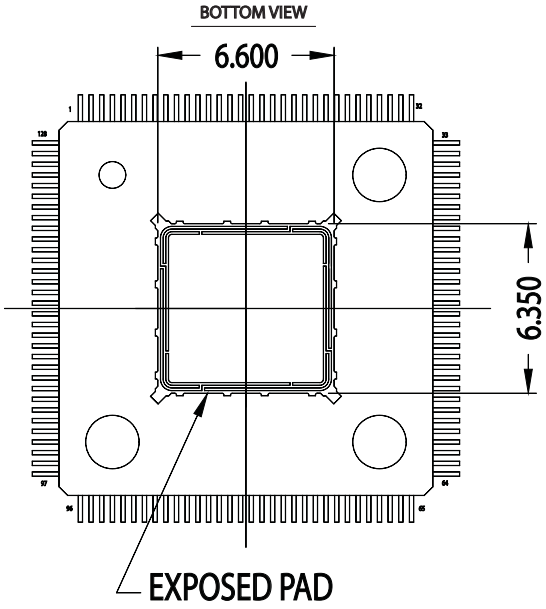
Figure 14-2. Mechanical Dimensions (14 x 14 mm^2 Exposed Pad TQFP Package)



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

Figure 14-2 Mechanical Dimensions (14 x 14 mm^2 Exposed Pad TQFP Package) *(Cont.)*



SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.01575 BSC.		
D_2	12.40			0.488		
E_2	12.40			0.488		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS, INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm.
   DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 mm PITCH PACKAGES.
3. ALL DIMENSIONS OF 128L ARE BASED ON THOSE OF 120L, BECAUSE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

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Appendix A General Information

A.1 Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table A-1. Product Ordering Information

Part Numbers	Description
PEX8605-AB50NI G	PEX 8605 4-Lane, 4-Port PCI Express Gen 2 Switch Dual-Row aQFN (10 x 10 mm^2, 136-pin) Lead-Free, RoHS, and Green Package
PEX8605-AB50TQI G	PEX 8605 4-Lane, 4-Port PCI Express Gen 2 Switch Exposed Pad TQFP (14 x 14 mm^2, 128-pin) Lead-Free, RoHS, and Green Package
where	PEX – PCI Express Product Family 8605 – Part Number AB – Silicon Revision 50 – Signaling Rate (5.0 GT/s) N – Dual-Row aQFN Package TQ – Exposed Pad TQFP Package I – Industrial Temperature G – Lead-Free, ROHS 6/6- and Green-compliant Packaging
PEX8605-AB RDK	PEX 8605 Rapid Development Kit, configured as one x1 upstream Port and three x1 downstream Ports
PEX8605-AB-2U1DRDK	PEX 8605 Rapid Development Kit, configured as one x2 upstream Port and two x1 downstream Ports

A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support, or call 800 759-3735 (domestic only) or 408 774-9060.