

DATA SHEET

AA107-310, AA107-310LF: GaAs IC 5-Bit Digital Attenuator with Serial-to-Parallel Driver 300 kHz–2 GHz

Features

- Positive voltage operation (5 V)
- QFN 5 x 5 mm leadless package
- Integrated silicon serial-to-parallel driver
- Attenuation 0.5 dB steps to 15.5 dB
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

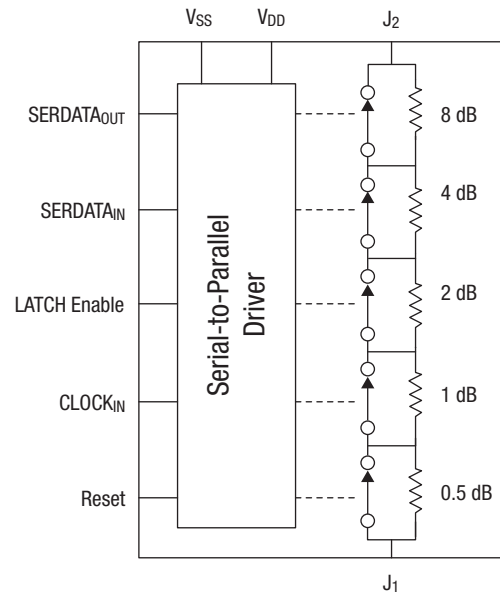
Description

The AA107-310 is a GaAs FET IC 5-bit digital attenuator with a serial-to-parallel driver packaged in a 32-leadless exposed pad plastic package. It is particularly suited at IF frequencies where high attenuation accuracy, low insertion loss, and low intermodulation products are required. Typical applications include base station, wireless and RF data and wireless local loop gain control circuits.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.



QFN 5 x 5 (-310)



Electrical Specifications at 25 °C

V_{DD} = 5 V, Z₀ = 50 Ω, unless otherwise specified

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Insertion loss ⁽¹⁾		300 kHz–1 GHz		1.4	1.7	dB
		300 kHz–2 GHz		1.7	2.2	dB
Attenuation range ^(2, 3)				15.5		dB
Attenuation accuracy ^(2, 3)		300 kHz–1 GHz	± (0.2 + 3% of Attenuation Setting in dB)			dB
		300 kHz–2 GHz	± (0.4 + 3% of Attenuation Setting in dB)			dB
VSWR (I/O)		300 kHz–2 GHz		1.4:1	1.8:1	
Switching characteristics						
Rise, fall	10/90% or 90/10% RF 50% CTL to 90/10% RF T _{RISE} = 1 ns, BW = 500 MHz			50		ns
On, off				100		ns
Video feedthru				50		mV
Input power for 1 dB compression		0.5–2 GHz	24	29		dBm
		0.05 GHz	15	22		dBm
Intermodulation intercept point (IP3)	For two-tone input power 5 dBm each tone	0.5–2 GHz	44	50		dBm
		0.05 GHz	26	40		dBm

1. Insertion loss changes by 0.003 dB/°C.

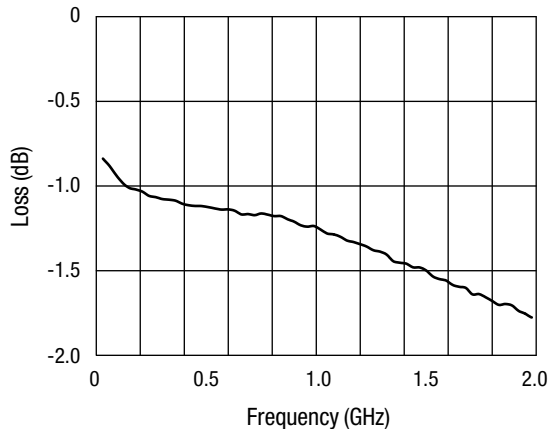
2. Attenuation value referenced above insertion loss.

3. Exposed pad must be connected to RF ground to obtain specified attenuation.

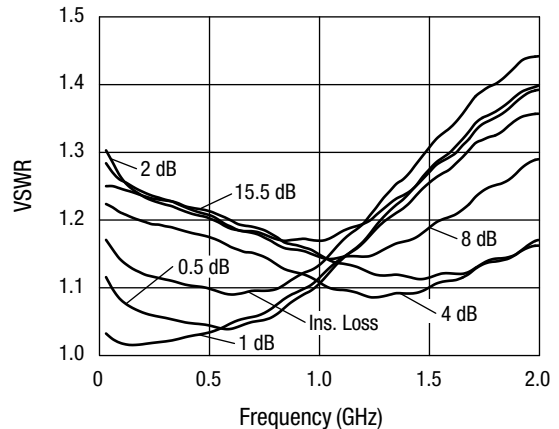
DC Electrical Characteristics at 25 °C (V_{DD} = 5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage high	V _{IH} (1)	1.7	3.5	5	V
Input voltage low	V _{IL} (0)	0	0.3	0.6	V
Input Leakage current	I _L		±0.5		μA
Quiescent current	I _{DD}		500		μA
Supply voltages	V _{DD}		5		V

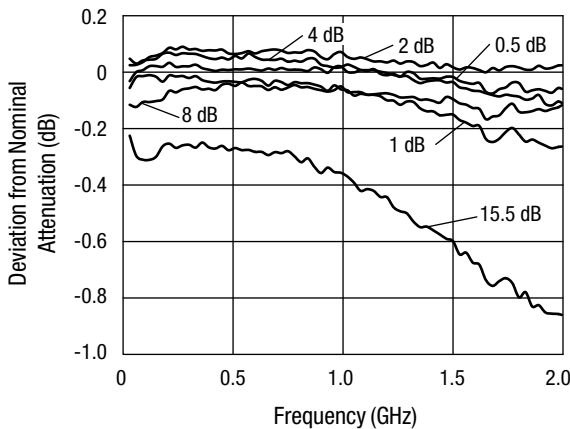
Typical Performance Data (V_{DD} = 5 V)



Insertion Loss vs. Frequency



VSWR vs. Frequency



Attenuation Accuracy vs. Frequency

Absolute Maximum Ratings

Characteristic	Value
Supply voltage (V _{DD})	-0.5 to +6 V
Input voltage (V _i)	-0.5 - V _{CC} + 0.5 V
Power dissipation (P _D)	500 mW
Storage temperature (T _{ST})	-65 °C to +150 °C
Operating temperature (T _{OP})	-40 °C to +85 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Truth Table

Reset	Serial Data Input					J ₁ -J ₂ Attenuation
	0.5 dB	1 dB	2 dB	4 dB	8 dB	
1	0	0	0	0	0	Insertion loss
1	1	0	0	0	0	0.5 dB
1	0	1	0	0	0	1 dB
1	0	0	1	0	0	2 dB
1	0	0	0	1	0	4 dB
1	0	0	0	0	1	8 dB
1	1	1	1	1	1	15.5 dB
0	X	X	X	X	X	Insertion loss

V_{IL} (0) = 0 to 0.5 V.
 V_{IH} (1) = 3.5 to 5 V.
 X = Don't Care.

Recommended Solder Reflow Profiles

Refer to the [“Recommended Solder Reflow Profile”](#) Application Note.

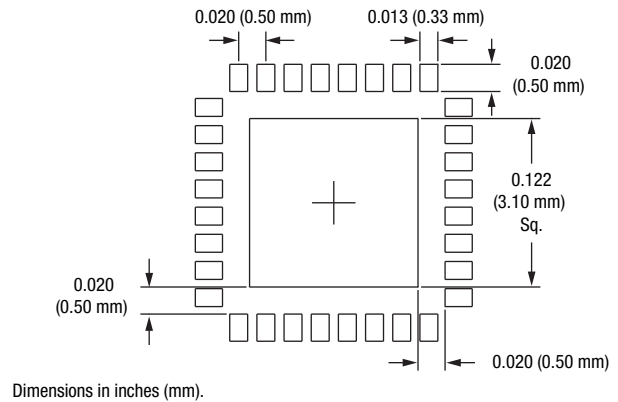
Tape and Reel Information

Refer to the [“Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation”](#) Application Note.

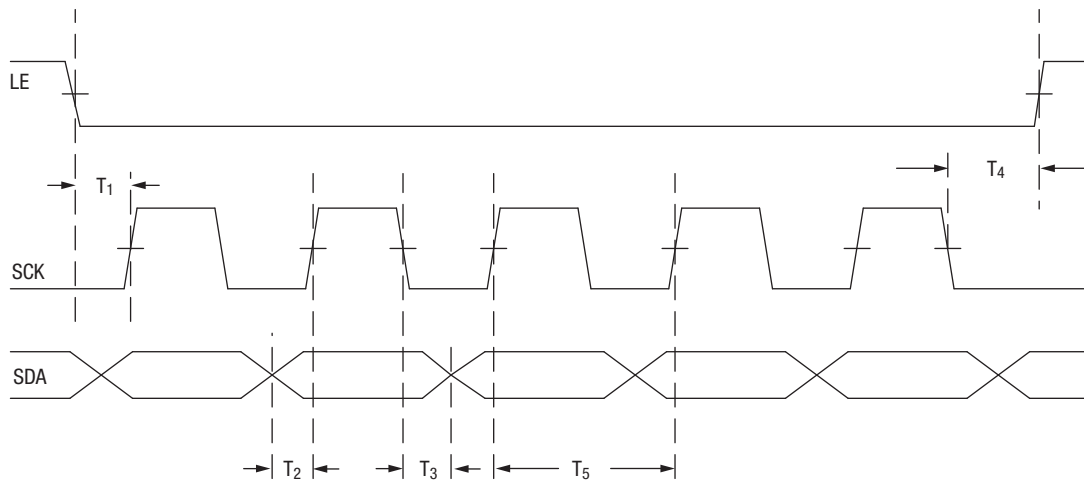
Pin	Symbol	Function
1	Serial data out	Serial data output
2-4	GND	Ground
5	J ₁	RF input/output
6-19	GND	Ground
20	J ₂	RF input/output
21-23	GND	Ground
24	RESET	Reset
25	LE	Latch enable
26	Serial data in	Serial data input
27	Clock In	Serial clock input
28	V _{SS}	Low output voltage level
29	GND	Ground
30	C ₂	Charge pump capacitor
31	C ₁	Charge pump capacitor
32	V _{DD}	Supply voltage

Surface Mount Land Pattern

5 x 5 mm QFN 32-Lead



Timing Diagram



Parameter	Symbol	Min.	Typ.	Max.	Unit
LE setup time	T ₁	7.5	15		ns
SDA setup time	T ₂	7.5	15		ns
SDA hold time	T ₃	5	10		ns
LE hold time	T ₄	5	10		ns
Clock frequency	f _{CLK}		16	100	MHz
Clock period	T ₅		1/f _{CLK}		

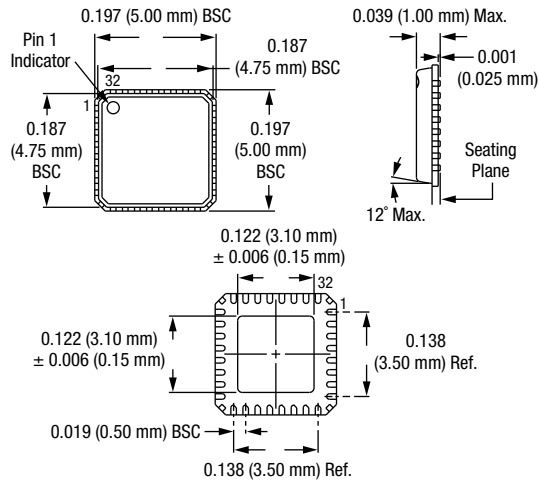
Serial data (SDA) is shifted into the register on the rising edge of the clock (SCK), least significant bit (LSB) first. The attenuator will change states on the rising edge of the latch-enable (LE) signal, according to the most recent 5 bits of shifted data accepted since the previous falling edge of the LE signal.

Power-up sequence:

0. Connect ground
1. Apply V_{DD}
2. Set all inputs (SCK, SDA, LE)

Power-down sequence should be the reverse of above.

QFN 5 x 5 (-310)



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