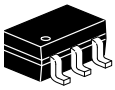
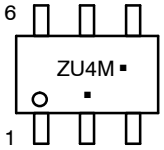
TinyLogic UHS Dual Unbuffered Inverter

NC7WZU04A



SC−88
CASE 419B−02

MARKING DIAGRAMS



BZU4 = Specific Device Code
M = Data Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

Description

The NC7WZU04A is a dual unbuffered inverter from **onsemi**'s Ultra High Speed Series of TinyLogic in the space saving SC−88 6−lead package. The special purpose unbuffered circuit design is intended for crystal oscillator or analog applications. The internal circuit consists of only one−stage, the output, to allow for this part to be used in these oscillator or analog applications. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage.

Features

- Space−Saving SC−88 6−Lead Package
- Unbuffered for Crystal Oscillator and Analog Applications
- Balanced Output Drive: ±8 mA at 4.5 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Low Quiescent Power: I_{CC} < 1 μA at 5 V V_{CC}, T_A = 25°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

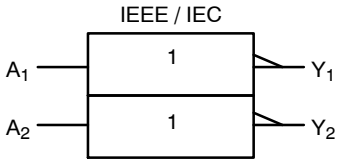


Figure 1. Logic Symbol

Pin Configurations

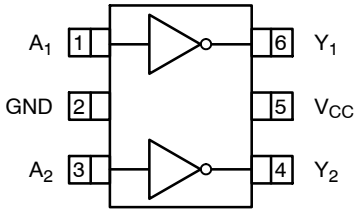
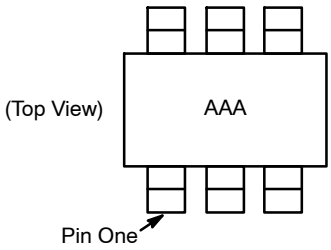


Figure 2. SC−88 (Top View)



AAA represents Product Code Top Mark − see ordering code

NOTE: Orientation of Top Mark determines Pin One location. Reading the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. SC−88 Pin 1 Orientation

PIN DEFINITIONS

Pin Name	Description
A_1, A_2	Data Inputs
Y_1, Y_2	Outputs

FUNCTION TABLE ($Y = \overline{A}$)

Input	Output
A	**Y**
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	−	−50	mA
		V_{OUT} > V_{CC}	−	+50	mA
I_{OUT}	DC Output Current		−	±50	mA
I_{CC} or I_{GND}	DC V_{CC} / GND Current		−	±50	mA
T_{STG}	Storage Temperature		−65	+150	°C
T_J	Junction Temperature Under Bias		−	150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		−	260	°C
P_D	Power Dissipation in Still Air	SC−88	−	332	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
θ_{JA}	Thermal Resistance	SC−88	−	377	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

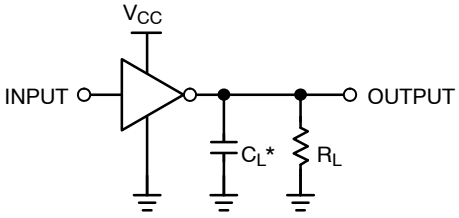
Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = −40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	1.8 to 2.7			0.85 V_{CC}	–	–	0.85 V_{CC}	–	V
		3.0 to 5.5			0.8 V_{CC}	–	–	0.8 V_{CC}	–	
V_{IL}	LOW Level Input Voltage	1.8 to 2.7			–	–	0.15 V_{CC}	–	0.15 V_{CC}	V
		3.0 to 5.5			–	–	0.2 V_{CC}	–	0.2 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IL}	I_{OH} = −100 μA	1.55	1.65	–	1.55	–	V
		1.8			1.6	1.79	–	1.6	–	
		2.3			2.1	2.29	–	2.1	–	
		3.0			2.7	2.99	–	2.7	–	
		4.5			4.0	4.48	–	4.0	–	
		1.65	V_{IN} = GND	I_{OH} = −2 mA	1.29	1.52	–	1.29	–	V
		2.3		I_{OH} = −2 mA	1.9	2.19	–	1.9	–	
		3.0		I_{OH} = −4 mA	2.4	2.82	–	2.4	–	
		3.0		I_{OH} = −6 mA	2.3	2.73	–	2.3	–	
		4.5		I_{OH} = −8 mA	3.8	4.24	–	3.8	–	
VOL	LOW Level Output Voltage	1.65	V_{IN} = V_{IH}	I_{OL} = 100 μA	–	0.01	0.2	–	0.2	V
		1.8			–	0.01	0.2	–	0.2	
		2.3			–	0.01	0.2	–	0.2	
		3.0			–	0.01	0.3	–	0.3	
		4.5			–	0.01	0.5	–	0.5	
		1.65	V_{IN} = V_{CC}	I_{OL} = 2 mA	–	0.10	0.24	–	0.24	V
		2.3		I_{OL} = 2 mA	–	0.12	0.3	–	0.3	
		3.0		I_{OL} = 4 mA	–	0.19	0.4	–	0.4	
		3.0		I_{OL} = 6 mA	–	0.29	0.55	–	0.55	
		4.5		I_{OL} = 8 mA	–	0.29	0.55	–	0.55	
I_{IN}	Input Leakage Current	1.65 to 5.5	V_{IN} = 5.5 V, GND		–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.5	V_{IN} = 5.5 V, GND		–	–	1.0	–	10	μA
I_{CCPEAK}	Peak Supply Current in Analog Operation	1.8	V_{OUT} = Open V_{IN} = Adjust for Peak I_{CC} Current		–	0.2	–	–	–	mA
		2.5			–	2	–	–	–	
		3.3			–	5	–	–	–	
		5.0			–	15	–	–	–	

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 4, 5)	1.65	C_L = 15 pF, R_L = 1 MΩ	–	5.5	9.8	–	11.0	ns
		1.8		–	4.6	8.1	–	8.9	
		2.5 ±0.2		–	3.3	5.7	–	6.3	
		3.3 ±0.3		–	2.7	4.1	–	4.5	
		5.0 ±0.5		–	2.2	3.3	–	3.6	
		3.3 ±0.3	C_L = 50 pF, R_L = 500 Ω	–	4.0	6.4	–	7.0	
		5.0 ±0.5		–	3.4	5.6	–	6.2	
C_{IN}	Input Capacitance	0		–	3	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Figure 6)	3.3	(Note 2)	–	3.5	–	–	–	pF
		5.0		–	5.5	–	–	–	

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



*C_L includes load and stray capacitance.
Input PRR = 1.0 MHz, t_W = 500 ns.

Figure 4. AC Test Circuit

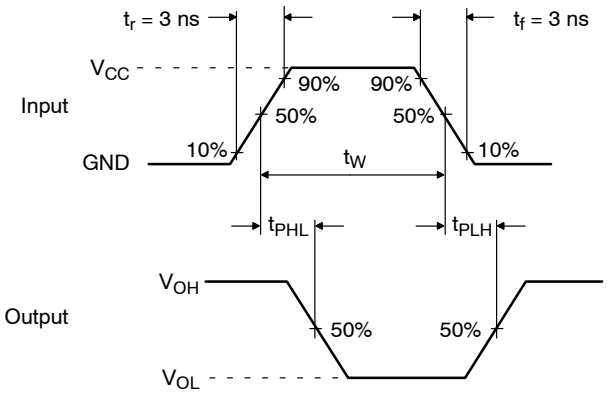
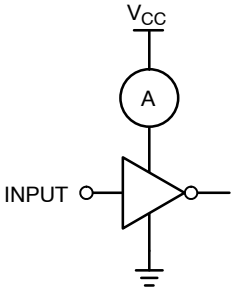


Figure 5. AC Waveforms



Application Note: When operating the NC7WZU04A's unbuffered output stage in its linear range, as in oscillator applications, care must be taken to observe maximum power rating for the device and package. The high drive nature of the design of the output stage will result in substantial simultaneous conduction currents when the stage is in the linear region. See the I_{CCPEAK} specification on page NO TAG.

Input = AC Waveform; $t_r = t_f$ = 1.8 ns.
PRR = 10 MHz; Duty Cycle = 50%.

Figure 6. I_{CCD} Test Circuit

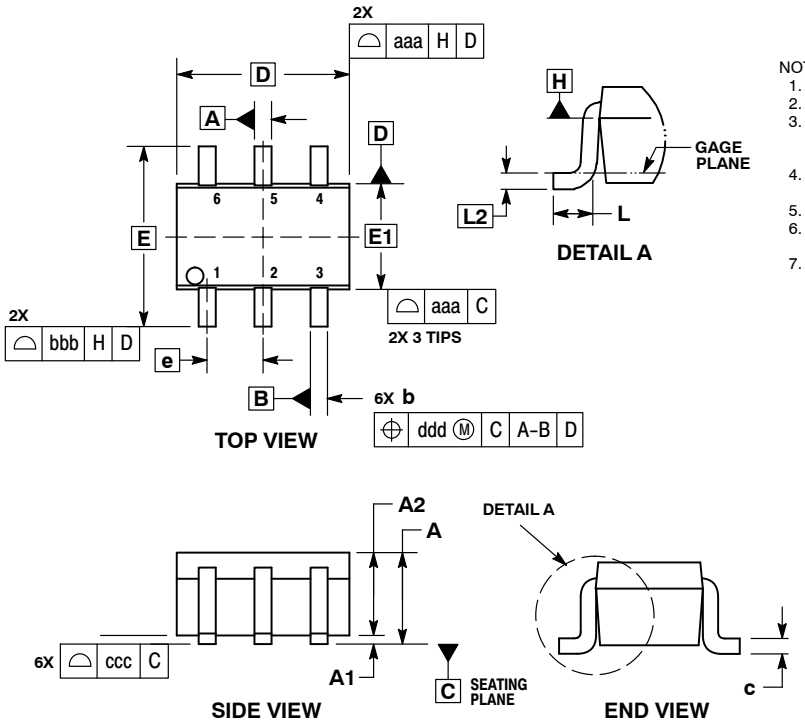
DEVICE ORDERING INFORMATION

Device	Top Mark	Packages	Shipping†
NC7WZU04AP6X	ZU4	SC−88	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

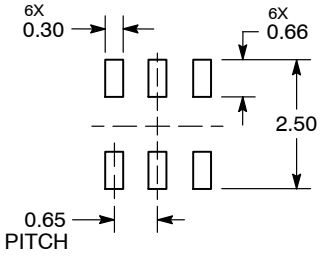
SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−−	−−−	1.10	−−−	−−−	0.043
A1	0.00	−−−	0.10	0.000	−−−	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales