1.7 V to 5.5 V, 3 A Load Switch with Negative V_{IN} Tolerance

DESCRIPTION

The SiP32448 and SiP32449 are low resistance slew rate controlled load switches. The part operates from 1.7 V to 5.5 V supply and can tolerate negative voltage at input to -2 V. The integrated charge pump drivers enable the part with low on resistance over the wide input voltage range.

Both SiP32448 and SiP32449 feature a controlled soft-on slew rate of typical 2.5 ms that limits the inrush current for designs of heavy capacitive load and minimizes the resulting voltage droop at the power rails.

The SiP32448 and SiP32449 feature a constant low voltage control logic interface over the full operation voltage range. It can interface with low voltage control signals without extra level shifting circuit. When EN is left open, the part will not turn on until V_{IN} is greater than 2.5 V.

The SiP32449 has a output discharge to help discharge the output capacitor during shutdown mode for fast turn off.

The SiP32448 and SiP32449 have exceptionally low shutdown current and provides reverse blocking to prevent high current flowing into the power source when the switch is off or V_{IN} is ground.

Both SiP32448 and SiP32449 are available in TDFN4 package of 1.2 mm x 1.6 mm x 0.55 mm.

FEATURES

Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

- 1.7 V to 5.5 V input voltage range
- Negative input voltage tolerance down to -2 V
- 38 mΩ typical R_{ON} from 1.8 V to 5 V
- 3 A maximum continuous switch current
- Slew rate controlled turn-on: 2.5 ms at 3.6 V
- Constant low control logic: V_{IH} = 1.15 V, V_{IL} = 0.7 V
- 2 V UVLO when EN is open
- Reverse current blocking when switch is off or V_{IN} is ground
- Output discharge (SiP32449)
- ESD protected
  - HBM: >6 kV
  - MM: >300 V
  - IEC61000-4-2 air discharge: >15 kV
  - IEC61000-4-2 contact discharge: >8 kV
- Compact TDFN4 package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- PDAs / smart phones
- Notebook / netbook computers
- Tablet PC
- Portable media players
- Digital camera
- GPS navigation devices
- Data storage devices
- Optical, industrial, medical, and healthcare devices

TYPICAL APPLICATION CIRCUIT

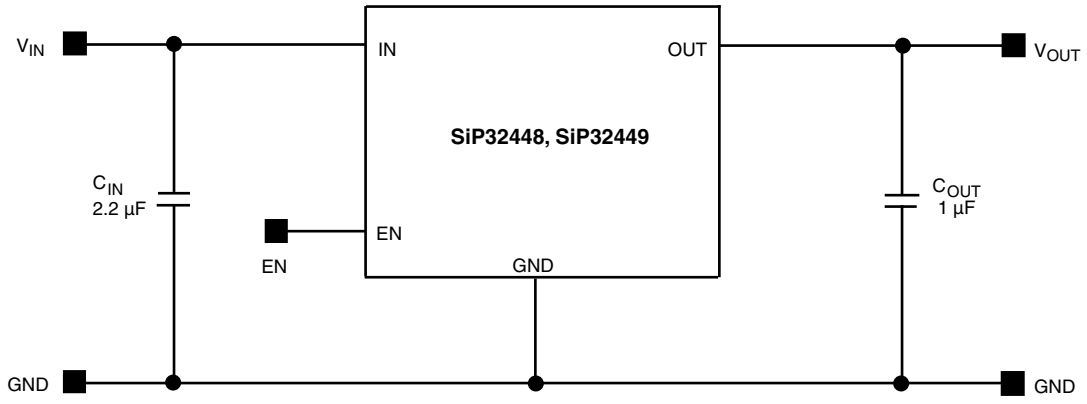


Fig. 1 - SiP32448, SiP32449 Typical Application Circuit

ORDERING INFORMATION

Part Number	Package	Marking	Output Discharge	Temperature Range
SiP32448DNP-T1-GE4	TDFN4 1.2 mm x 1.6 mm	Lx	No	-40 °C to +85 °C
SiP32449DNP-T1-GE4		Px	Yes	

Notes

- x = Lot code
- GE4 denotes halogen-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Supply Input Voltage (V_{IN})		-2 to +6	V
Enable Input Voltage (V_{EN})		-2 to +6	
Output Voltage (V_{OUT})		-0.3 to +6	
Maximum Continuous Switch Current ($I_{max.}$) [c]		4	A
Maximum Repetitive Pulsed Current (1 ms, 10 % Duty Cycle) [c]		7	
Maximum Non-Repetitive Pulsed Current (100 µs, EN = Active) [c]		12	
Junction Temperature (T_J)		-40 to +150	°C
Thermal Resistance (q_{JA}) [a]		170	°C/W
Power Dissipation (P_D) [a,b]		735	mW
ESD Rating	HBM	6	kV
	MM	300	V
	IEC41000-4-2 Air Discharge [d]	15	kV
	IEC41000-4-2 Contact Discharge [d]	8	

Notes

a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout.
b. Derate 5.9 mW/°C above T_A = 25 °C, see PCB layout.
c. T_A = 25 °C, see PCB layout.
d. Tested on V_{IN} with 2.2 µF C_{IN}. V_{IN} connected to micro-USB connector.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage Range (V_{IN})	1.7 to 5.5	V
Operating Junction Temperature Range (T_J)	-40 to +125	°C

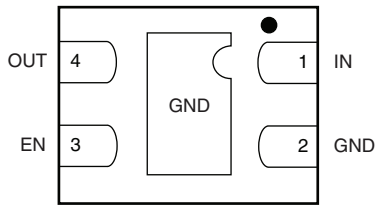
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 5 V, T_A = -40 °C to +85 °C (Typical values are at T_A = 25 °C)	Limits -40 °C to +85 °C			Unit
			Min. [a]	Typ. [b]	Max. [a]	
Operating Voltage [c]	V_{IN}		1.7	-	5.5	V
Negative Input Voltage Tolerance	I_{NEG}	V_{IN} = -2 V	-	-15	-	mA
Under Voltage Lock Out	$UVLO_{H-L}$	EN = open, 25 °C (switch On to Off)	-	-	2	V
	$UVLO_{L-H}$	EN = open, 25 °C (switch Off to On)	2.5	-	-	
UVLO Hysteresis	$UVLO_{HYS}$	EN = open, 25 °C	-	0.25	-	
Quiescent Current	I_Q	V_{IN} = 1.8 V, EN = active	-	35	50	µA
		V_{IN} = 2.5 V, EN = active	-	54	90	
		V_{IN} = 3.6 V, EN = active	-	78	110	
		V_{IN} = 4.3 V, EN = active	-	93	130	
		V_{IN} = 5 V, EN = active	-	110	180	
Off Supply Current	$I_{Q(off)}$	EN = inactive, OUT = open	-	8	18	
Off Switch Current	$I_{DS(off)}$	EN = inactive, OUT = GND	-	-	1	
Reverse Blocking Current	I_{RB}	V_{OUT} = 5 V, V_{IN} = 0 V, V_{EN} = inactive	-	-	10	
On-Resistance	$R_{DS(on)}$	V_{IN} = 1.8 V, I_L = 500 mA, T_A = 25 °C	-	38	43	mΩ
		V_{IN} = 2.5 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
		V_{IN} = 3.6 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
		V_{IN} = 4.3 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
		V_{IN} = 5 V, I_L = 500 mA, T_A = 25 °C	-	38	43	
On-Resistance Temp.-Coefficient	TC_{RDS}		-	3100	-	ppm/°C
EN Input Low Voltage [c]	V_{IL}	V_{IN} = 1.8 V to 5.5 V	-	-	0.7 [d]	V
EN Input High Voltage [c]	V_{IH}		1.15 [d]	-	-	
EN Input Leakage	I_{SINK}	V_{EN} = 5.5 V	-6	-	6	µA
Output Pulldown Resistance	R_{PD}	EN = inactive, T_A = 25 °C (for SiP32449 only)	-	210	280	Ω
Output Turn-On Delay Time	$t_{d(on)}$	V_{IN} = 3.6 V, R_{load} = 10 Ω, T_A = 25 °C	-	1.35	-	ms
Output Turn-On Rise Time	$t_{(on)}$		1	1.7	3.8	
Output Turn-Off Delay Time	$t_{d(off)}$		-	-	0.005	

Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. For V_{IN} outside this range consult typical EN threshold curve.
d. Not tested, guarantee by design.

PIN CONFIGURATION



Bottom View

Fig. 2 - TDFN4 1.2 mm x 1.6 mm Package

PIN DESCRIPTION

Pin Number	Name	Function
1	IN	This is the input pin of the switch
2	GND	Ground connection
3	EN	Enable input
4	OUT	This is the output pin of the switch

BLOCK DIAGRAM

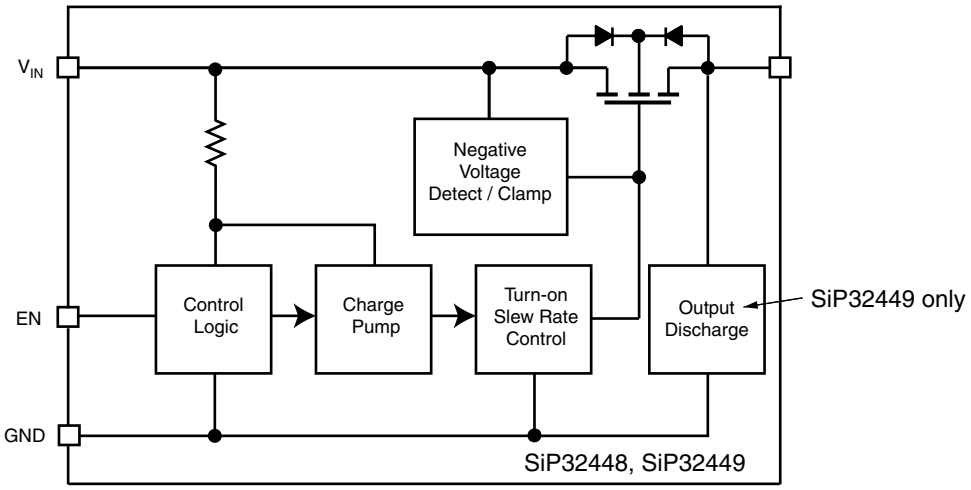


Fig. 3 - Functional Block Diagram

DETAILED DESCRIPTION

SiP32448 and SiP32449 are advanced slew rate controlled high side load switches with an integrated N-channel power switch. When the device is enabled the gate of the power switch is turned on at a controlled rate to avoid excessive inrush current. Once fully on the gate to source voltage of the power switch is biased at a constant level. The design gives a flat on resistance throughout the operating voltages. A special reverse blocking circuitry prevents current flowing from output to input when the switch is off. The V_{IN} and EN pin can tolerate -2 V voltage without drawing excessive current.

APPLICATION INFORMATION

Input Capacitor

In general, under steady state conditions the SiP32448 and SiP32449 do not require an input capacitor. Nevertheless, an input bypass capacitor is recommended in order to reduce the input voltage drop caused by transient inrush currents. Commonly, a 2.2 µF ceramic capacitor is sufficient and should be placed in close proximity to V_{IN} and GND pins. A higher value input capacitor can help to further reduce the voltage drop. Ceramic capacitors are recommended for their low ESR characteristic.

Output Capacitor

While these devices work without an output capacitor, a 1 µF or higher value capacitor across V_{OUT} and GND is recommended in order to handle potential load transient conditions. In the event that the switch is turning of while running high current, circuit stray inductances might force the output to some negative voltage in order to mitigate this phenomenon a proper output capacitor is required.

Enable

The device is logic high active. Enable pin voltage can exceed V_{IN} as long as it is within the absolute maximum rating range. The EN pin is compatible with both TTL and CMOS logic voltage levels. The part features a constant control logic threshold over the operation voltage range. When enable pin is left open, a built-in voltage divider sets the internal logic. The switch will turn on when the V_{IN} exceeds the UVLO trip point.

Reverse Voltage Protection

The SiP32448 and SiP32449 contain a reverse blocking circuitry to protect the current from going to the input from the output when the switch is off. Reverse blocking works for input voltage as low as 0 V.
In case the EN pin is left open, the reverse blocking circuitry will prevents current flow from output pin to input pin if the output voltage is higher by at least 1 V than the input voltage.

THERMAL CONSIDERATIONS

The maximum allowed DC Current depends on the thermal condition in which the device operates. In order to calculate max allowed DC current, first the max power dissipation should be considered.

The SiP32448 and SiP32449 are packaged in a TDFN4 1.2 mm x 1.6 mm package which has a thermal resistance of $\theta_{J\text{-}A}{}^{a} = 170$ °C/W.

Note

a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout. For any other layout configuration the actual junction to ambient thermal impedance should be considered

The following formula shows the maximum allowed power dissipation as a function of the ambient temperature T_A when the maximum junction temperature is limited to $T_{J\,(max.)} = 125$ °C:

$$P_{max.} = \frac{T_{J\,(max.)} - T_A}{\theta_{J\text{-}A}} = \frac{125 - T_A}{170}$$

For example at ambient temperature of 70 °C, the maximum power dissipation will be limited to about 324 mW.

In order to calculate the maximum allowed DC current the switch $R_{DS(on)}$ temperature dependency should be considered.

As an example let us calculate maximum load current at T_A = 70 °C and input voltage of 1.8 V. At this input voltage the $R_{DS(on)}$ at 25 °C 43 mΩ (see specification table). The $R_{DS(on)}$ at 125 °C can be extrapolated from this data using the following formula:

$$R_{DS(on)\_125\ °C} = R_{DS(on)\_25\ °C} \times (1 + T_C \times (T_{J\ max.} - 25)/100)$$

Where T_C is the $R_{DS(on)}$ temperature coefficient expressed in percent change per degree C.

For SiP32448 the approximated value is 0.31 %/°C. $T_{J\ max.}$ is the maximum allowed junction temperature (125 °C).

Therefore,

$$R_{DS(on)\ (at\ 125\ °C)} = 43\ m\Omega \times (1 + 0.31 \times (125 - 25)/100) \approx 57\ m\Omega$$

The maximum current limit is then determined by

$$I_{LOAD}\ (max.) < \sqrt{\frac{P\ (max.)}{R_{DS(on)}}}$$

Which in this case is 2.38 A.

Due to device limitation the max switch DC current should exceed 3 A in any condition.

To obtain the highest power dissipation the power pad of the device should be connected to a heat sink on the printed circuit board. Figure 4 shows a typical PCB layout. All copper traces and vias for the V_{IN} and V_{OUT} pins should be sized adequately to carry the maximum continuous current.

TYPICAL APPLICATION SCHEMATIC

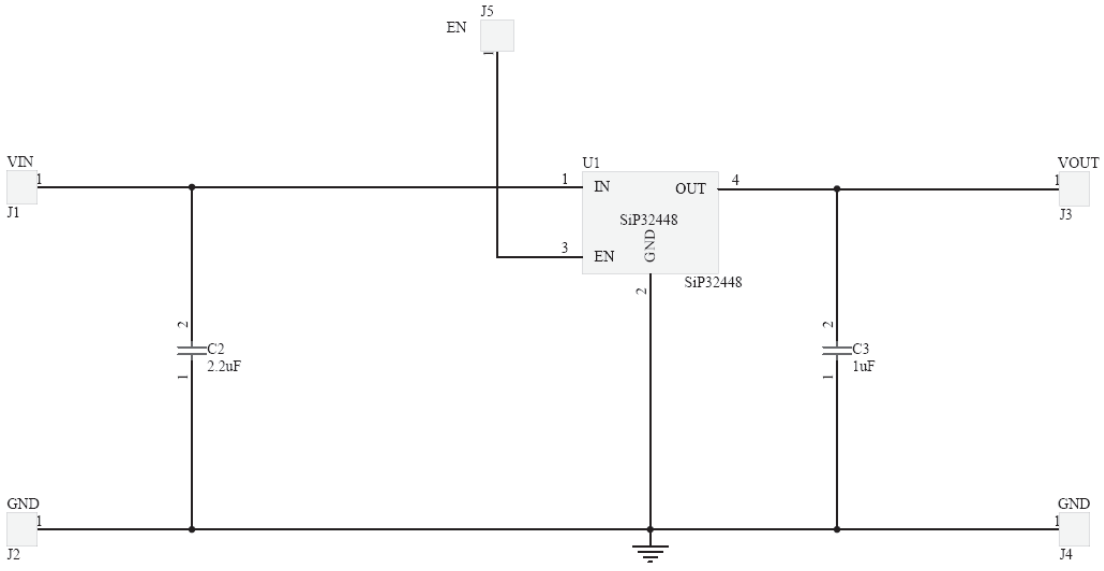


Fig. 5 - Application Schematic

Negative Input Voltage

The SiP32448 and SiP32449 can withstand maximum negative 2 V at its input due to any spike from abnormal or fault condition of the system.

Recommended Board Layout

For improved performance, all traces should be as short as possible to minimize stray inductances and parasitic effects. The input and output capacitors should be kept as close as possible to the input and output pins respectively. Connecting the central exposed pad to GND, using wide traces for input, output, and GND help reducing the case to ambient thermal impedance. See fig. 4.

BOARD LAYOUT

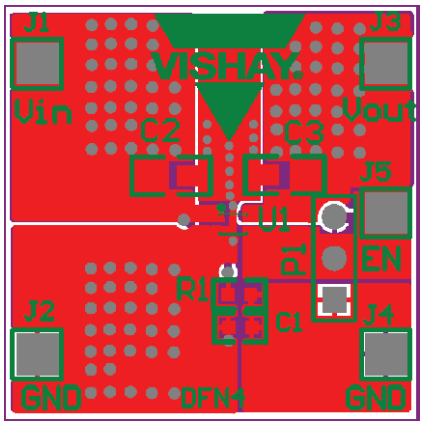
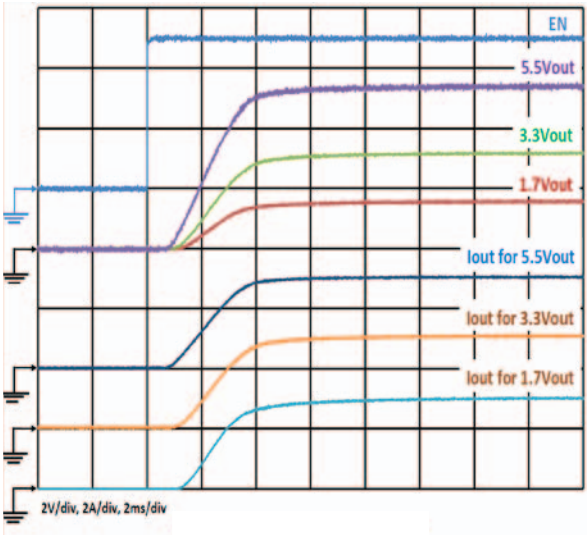
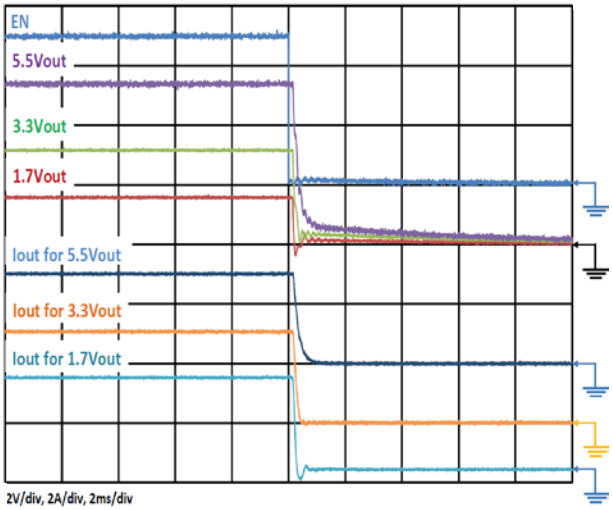


Fig. 4 - Recommended Board Layout

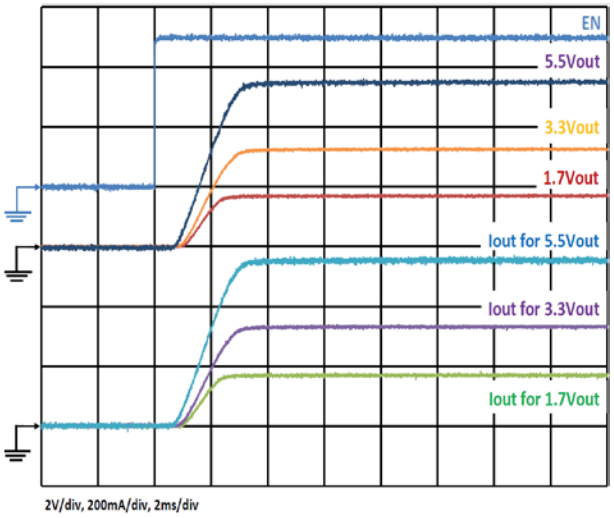
TYPICAL ENABLE POWER ON AND OFF WAVEFORMS



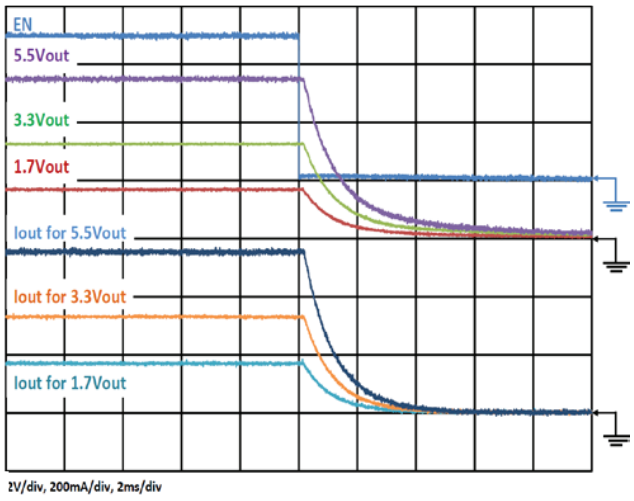
Typical Turn-On Delay, Rise Time,
C_{OUT} = 1 µF, C_{IN} = 2.2 µF, I_{OUT} = 3 A



Typical Turn-Off Delay, Fall Time,
C_{OUT} = 1 µF, C_{IN} = 2.2 µF, I_{OUT} = 3 A



Typical Turn-On Delay, Rise Time,
C_{OUT} = 1 µF, C_{IN} = 2.2 µF, R_{OUT} = 10 Ω



Typical Turn-Off Delay, Fall Time,
C_{OUT} = 1 µF, C_{IN} = 2.2 µF, R_{OUT} = 10 Ω

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

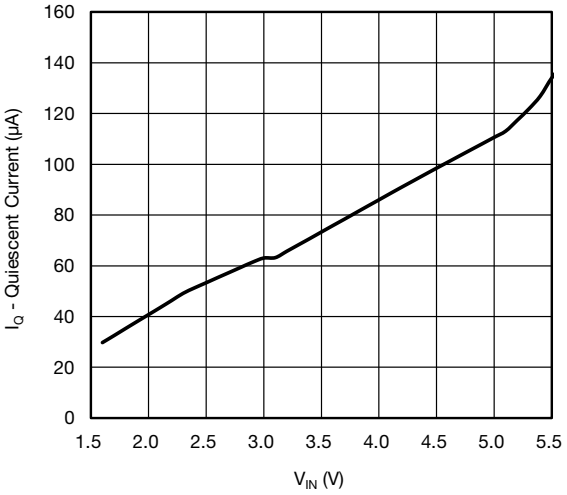


Fig. 6 - Quiescent Current vs. Input Voltage

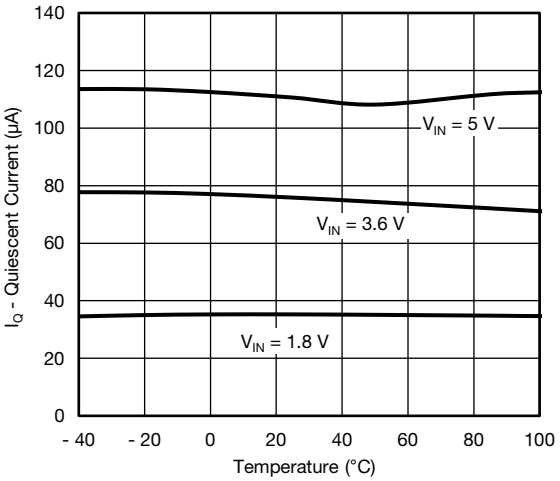


Fig. 9 - Quiescent Current vs. Temperature

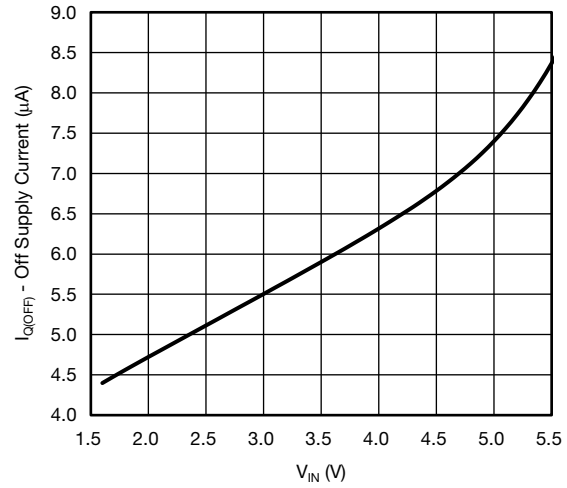


Fig. 7 - Off Supply Current vs. Input Voltage

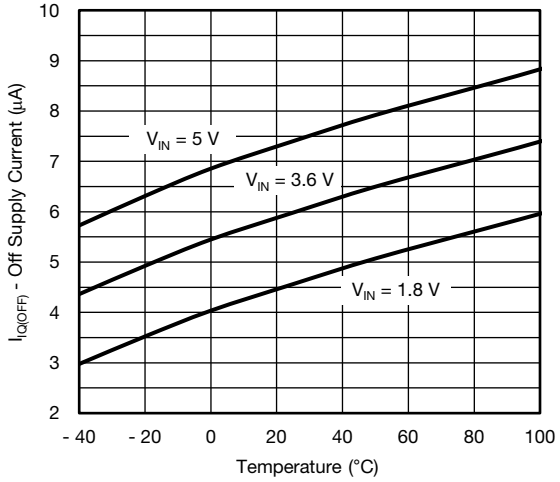


Fig. 10 - Off Supply Current vs. Temperature

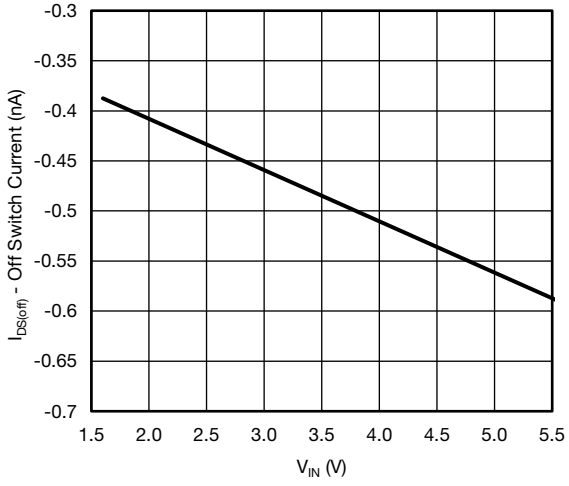


Fig. 8 - Off Switch Current vs. Input Voltage

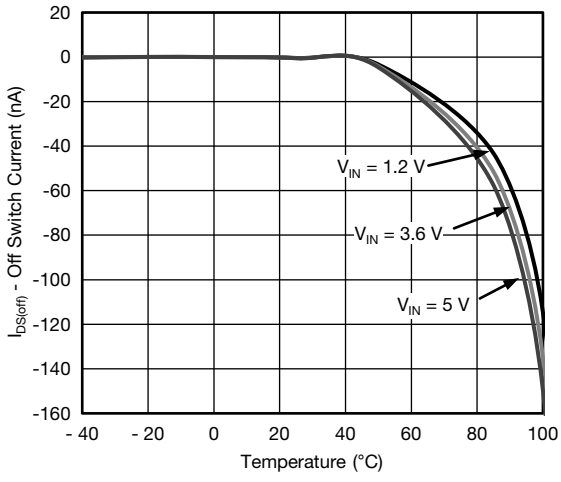


Fig. 11 - Off Switch Current vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

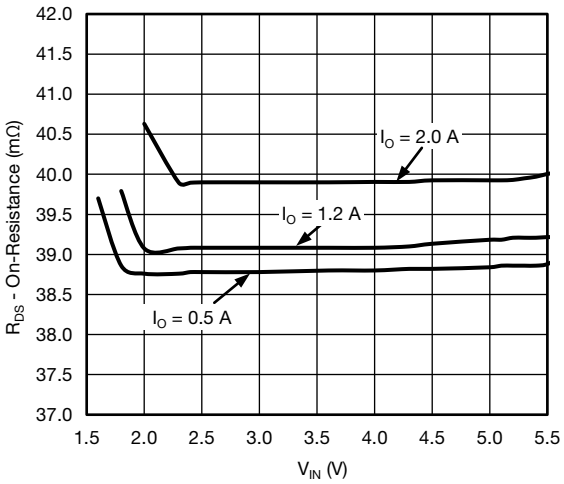


Fig. 12 - On-Resistance vs. Input Voltage

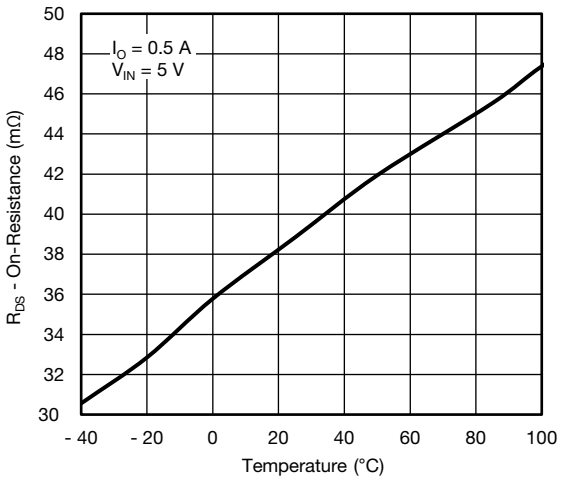


Fig. 15 - On-Resistance vs. Temperature

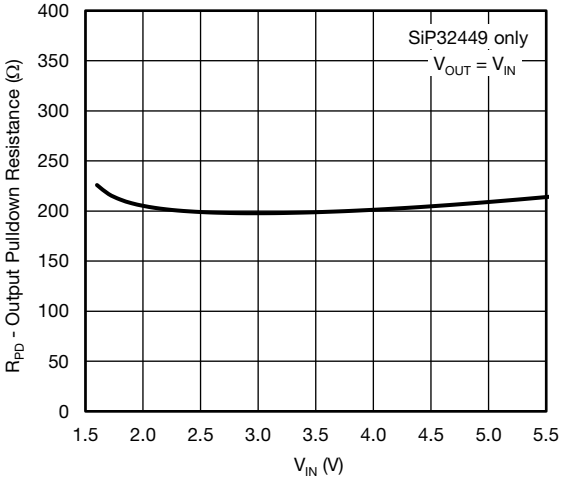


Fig. 13 - Output Pulldown Resistance vs. V_{IN}

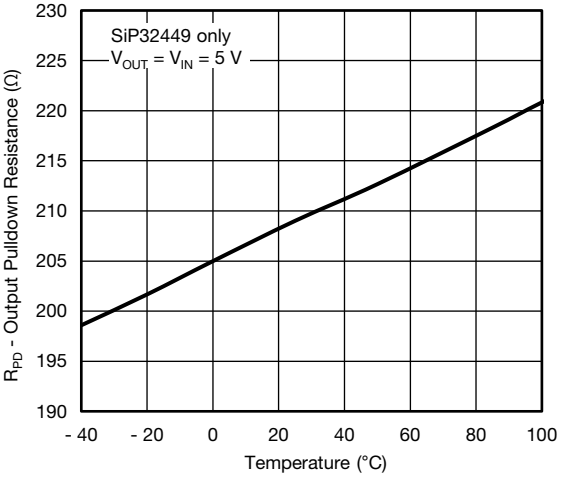


Fig. 16 - Output Pulldown Resistance vs. Temperature

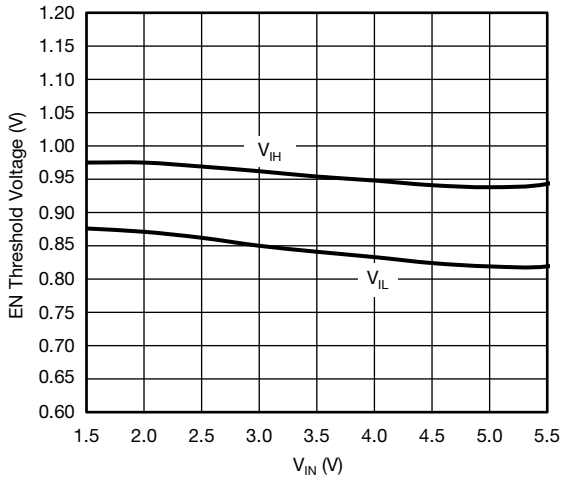


Fig. 14 - Threshold Voltage vs. Input Voltage

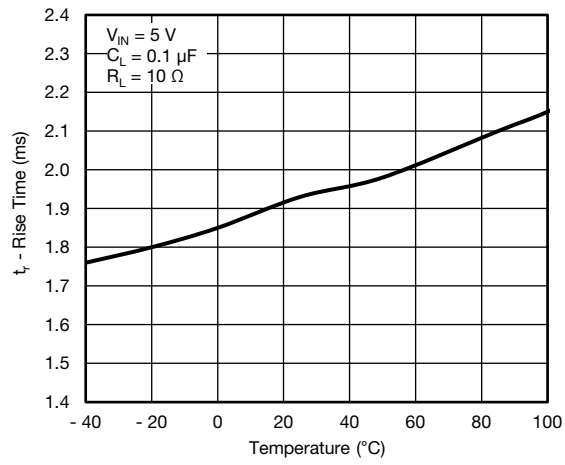


Fig. 17 - Rise Time vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

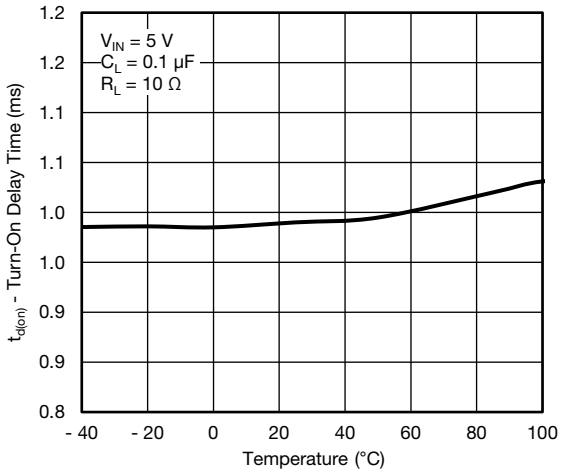


Fig. 18 - Turn-On Delay Time vs. Temperature

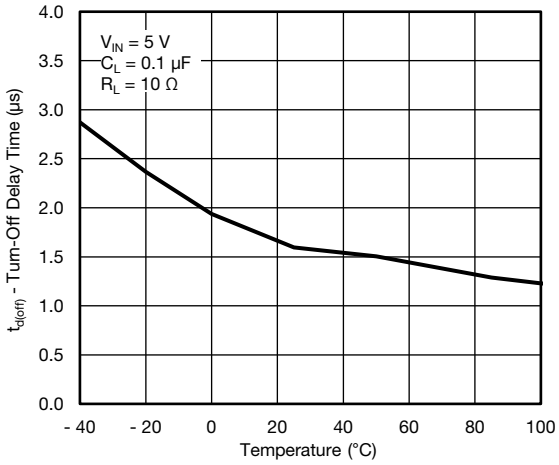


Fig. 20 - Turn-Off Delay Time vs. Temperature

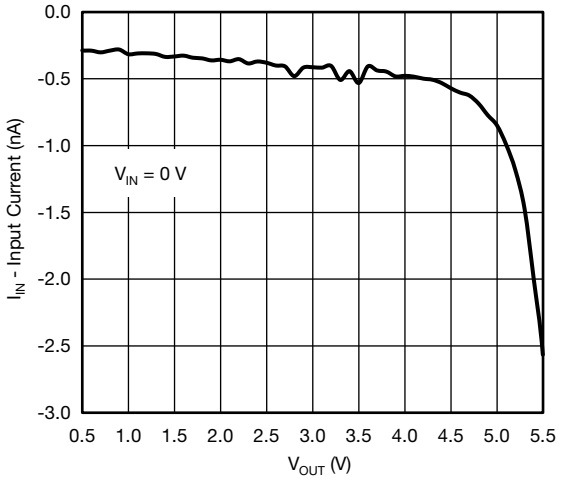


Fig. 19 - Reverse Blocking Current

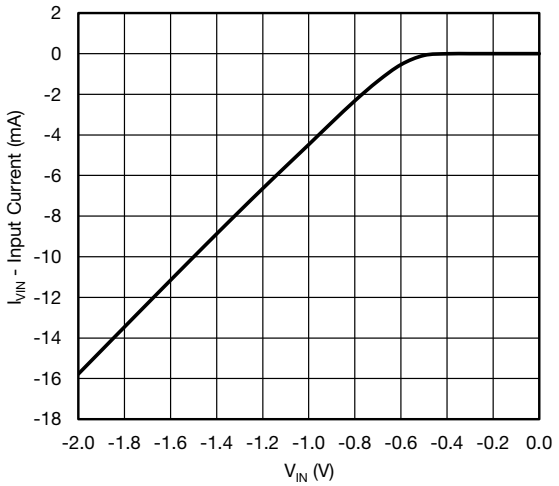
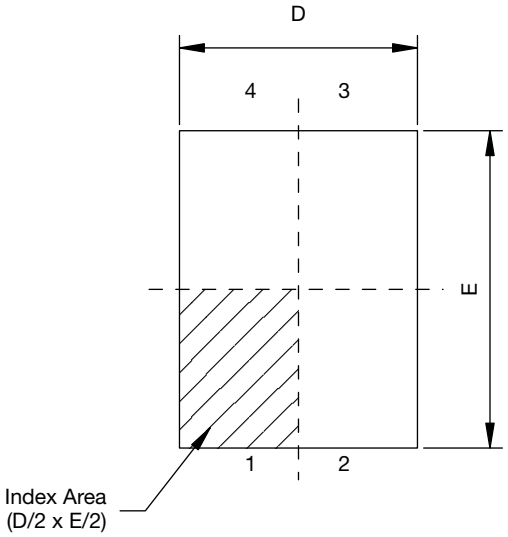


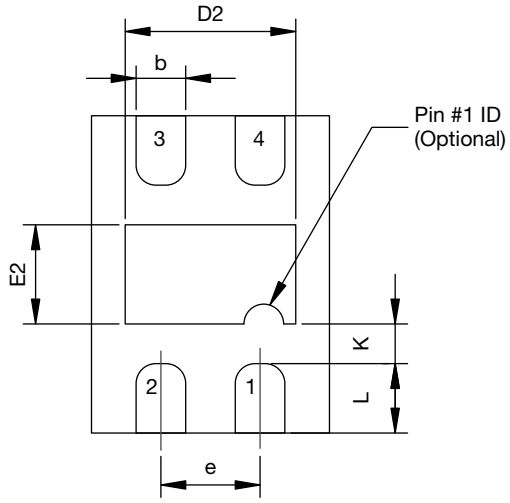
Fig. 21 - Negative Input Voltage Tolerance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62959.

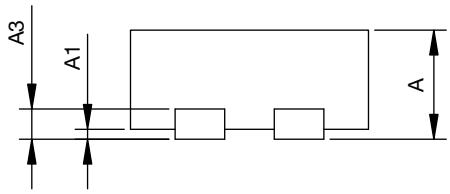
TDFN4 1.2 x 1.6 Case Outline



Top View



Bottom View



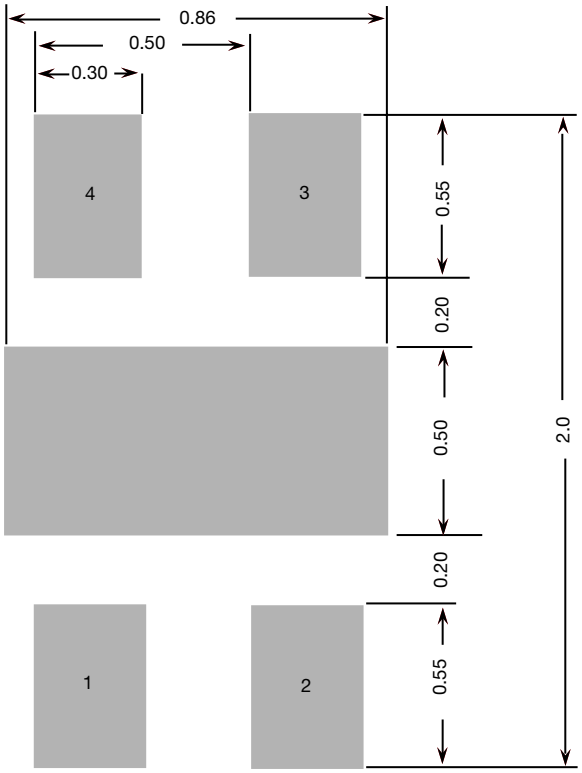
Side View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.45	0.55	0.60	0.017	0.022	0.024
A1	0.00	-	0.05	0.00	-	0.002
A3	0.15 REF. or 0.127 REF. (1)			0.006 or 0.005 (1)		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.15	1.20	1.25	0.045	0.047	0.049
D2	0.81	0.86	0.91	0.032	0.034	0.036
e	0.50 BSC			0.020		
E	1.55	1.60	1.65	0.061	0.063	0.065
E2	0.45	0.50	0.55	0.018	0.020	0.022
K	0.25 typ.			0.010 typ.		
L	0.25	0.30	0.35	0.010	0.012	0.014
ECN: T16-0143-Rev. C, 18-Apr-16 DWG: 5995						

Note

(1) The dimension depends on the leadframe that assembly house used.

RECOMMENDED MINIMUM PADS FOR TDFN4 1.2 x 1.6



Recommended Minimum Pads
Dimensions in mm

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