Maplesemi

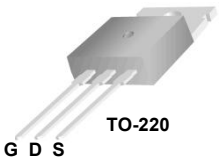
SLP13N50A / SLF13N50A
500V N-Channel MOSFET

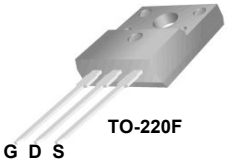
General Description

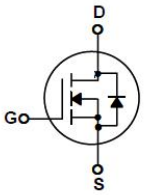
This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 13A, 500V, $R_{DS(on)}$ = 0.483Ω@V_{GS} = 10 V
- Low gate charge (typical 19.1nC)
- Low Crss (typical 4.6pF)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability







Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLP13N50A	SLF13N50A	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current - Continuous (TC= 25°C)	13		A
	- Continuous (TC= 100°C)	6.4*		A
I_{DM}	Drain Current - Pulsed (Note 1)	40*		A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	346		mJ
I_{AR}	Avalanche Current (Note 1)	10		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	41		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5		V/ns
P_D	Power Dissipation (TC = 25°C)	32.5		W
	- Derate above 25°C	0.26		W/°C
T_j , T_{stg}	Operating and Storage Temperature Range	-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds	300		°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	SLP13N50A	SLF13N50A	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.0		°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	--		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	47.8		°C/W

Electrical Characteristics TC = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		0.51		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V			1	μA
		V_{DS} = 400 V, TC = 125°C			10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V			-100	nA
On Characteristics						
$V_{GS(TH)}$	Gate Threshold voltage	V_{DS}=V_{GS}, I_D =250 uA	2.0		4.0	V
$R_{DS(On)}$	Drain-Source on-state resistance	V_{GS}=10 V, I_D = 5 A, T_J = 25°C		0.483	0.650	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 5 A (Note 4)		7.5		S
Dynamic Characteristics						
C_{iss}	Input capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1066		pF
C_{oss}	Output capacitance			153		pF
C_{rss}	Reverse transfer capacitance			4.6		pF
Switching Characteristics						
$t_{d(on)}$	Turn On Delay Time	V_{DD} = 250 V, ID = 10 A, R_G = 25 Ω (Note 4, 5)		20		ns
t_r	Rising Time			32		ns
$t_{d(off)}$	Turn Off Delay Time			64		ns
t_f	Fall Time			32		ns
Q_g	Total Gate Charge	V_{DS} = 400 V, ID = 10 A, V_{GS} = 10 V (Note 4, 5)		19.1		nC
Q_{gs}	Gate-Source Charge			5.5		nC
Q_{gd}	Gate-Drain Charge			6.4		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				10	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				40	A
V_{SD}	Diode Forward Voltage	V_{GS}= 0 V, I_S = 10 A			1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 10 A, dI_F / dt = 100 A/μs Note 4)		320		ns
Q_{rr}	Reverse Recovery Charge			2.2		μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 7.2 mH, IAS = 10 A, VDD = 50V, RG = 25 Ω, Starting TJ = 25°C
3. ISD≤10A, di/dt ≤200A/us, VDD ≤ BVDSS, Starting TJ = 25°C
4. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

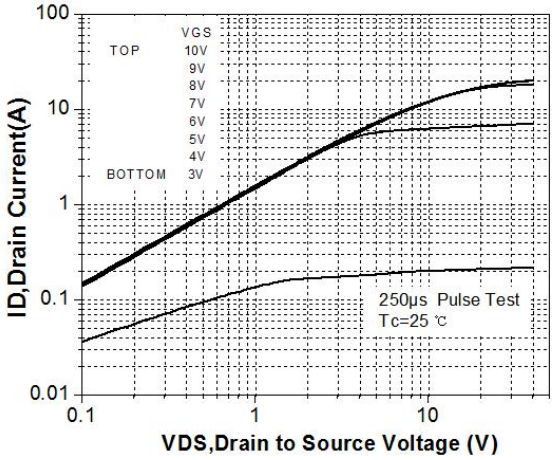


Figure 1. On-Region Characteristics

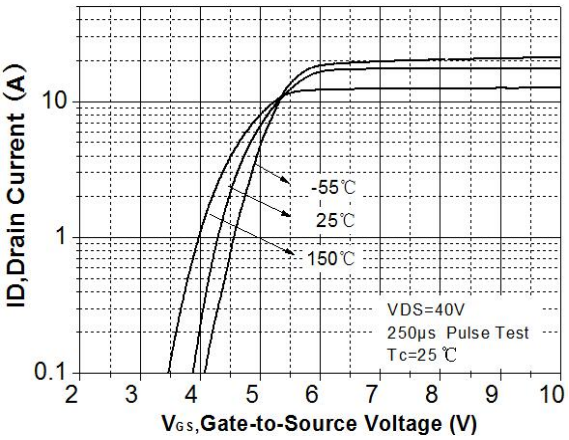


Figure 2. Transfer Characteristics

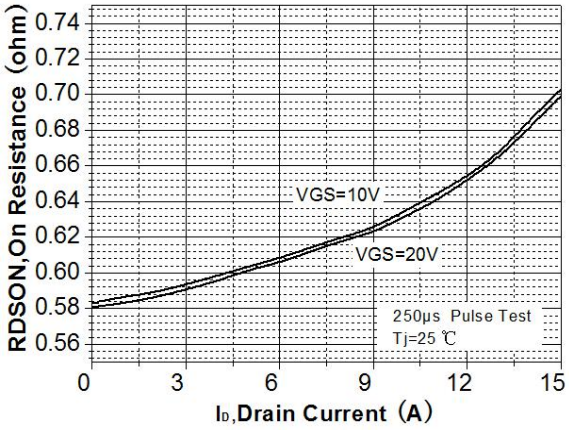


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

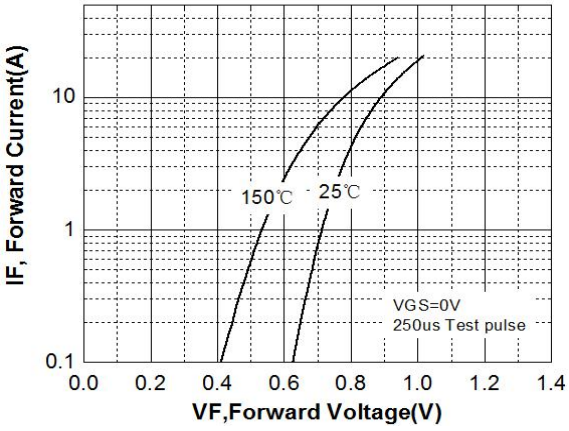


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

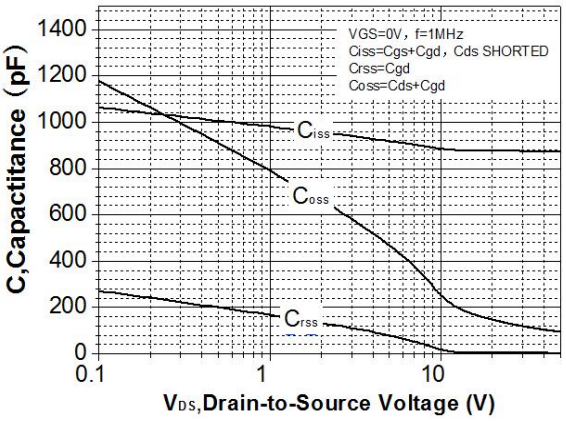


Figure 5. Capacitance Characteristics

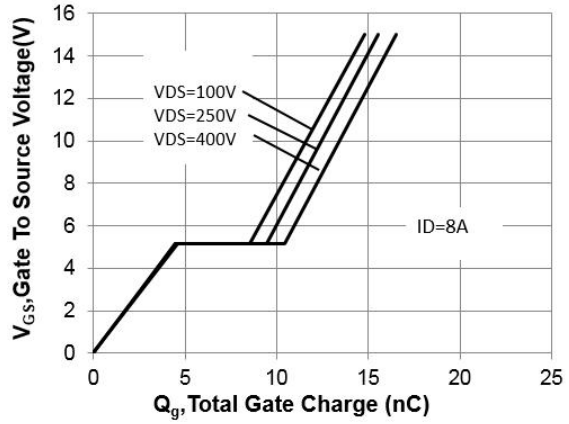


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

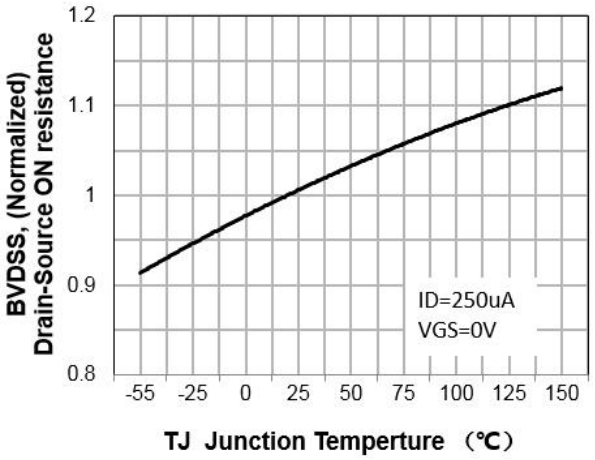


Figure 7. Breakdown Voltage Variation vs Temperature

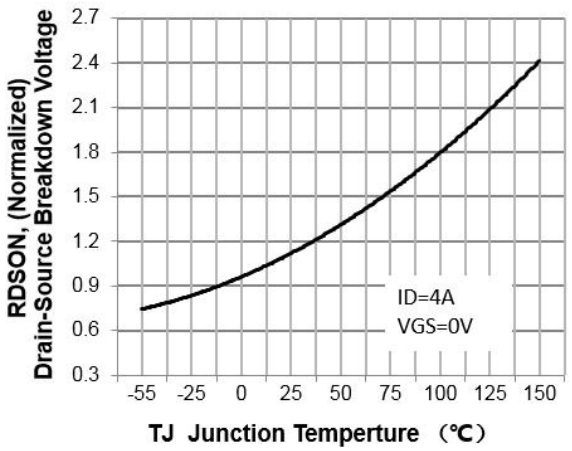


Figure 8. On-Resistance Variation vs Temperature

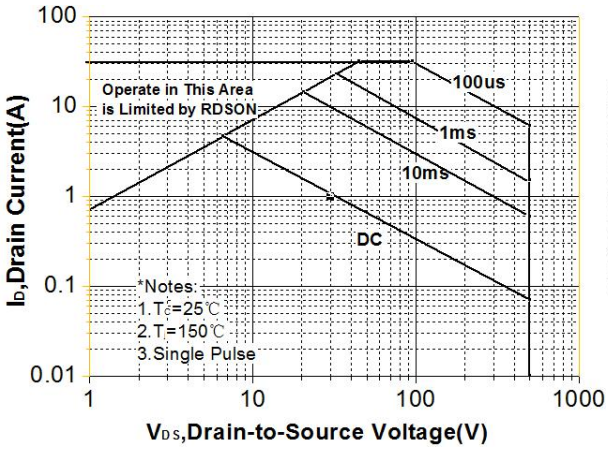


Figure 9. Maximum Safe Operating Area

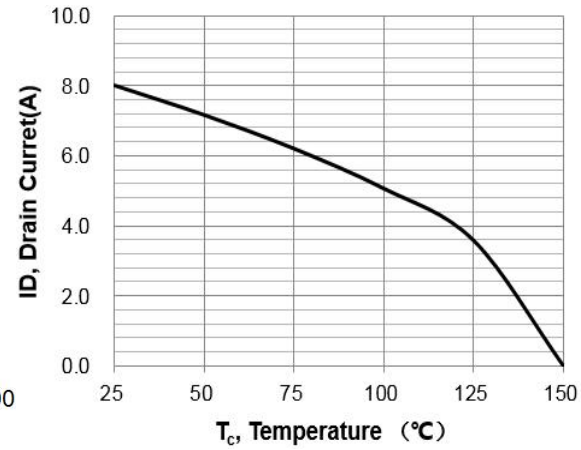


Figure 10. Maximum Drain Current vs Case Temperature

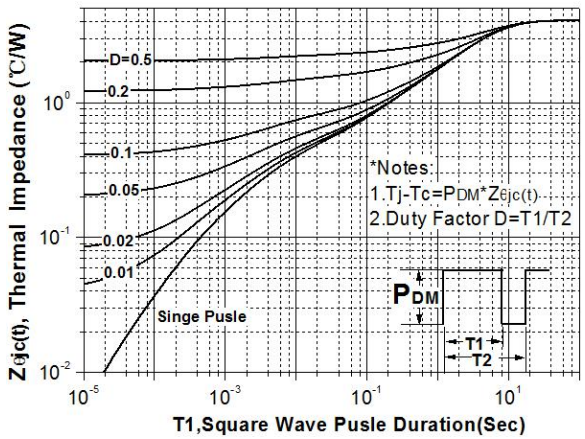
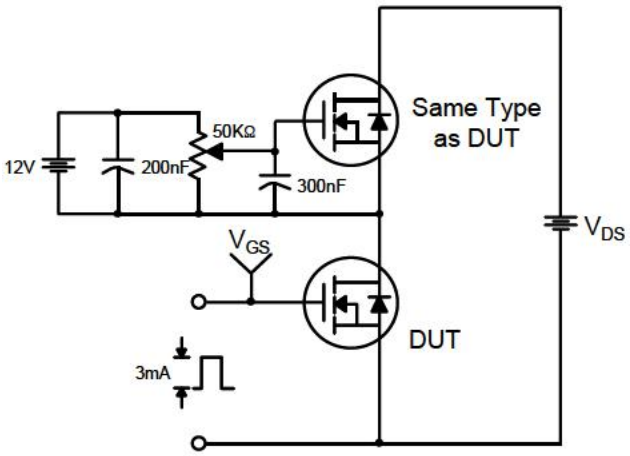
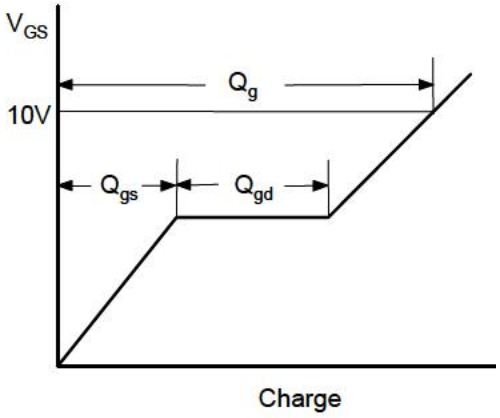


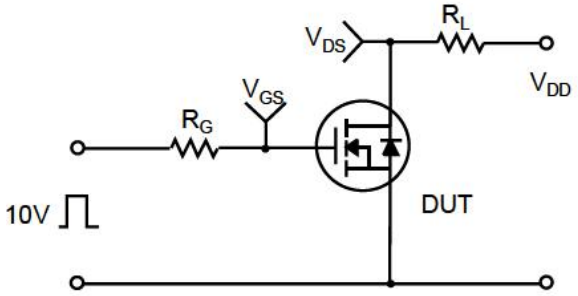
Figure 11. Transient Thermal Response Curve

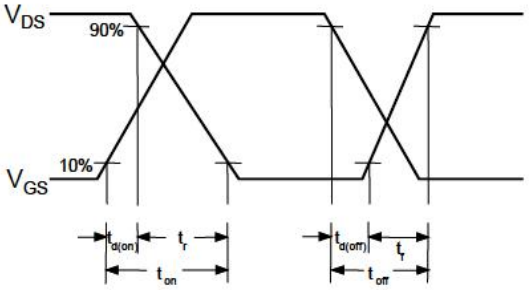
Gate Charge Test Circuit & Waveform



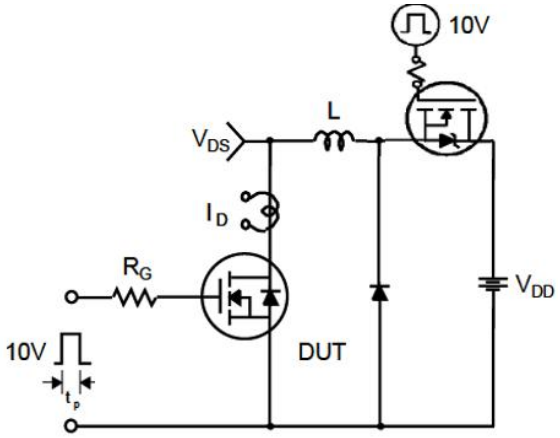


Resistive Switching Test Circuit & Waveforms

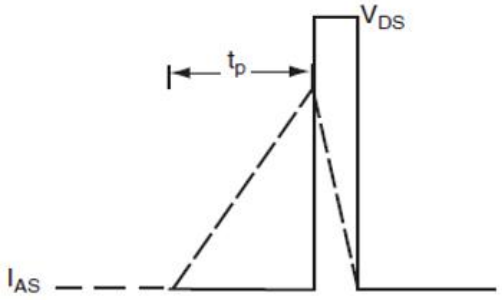




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms