PD77728 and PD77020 Evaluation Board User Guide
EV42P34A

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Introduction

The EV42P34A evaluation board is based on Microchip's PD77728 PoE manager and the PD77020 PoE controller. The EV42P34A demonstrates eight IEEE® 802.3bt 4-pair ports using the PD77728 and PD77020 in Controller Mode

The PD77728 device is a part of the seventh generation IEEE 802.3bt compliant Power over Ethernet (PoE) Power Sourcing Equipment (PSE) family from Microchip. This device is a fully integrated eight port PoE controller and PoE manager, with integrated Field Effect Transistor (FET) switches and current sense resistors. The PD77728 chipset supports IEEE 802.3af/at/bt standards, as well as legacy/pre-standard PD detection. The device is available in a 56-pin, 8 mm × 8 mm Quad flat no-lead (QFN) package.

The Evaluation Board (EVB) includes two, dedicated, bi-color (green and yellow) LEDs per each port. These LEDs provide the visual status of each port.

The following figure shows the top view of the evaluation board.

Figure 1. Evaluation Board - Top View
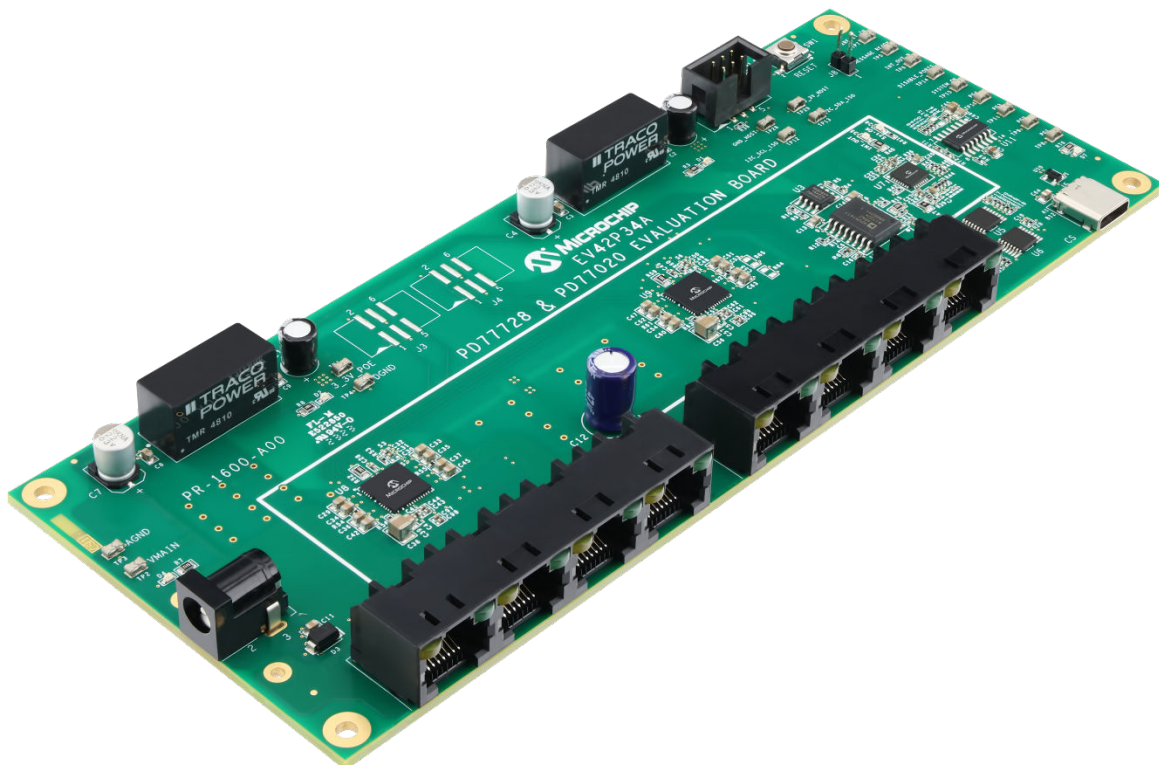
Features

The evaluation board has the following features.

- RJ45 Gang (Contains Eight RJ45 Connectors)
- Eight 4-pair ports structured by two PD77728 devices and controlled by the PD77020
- Switch Domain USB-C Interface to be connected to a PC with the Microchip GUI
- Manual Reset and Disable Port jumper
- Green And Yellow Bi-Color LED Status Indication for all eight ports
- Requires only a single power source
- 0 °C to 40 °C Operating Temperature
- RoHS Compliant

The following images show the system block diagram and the dimensions of the evaluation board.
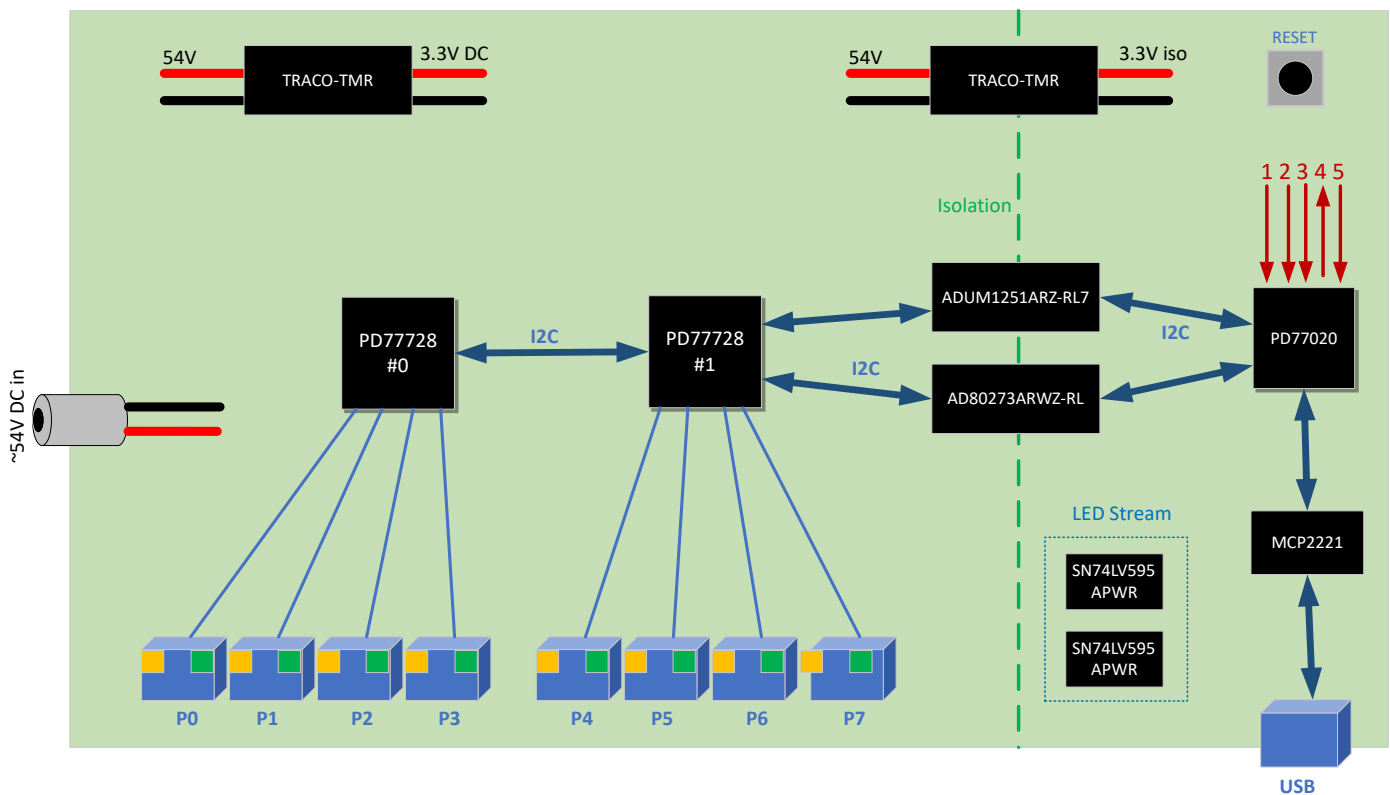
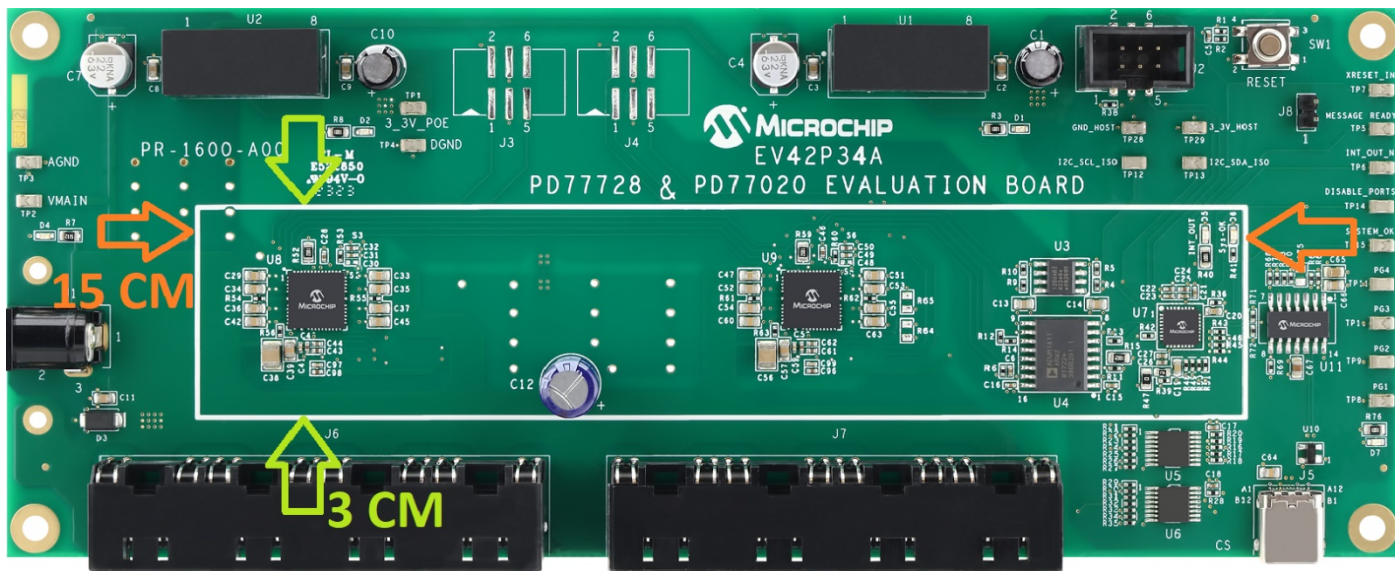**Figure 2.** EV42P34A Evaluation Board Block Diagram

Figure 3. EV42P34A Dimension

Note: Actual PoE application size is 15 cm × 3 cm

Table of Contents

1.   Overview

This section provides the basic overview of the EV42P34A Evaluation board.

1.1   Power

The EVB is powered by a single source through the DC connector J1. The input voltage level can be selected according to the following IEEE 802.3 PoE standards:

1. IEEE 802.3af: 44 V_{DC} to 57 V_{DC}

2. IEEE 802.3at: 50 V_{DC} to 57 V_{DC}

3. IEEE 802.3bt:

    a. 50 V_{DC} to 57 V_{DC} for type 3

    b. 52 V_{DC} to 57 V_{DC} for type 4

The recommended voltage level is 53 V_{DC} to 55 V_{DC}, which covers all the PoE standards. The EVB has three power domains as follows:

1. PoE domain, which is fed directly by the main supply and is the power domain provided by the RJ45

2. 3.3 V_{DC} which feeds the PD77728 and serial communication peripherals, same ground as the PoE domain. That 3.3 V_{DC} is generated by U2 (a DC/DC module).

3. Isolated 3.3 V_{DC} for the PD77020, LED stream, and for the USB port; this power is provided by U1.

Note: The EVB is polarity sensitive. The correct polarity is shown in the following figure.

Figure 1-1. DC Connector J1 Polarity

> **Important:** DC input connector J1 is limited to current level up to 4A. If higher current is needed, the 2 via holes next to J1 can be used, by soldering a cable to it. The two via holes support up to 8A to feed the whole EVB at full power.

The via holes are marked in the following figure; hole marked red is the V_{main} (+), and the hole marked black is the AGND (−).

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Figure 1-2. Power via Holes
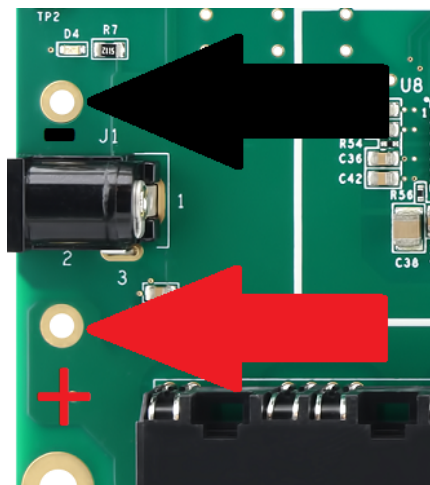
1.2   Interface and Control

This section describes the set-up procedures for serial communication, reset push-button, Over Supply Shutdown (OSS), PoE ports disable, power good input (PGD1–PGD4), and additional test points.

1.2.1   Serial Communication

The EVB supports serial communication with the PD77020 by I^2C. The serial communication is converted to USB by the Microchip MCP2221A (U11) to allow a user-friendly experience using the Microchip dedicated GUI.

To use the USB port, install the MCP2221A driver on your PC. The driver can be downloaded from the Microchip website at www.microchip.com/wwwproducts/en/MCP2221A

If R75 is installed as 0Ω, the USB converter (U11) is disabled, which allows the user to connect directly to the I^2C bus through the I^2C pins of U11, and control the EVB through I^2C. The DGND test-point is the GND for the I^2C bus.

For test points location, see figure Figure 1-7.

The EVB is set to I^2C address 0x4 (R37=147K).

In order to select the I^2C address, R37 should be installed according to the following table.

Table 1-1. I^2C Address Select

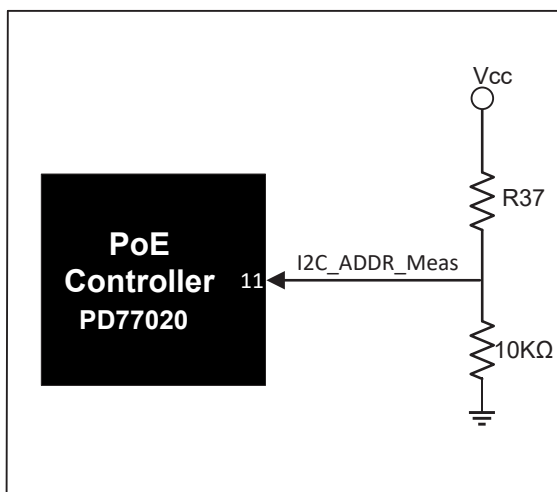| I^2C Address	Address (Hex)	R37 (kΩ)
#1	0x4	147
#2	0x8	86.6
#3	0xC	57.6
#4	0x10	43.2
#5	0x14	34
#6	0x18	26.7
#7	0x1C	22.1
#8	0x20	18.2
#9	0x24	15.4
#10	0x28	13

..........continued		
I²C Address	Address (Hex)	R37 (kΩ)
#11	0x2C	11
#12	0x30	9.31
#13	0x34	7.87
#14	0x38	6.49
#15	0x3C	5.49

The following diagram shows the I²C address setting for the PD77020 controller.
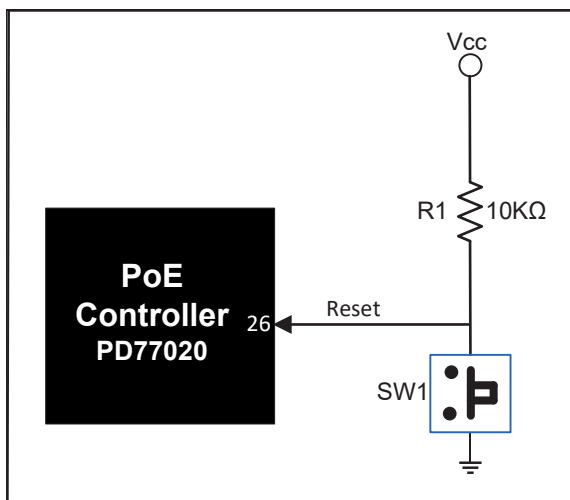
Figure 1-3. I²C Address Setting Diagram

1.2.2   Reset Pushbutton

The pushbutton is connected to the Reset pin of the PD77020 (pin 26), as shown in the following figure. Pressing the SW1 switch connects the Reset pin to GND, and resets the PoE system.

Figure 1-4. Reset Control Diagram

1.2.3 Over Supply Shutdown (OSS)

OSS is used to shut down ports based on the priority settings. The following figure shows the OSS control diagram.

Figure 1-5. OSS Control Diagram
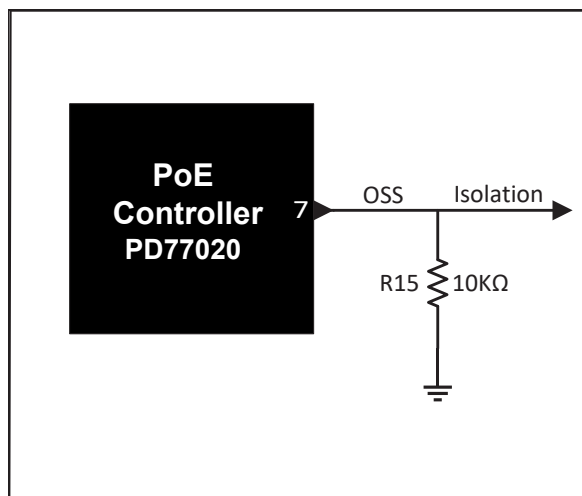
1.2.4 PoE Ports Disable Settings

The jumper J8 is connected to the Disable pin of the PD77020 (Pin 24). When the jumper J8 is installed, the Disable pin is connected to GND.

In normal operations, the host can disable all ports by setting this pin to '0'.

The following figure shows the J8 jumper settings.

Figure 1-6. Ports Disable Control Jumper Diagram

The following figure shows the J8 jumper port and the I^{2}C bus and GND_HOST test points on the evaluation board.

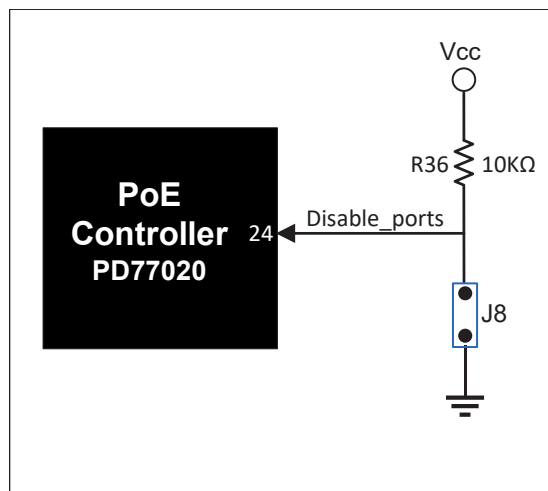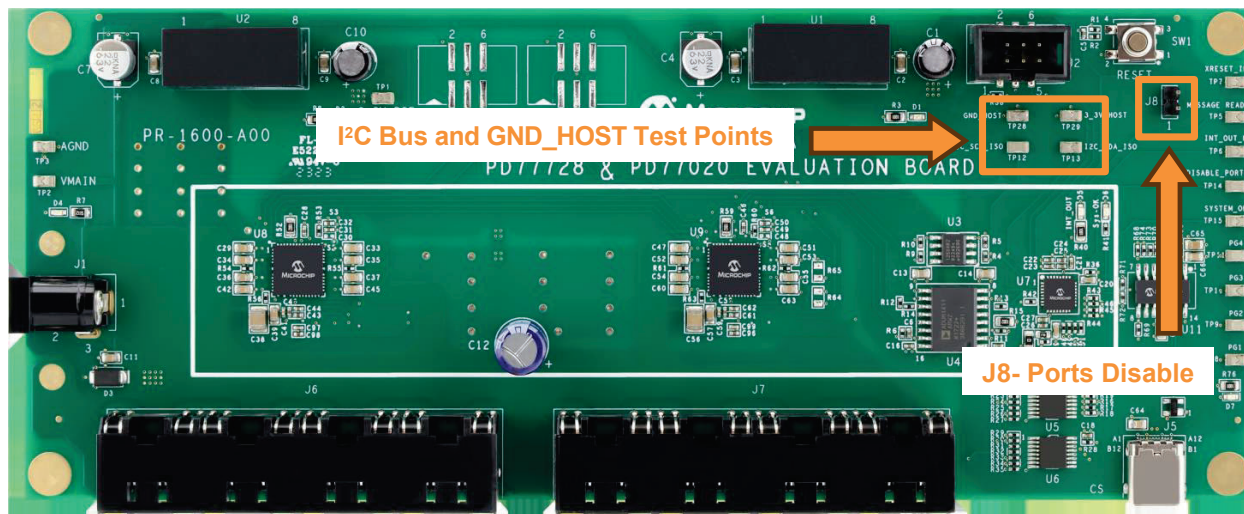**Figure 1-7.** I2C Bus and GND_HOST Test Points

> **Important:** These I^{2}C test points are connected to the I^{2}C bus, which connects the PD77020 to the two PD77728 devices.

1.2.5 Power Good Input (PGD) Settings

The EVB supports feeding from up to four power supplies, which includes 16 power banks (bank0 to bank15). Each power supply must generate a digital signal (0-3.3 V_{DC}), which indicates the power supply is active. The generated digital signal must be connected to one of the PGD pins of PD77020 (pins 17, 18, 19, and 20).

On the EVB, four PGD pins are pulled down with a 10K resistor to GND_HOST, which sets the default power bank to 0x00. To set a different bank than 0x00, the user can use the PG1–PG4 test points, located next to U11.

The four PG signals are referenced to the PD77020 domain (GND_HOST), see the following figures.

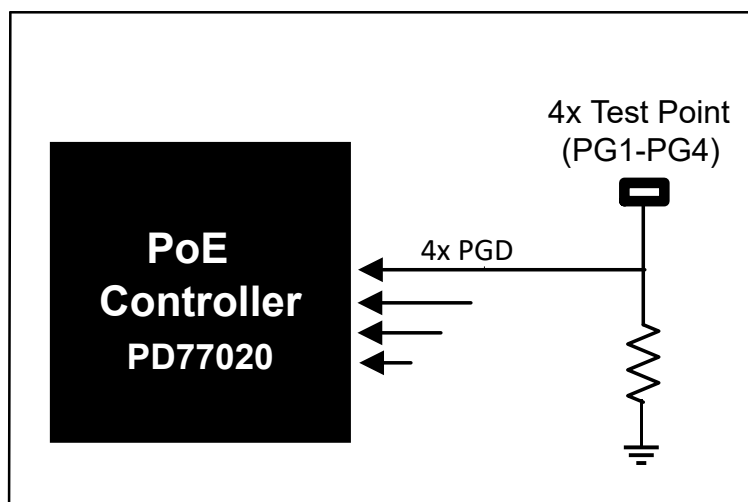**Figure 1-8.** PG1–PG4 Test Points Diagram

Figure 1-9. PG1–PG4 Test Points

1.2.6   Additional Test Points

The additional test points and their uses are listed below:

1. xI2C_Message_Ready (TP5): I^2C message ready for reading by the host. Controller asserts this line low when it has an answer to the host. Therefore, the host can poll this line and initiate I2C read cycle only when the message is ready. After the host reads the data from the controller, this pin is asserted to high. (Active Low).

2. xINT_OUT (TP6): Interrupt output indication. This line is asserted Low when a pre-configured event is in progress. (Active Low).

3. xReset_IN (TP7): Host reset input. (Active Low).

4. Disable ports (TP14): When this pin is pulled down, the PSE activity is off (Active Low)

5. xSys_ok (TP15): System validity indication. The behavior of this output is controlled by individual software mask. (Active Low).

Note: All the TPs in the preceding list are referenced to the PD77020 domain (GND_HOST).

The placement of the test points in the evaluation board is as shown in the following figure.

Figure 1-10. Test Points

1.3 LED Indication

The evaluation board contains status indication LED. These LEDs and their corresponding functions are listed in the following table.

Table 1-2. LED List

Designation	Function
D1	Isolated 3.3 V_{DC} ON (powers the PD77020, reset, LED stream, USB comm)
D2	3.3 V_{DC} ON (powers the two PD77728)
D4	V_{MAIN} ON
D5	Interrupt out (active low)
D6	System OK (active low)
Port (0–7)	Green and yellow LED per port: • LED OFF= Port is OFF • Green LED on= 4-pair port is on • Yellow LED on= 2-pair port is on • LED blinking= Port is OFF due to error/under load/ power management

1.4 RJ45 Connectors Polarity

The eight ports of J6 and J7 are 4-pair up to 90W each. The polarity of the port is listed in the following table.

Table 1-3. J6 and J7/RJ45 Connector 4-Pair Port (Ports 0-7)

Pin Number (Each RJ45 Port)	Polarity
1, 2	Negative Alt A
3, 6	Positive Alt A
4, 5	Positive Alt B
7, 8	Negative Alt B

See the following figure for port numbering.

Figure 1-11. Port Numbering
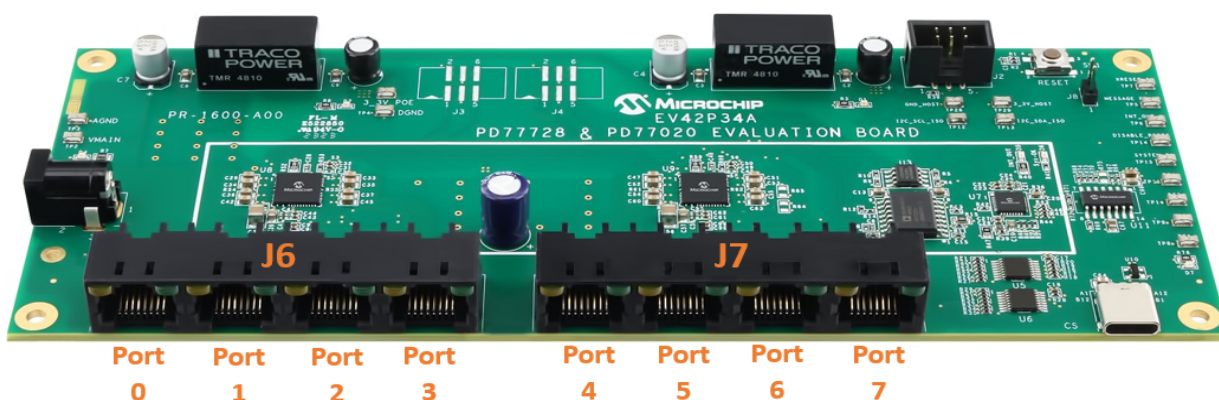
2.   Installation and Setting

This section describes the steps required to install and operate the EVB. Take the following precautions before starting the installation:

- Ensure that the 52 V_{DC}– 57V_{DC} power supply of the board is turned off before plugging in the DC connector
- Turn the main power supply on only after the DC connector is plugged in
- Ensure the correct polarity of the power supply cable. The polarity of the power supply cable is as shown in Figure 1-1.

2.1   Schematics

Contact Microchip for the full-board schematics.

3.   Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
A	04/2024	Initial release

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