



**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



16-Mbit (2M words × 8 bits) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby power
  - Typical standby current: 5.5 μA
  - Maximum standby current: 16 μA
- High speed: 45 ns/55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 4.5 V to 5.5 V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-ball VFBGA package

Functional Description

CY62168G and CY62168GE are high-performance CMOS low-power (MoBL<sup>®</sup>) SRAM devices with embedded ECC. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62168GE device includes an error indication pin that signals a single-bit error-detection and correction event during a read cycle.

Devices with a single chip enable input are accessed by asserting the chip enable input (CE) LOW. Dual chip enable devices are accessed by asserting both chip enable inputs – CE<sub>1</sub> as LOW and CE<sub>2</sub> as HIGH.

Write to the device by taking Chip Enable 1 ( $\overline{CE}_1$ ) LOW and Chip Enable 2 (CE<sub>2</sub>) HIGH and the Write Enable (WE) input LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>).

Read from the device by taking Chip Enable 1 ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW and Chip Enable 2 (CE<sub>2</sub>) HIGH while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input and output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or CE<sub>2</sub> LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $\overline{CE}_1$  LOW and CE<sub>2</sub> HIGH and WE LOW). See the Truth Table – CY62168G/CY62168GE on page 14 for a complete description of read and write modes.

On CY62168GE devices, the detection and correction of a single bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH) [1].

The CY62168G and CY62168GE devices are available in a Pb-free 48-pin VFBGA package. The logic block diagrams are on page 2.

For a complete list of related resources, [click here](#).

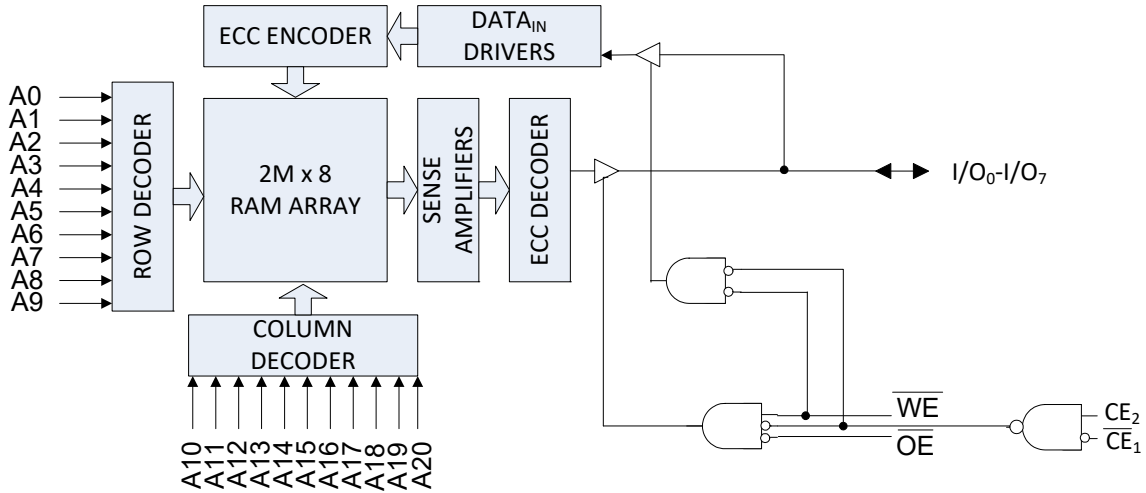
Product Portfolio

| Product       | Features and Options<br>(see Pin Configurations section) | Range      | V <sub>CC</sub> Range (V) | Speed (ns) | Power Dissipation              |     |                                |     |
|---------------|--|------------|---------------------------|------------|--------------------------------|-----|--------------------------------|-----|
|               |  |            |                           |            | Operating I <sub>CC</sub> (mA) |     | Standby, I <sub>SB2</sub> (μA) |     |
|               |  |            |                           |            | f = f <sub>max</sub>           |     |                                |     |
|               |  |            |                           |            | Typ <sup>[2]</sup>             | Max | Typ <sup>[2]</sup>             | Max |
| CY62168G(E)18 | Single or dual Chip Enables                              | Industrial | 1.65 V–2.2 V              | 55         | 29                             | 32  | 7                              | 26  |
| CY62168G(E)   |  |            | 4.5 V–5.5 V               | 45         | 29                             | 36  | 5.5                            | 16  |
|               | Optional ERR pin   |            |                           |            |                                |     |                                |     |

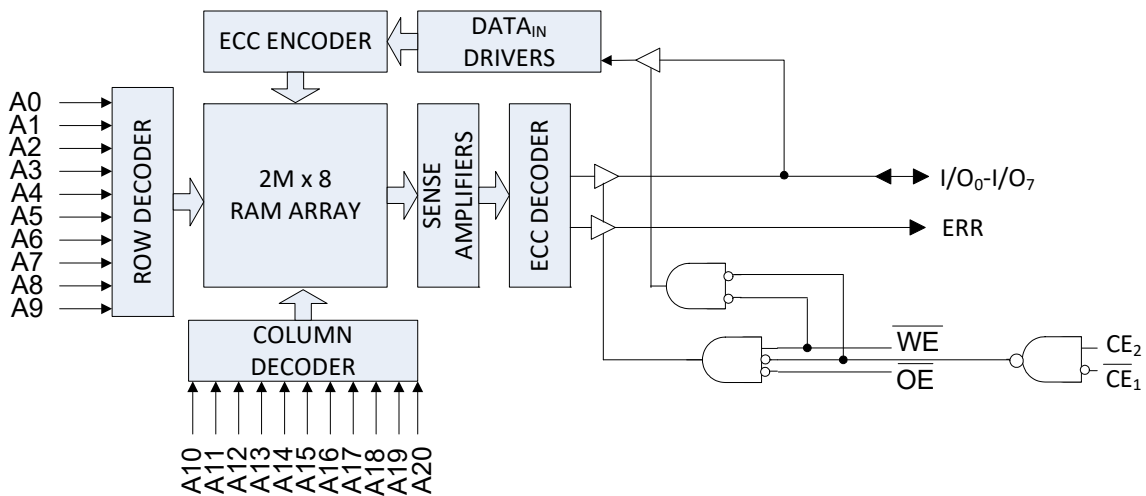
Notes

1. This device does not support automatic write-back on error detection.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

Logic Block Diagram – CY62168G



Logic Block Diagram – CY62168GE



## Contents

|   |           |  |           |
|---|-----------|--|-----------|
| <b>Pin Configurations</b> .....               | <b>4</b>  | <b>Ordering Information</b> .....                    | <b>15</b> |
| <b>Maximum Ratings</b> .....                  | <b>5</b>  | Ordering Code Definitions .....                      | 15        |
| <b>Operating Range</b> .....                  | <b>5</b>  | <b>Package Diagrams</b> .....                        | <b>16</b> |
| <b>DC Electrical Characteristics</b> .....    | <b>5</b>  | <b>Acronyms</b> .....                                | <b>17</b> |
| <b>Capacitance</b> .....                      | <b>7</b>  | <b>Document Conventions</b> .....                    | <b>17</b> |
| <b>Thermal Resistance</b> .....               | <b>7</b>  | Units of Measure .....                               | 17        |
| <b>AC Test Loads and Waveforms</b> .....      | <b>7</b>  | <b>Document History Page</b> .....                   | <b>18</b> |
| <b>Data Retention Characteristics</b> .....   | <b>8</b>  | <b>Sales, Solutions, and Legal Information</b> ..... | <b>20</b> |
| <b>Data Retention Waveform</b> .....          | <b>8</b>  | Worldwide Sales and Design Support .....             | 20        |
| <b>Switching Characteristics</b> .....        | <b>9</b>  | Products .....                                       | 20        |
| <b>Switching Waveforms</b> .....              | <b>10</b> | PSoC® Solutions .....                                | 20        |
| <b>Truth Table – CY62168G/CY62168GE</b> ..... | <b>14</b> | Cypress Developer Community .....                    | 20        |
| <b>ERR Output – CY62168GE</b> .....           | <b>14</b> | Technical Support .....                              | 20        |

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1 mm) pinout<sup>[3]</sup>  
CY62168G

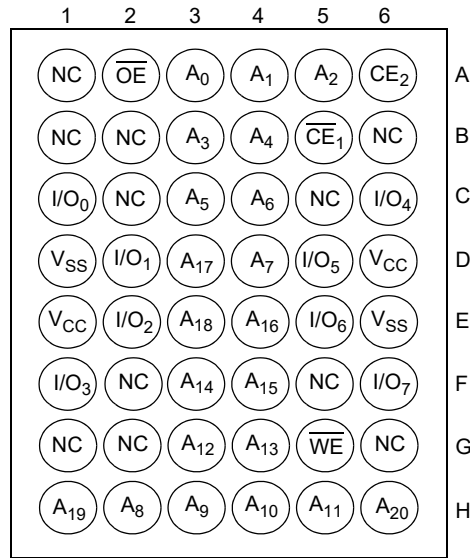
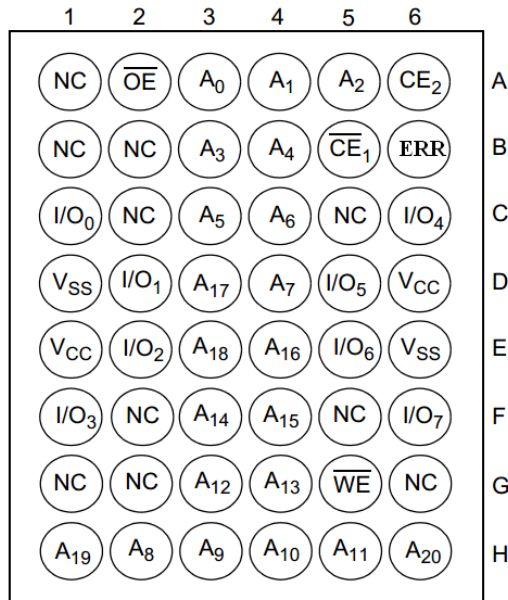


Figure 2. 48-ball VFBGA (6 × 8 × 1 mm) pinout<sup>[3, 4]</sup>  
CY62168GE



Note

- 3. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- 4. ERR is an Output pin. If not used, this pin should be left floating.

### Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage temperature ..... -65 °C to + 150 °C
- Ambient temperature with power applied ..... -55 °C to + 125 °C
- Supply voltage to ground potential ..... -0.5 V to 6 V
- DC voltage applied to outputs in High Z state<sup>[5]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

- DC input voltage<sup>[5]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V
- Output current into outputs (LOW) ..... 20 mA
- Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V
- Latch-up current ..... >140 mA

### Operating Range

| Grade      | Ambient Temperature | V <sub>CC</sub> <sup>[6]</sup>  |
|------------|---------------------|---------------------------------|
| Industrial | -40 °C to +85 °C    | 1.65 V to 2.2 V, 4.5 V to 5.5 V |

### DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

| Parameter       | Description                      |                 | Test Conditions  | 45 ns/55 ns                          |                    |                       | Unit |
|-----------------|----------------------------------|-----------------|--|--------------------------------------|--------------------|-----------------------|------|
|                 |                                  |                 |  | Min                                  | Typ <sup>[7]</sup> | Max                   |      |
| V <sub>OH</sub> | Output HIGH voltage              | 1.65 V to 2.2 V | V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA           | 1.4                                  | -                  | -                     | V    |
|                 |                                  | 4.5 V to 5.5 V  | V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA           | 2.4                                  | -                  | -                     | V    |
|                 |                                  | 4.5 V to 5.5 V  | V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA           | V <sub>CC</sub> - 0.4 <sup>[8]</sup> | -                  | -                     | V    |
| V <sub>OL</sub> | Output LOW voltage               | 1.65 V to 2.2 V | V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA            | -                                    | -                  | 0.2                   | V    |
|                 |                                  | 4.5 V to 5.5 V  | V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA            | -                                    | -                  | 0.4                   | V    |
| V <sub>IH</sub> | Input HIGH voltage               | 1.65 V to 2.2 V | -  | 1.4                                  | -                  | V <sub>CC</sub> + 0.2 | V    |
|                 |                                  | 4.5 V to 5.5 V  | -  | 2.2                                  | -                  | V <sub>CC</sub> + 0.5 | V    |
| V <sub>IL</sub> | Input LOW voltage <sup>[9]</sup> | 1.65 V to 2.2 V | -  | -0.2                                 | -                  | 0.4                   | V    |
|                 |                                  | 4.5 V to 5.5 V  | -  | -0.5                                 | -                  | 0.8                   | V    |
| I <sub>Ix</sub> | Input leakage current            |                 | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                    | -1.0                                 | -                  | +1.0                  | μA   |
| I <sub>Oz</sub> | Output leakage current           |                 | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled | -1.0                                 | -                  | +1.0                  | μA   |

**Notes**

5. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
6. Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for V<sub>CC</sub> range of 1.65 V-2.2 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V-5.5 V), T<sub>A</sub> = 25 °C.
8. This parameter is guaranteed by design and is not tested.
9. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.

**DC Electrical Characteristics** (continued)

 Over the operating range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ 

| Parameter        | Description   | Test Conditions   | 45 ns/55 ns                       |                    |           | Unit          |               |
|------------------|---|---|-----------------------------------|--------------------|-----------|---------------|---------------|
|                  |   |   | Min                               | Typ <sup>[7]</sup> | Max       |               |               |
| $I_{CC}$         | $V_{CC}$ operating supply current   | $V_{CC} = \text{Max}$ ,<br>$I_{OUT} = 0\text{ mA}$ ,<br>CMOS levels   | $f = 22.22\text{ MHz}$<br>(45 ns) | –                  | 29.0      | 36.0          | mA            |
|                  |   |   | $f = 18.18\text{ MHz}$<br>(55 ns) | –                  | 29.0      | 32.0          | mA            |
|                  |   |   | $f = 1\text{ MHz}$                | –                  | 7.0       | 9.0           | mA            |
| $I_{SB1}^{[10]}$ | Automatic power down current –<br>CMOS inputs;<br>$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$ | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \leq 0.2\text{ V}$ ,<br>$f = f_{max}$ (address and data only),  | –                                 | 5.5                | 16.0      | $\mu\text{A}$ |               |
|                  | Automatic power down current –<br>CMOS inputs; $V_{CC} = 1.65$ to $2.2\text{ V}$            | $f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), $V_{CC} = V_{CC(max)}$   | –                                 | 7                  | 26.0      | $\mu\text{A}$ |               |
| $I_{SB2}^{[10]}$ | Automatic power down current –<br>CMOS inputs;<br>$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$ | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or<br>$CE_2 \leq 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or<br>$V_{IN} \leq 0.2\text{ V}$ ,<br>$f = 0$ , $V_{CC} = V_{CC(max)}$ | $25\text{ }^{\circ}\text{C}$ [11] | –                  | 5.5       | 6.5           | $\mu\text{A}$ |
|                  |   |   | $40\text{ }^{\circ}\text{C}$ [11] | –                  | 6.3       | 8.0           | $\mu\text{A}$ |
|                  |   |   | $70\text{ }^{\circ}\text{C}$ [11] | –                  | 8.4       | 12.0          | $\mu\text{A}$ |
|                  |   |   | $85\text{ }^{\circ}\text{C}$      | –                  | 12.0 [11] | 16.0          | $\mu\text{A}$ |
|                  | Automatic power down current –<br>CMOS inputs;<br>$V_{CC} = 1.65$ to $2.2\text{ V}$         | $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ ,<br>$f = 0$ , $V_{CC} = V_{CC(max)}$       | –                                 | 7.0                | 26.0      | $\mu\text{A}$ |               |

**Notes**

10. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.  
 11. The  $I_{SB2}$  limits at  $25\text{ }^{\circ}\text{C}$ ,  $40\text{ }^{\circ}\text{C}$ ,  $70\text{ }^{\circ}\text{C}$  and typical limit at  $85\text{ }^{\circ}\text{C}$  are guaranteed by design and not 100% tested.

### Capacitance

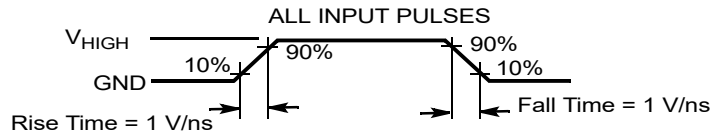
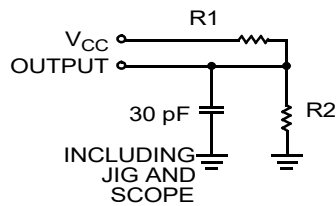
| Parameter <sup>[12]</sup> | Description        | Test Conditions   | Max | Unit |
|---------------------------|--------------------|---|-----|------|
| C <sub>IN</sub>           | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub> | 10  | pF   |
| C <sub>OUT</sub>          | Output capacitance |   | 10  | pF   |

### Thermal Resistance

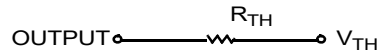
| Parameter <sup>[12]</sup> | Description                              | Test Conditions   | 48-ball VFBGA | Unit |
|---------------------------|--|---|---------------|------|
| θ <sub>JA</sub>           | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 31.50         | °C/W |
| θ <sub>JC</sub>           | Thermal resistance (junction to case)    |   | 15.75         | °C/W |

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



| Parameters        | 1.8 V | 2.5 V | 3.0 V | 5.0 V | Unit |
|-------------------|-------|-------|-------|-------|------|
| R1                | 13500 | 16667 | 1103  | 1800  | Ω    |
| R2                | 10800 | 15385 | 1554  | 990   | Ω    |
| R <sub>TH</sub>   | 6000  | 8000  | 645   | 639   | Ω    |
| V <sub>TH</sub>   | 0.8   | 1.2   | 1.75  | 1.77  | V    |
| V <sub>HIGH</sub> | 1.8   | 2.5   | 3.0   | 5.0   | V    |

**Note**

12. Tested initially and after any design or process changes that may affect these parameters.



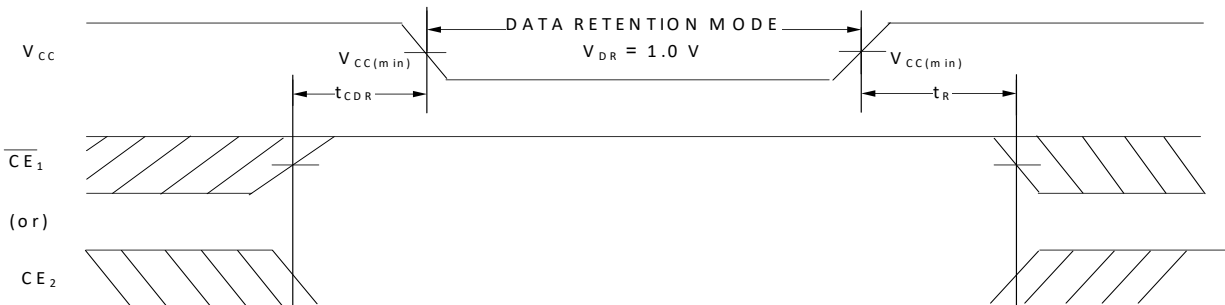
## Data Retention Characteristics

Over the Operating Range

| Parameter                      | Description                          | Conditions  | Min   | Typ <sup>[13]</sup> | Max  | Unit          |
|--------------------------------|--------------------------------------|---|-------|---------------------|------|---------------|
| $V_{DR}$                       | $V_{CC}$ for data retention          |   | 1.0   | –                   | –    | V             |
| $I_{CCDR}$ <sup>[14, 15]</sup> | Data retention current               | $1.2\text{ V} \leq V_{CC} \leq 2.2\text{ V}$ ,<br>$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | –     | 7.0                 | 26.0 | $\mu\text{A}$ |
|                                |                                      | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ ,<br>$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | –     | 5.5                 | 16.0 | $\mu\text{A}$ |
| $t_{CDR}$ <sup>[16]</sup>      | Chip deselect to data retention time |   | 0     | –                   | –    | –             |
| $t_R$ <sup>[16, 17]</sup>      | Operation recovery time              |   | 45/55 | –                   | –    | ns            |

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

13. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8\text{ V}$  (for  $V_{CC}$  range of 1.65 V–2.2 V), and  $V_{CC} = 5\text{ V}$  (for  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25\text{ }^\circ\text{C}$ .
14. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.
15.  $I_{CCDR}$  is guaranteed only after device is first powered up to  $V_{CC(min)}$  and brought down to  $V_{DR}$ .
16. These parameters are guaranteed by design.
17. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .

## Switching Characteristics

| Parameter <sup>[18, 19]</sup>          | Description  | 45 ns |      | 55 ns |      | Unit |
|--|--|-------|------|-------|------|------|
|  |  | Min   | Max  | Min   | Max  |      |
| <b>Read Cycle</b>                      |  |       |      |       |      |      |
| $t_{RC}$                               | Read cycle time  | 45.0  | –    | 55.0  | –    | ns   |
| $t_{AA}$                               | Address to data valid / Address to ERR valid   | –     | 45.0 | –     | 55.0 | ns   |
| $t_{OHA}$                              | Data hold from address change / ERR hold from address change                           | 10.0  | –    | 10.0  | –    | ns   |
| $t_{ACE}$                              | $\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid / $\overline{CE}$ LOW to ERR valid | –     | 45.0 | –     | 55.0 | ns   |
| $t_{DOE}$                              | $\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid                   | –     | 22.0 | –     | 25.0 | ns   |
| $t_{LZOE}$                             | $\overline{OE}$ LOW to Low Z <sup>[19, 20]</sup>                                       | 5.0   | –    | 5.0   | –    | ns   |
| $t_{HZOE}$                             | $\overline{OE}$ HIGH to High Z <sup>[19, 20, 21]</sup>                                 | –     | 18.0 | –     | 18.0 | ns   |
| $t_{LZCE}$                             | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z <sup>[19, 20]</sup>                     | 10.0  | –    | 10.0  | –    | ns   |
| $t_{HZCE}$                             | $\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z <sup>[19, 20, 21]</sup>                | –     | 18.0 | –     | 18.0 | ns   |
| $t_{PU}$ <sup>[22]</sup>               | $\overline{CE}_1$ LOW and $CE_2$ HIGH to power-up                                      | 0     | –    | 0     | –    | ns   |
| $t_{PD}$ <sup>[22]</sup>               | $\overline{CE}_1$ HIGH and $CE_2$ LOW to power-down                                    | –     | 45.0 | –     | 55.0 | ns   |
| <b>Write Cycle</b> <sup>[23, 24]</sup> |  |       |      |       |      |      |
| $t_{WC}$                               | Write cycle time   | 45.0  | –    | 55.0  | –    | ns   |
| $t_{SCE}$                              | $\overline{CE}_1$ LOW and $CE_2$ HIGH to write end                                     | 35.0  | –    | 40.0  | –    | ns   |
| $t_{AW}$                               | Address setup to write end   | 35.0  | –    | 40.0  | –    | ns   |
| $t_{HA}$                               | Address hold from write end  | 0     | –    | 0     | –    | ns   |
| $t_{SA}$                               | Address setup to write start   | 0     | –    | 0     | –    | ns   |
| $t_{PWE}$                              | $\overline{WE}$ pulse width  | 35.0  | –    | 40.0  | –    | ns   |
| $t_{SD}$                               | Data setup to write end  | 25.0  | –    | 25.0  | –    | ns   |
| $t_{HD}$                               | Data hold from write end   | 0     | –    | 0     | –    | ns   |
| $t_{HZWE}$                             | $\overline{WE}$ LOW to High Z <sup>[19, 21, 20]</sup>                                  | –     | 18.0 | –     | 20.0 | ns   |
| $t_{LZWE}$                             | $\overline{WE}$ HIGH to Low Z <sup>[19, 20]</sup>                                      | 10.0  | –    | 10.0  | –    | ns   |

### Notes

18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
19. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
20. Tested initially and after any design or process changes that may affect these parameters.
21.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
22. These parameters are guaranteed by design and are not tested.
23. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
24. The minimum write cycle pulse width for write cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  Low) should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62168G (Address Transition Controlled)<sup>[25, 26]</sup>

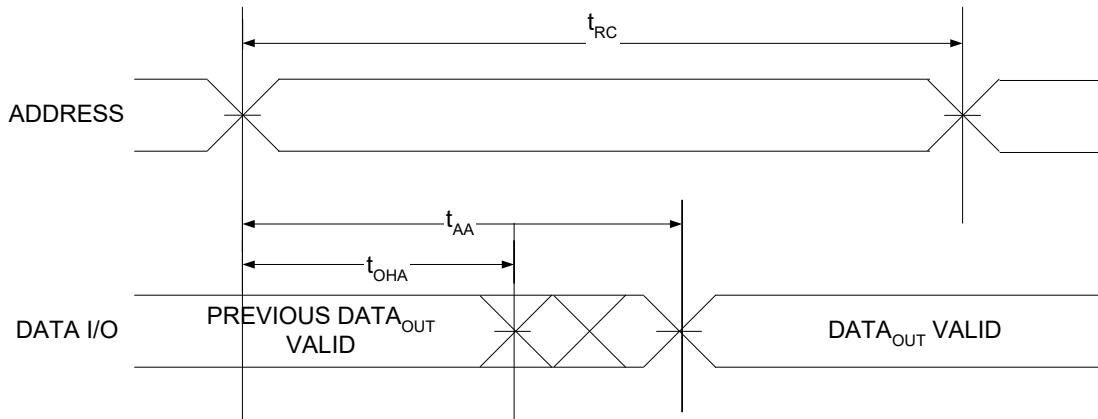
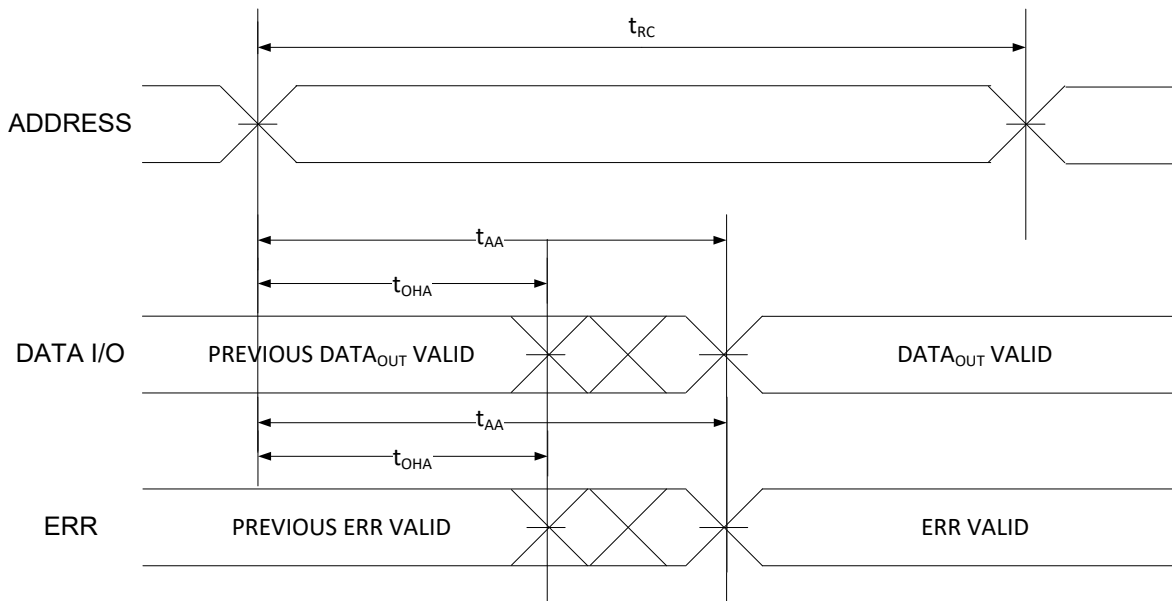


Figure 6. Read Cycle No. 1 of CY62168GE (Address Transition Controlled)<sup>[25, 26]</sup>

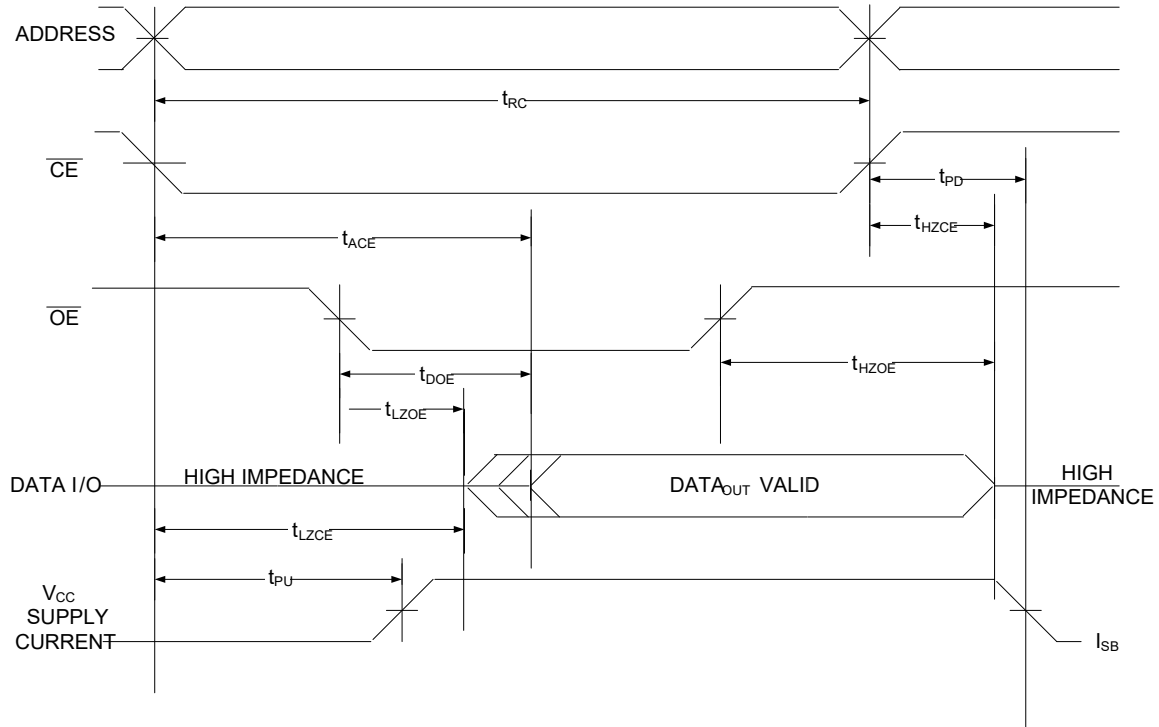


### Notes

25. The device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ .  
 26.  $\overline{WE}$  is HIGH for read cycle.

Switching Waveforms (continued)

Figure 7. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[27, 28, 29]</sup>

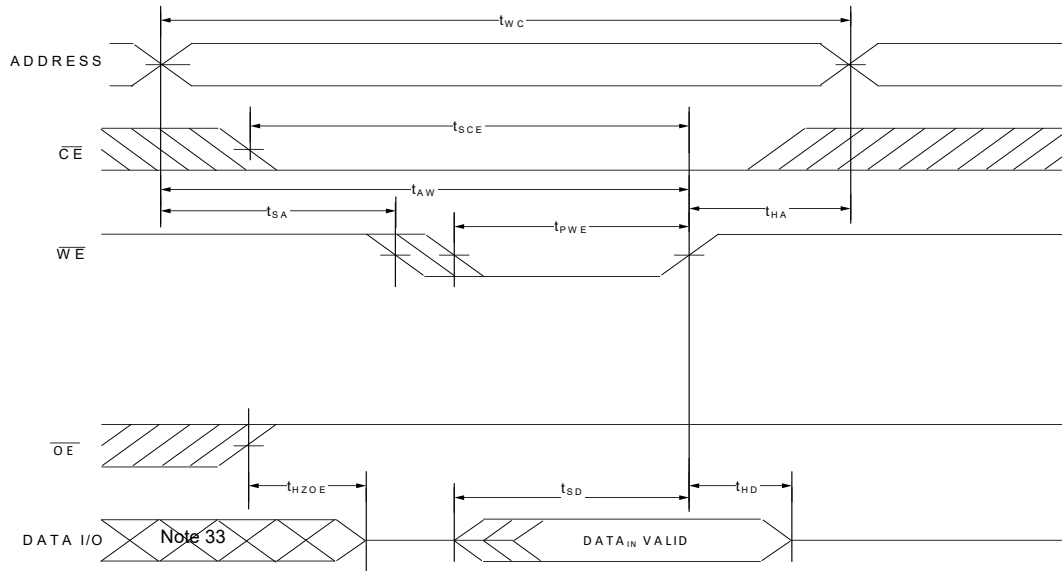


Notes

- 27.  $\overline{WE}$  is HIGH for read cycle.
- 28. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 29. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[30, 31, 32]</sup>



Notes

- 30. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 31. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 32. Data I/O is in the high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ .
- 33. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  Low)<sup>[34, 35, 36, 37]</sup>

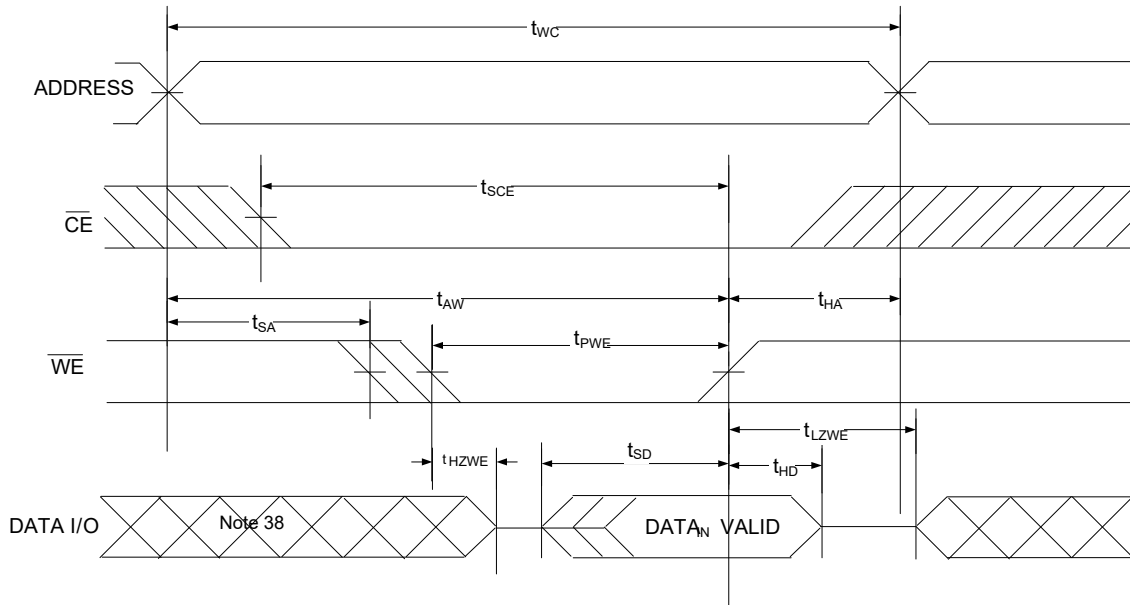
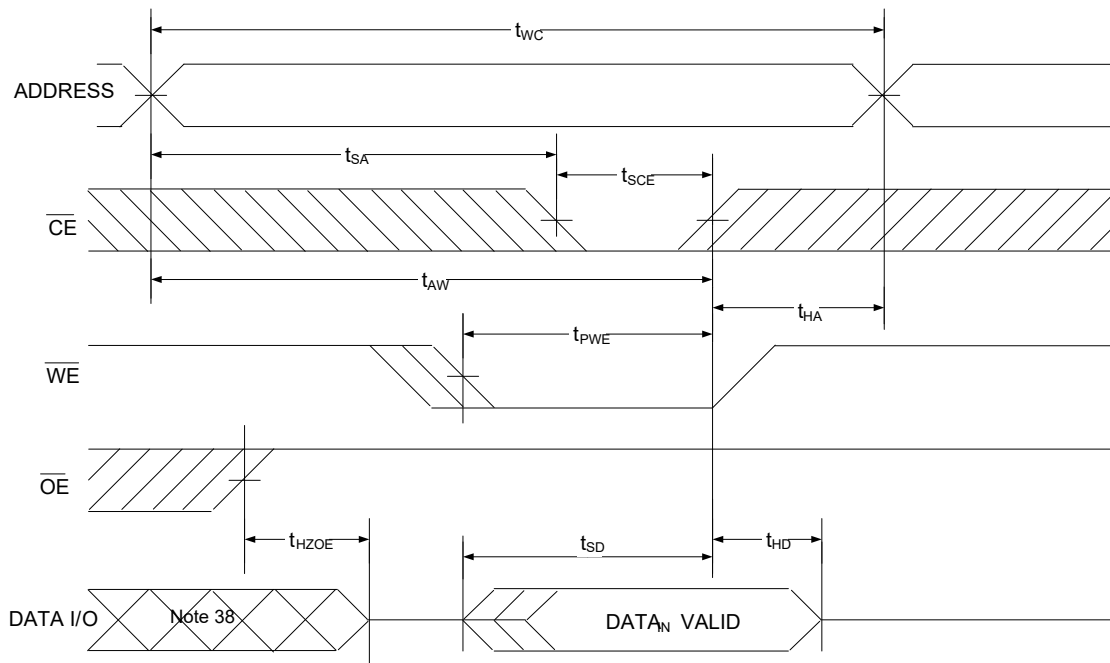


Figure 10. Write Cycle No. 3 ( $\overline{CE}$  Controlled)<sup>[34, 35, 36]</sup>



Notes

- 34. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 35. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 36. Data I/O is in high impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ .
- 37. The minimum write cycle pulse width should be equal to the sum of the  $t_{HZWE}$  and  $t_{SD}$ .
- 38. During this period I/O are in the output state. Do not apply input signals.

**Truth Table – CY62168G/CY62168GE**

| $\overline{CE}_1$ | $CE_2$            | $\overline{WE}$   | $\overline{OE}$   | I/Os   | Mode                | Power                       |
|-------------------|-------------------|-------------------|-------------------|--|---------------------|-----------------------------|
| H                 | X <sup>[39]</sup> | X <sup>[39]</sup> | X <sup>[39]</sup> | High Z   | Deselect/Power down | Standby (I <sub>SB2</sub> ) |
| X <sup>[39]</sup> | L                 | X <sup>[39]</sup> | X <sup>[39]</sup> | High Z   | Deselect/Power down | Standby (I <sub>SB2</sub> ) |
| L                 | H                 | H                 | L                 | Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ) | Read                | Active (I <sub>CC</sub> )   |
| L                 | H                 | H                 | H                 | High Z   | Output disabled     | Active (I <sub>CC</sub> )   |
| L                 | H                 | L                 | X                 | Data In (I/O <sub>0</sub> –I/O <sub>7</sub> )  | Write               | Active (I <sub>CC</sub> )   |

**ERR Output – CY62168GE**

| Output <sup>[40]</sup> | Mode   |
|------------------------|--|
| 0                      | Read Operation, no single-bit error in the stored data.  |
| 1                      | Read Operation, single-bit error detected and corrected. |
| High Z                 | Device deselected/Outputs disabled/Write Operation.      |

**Note**

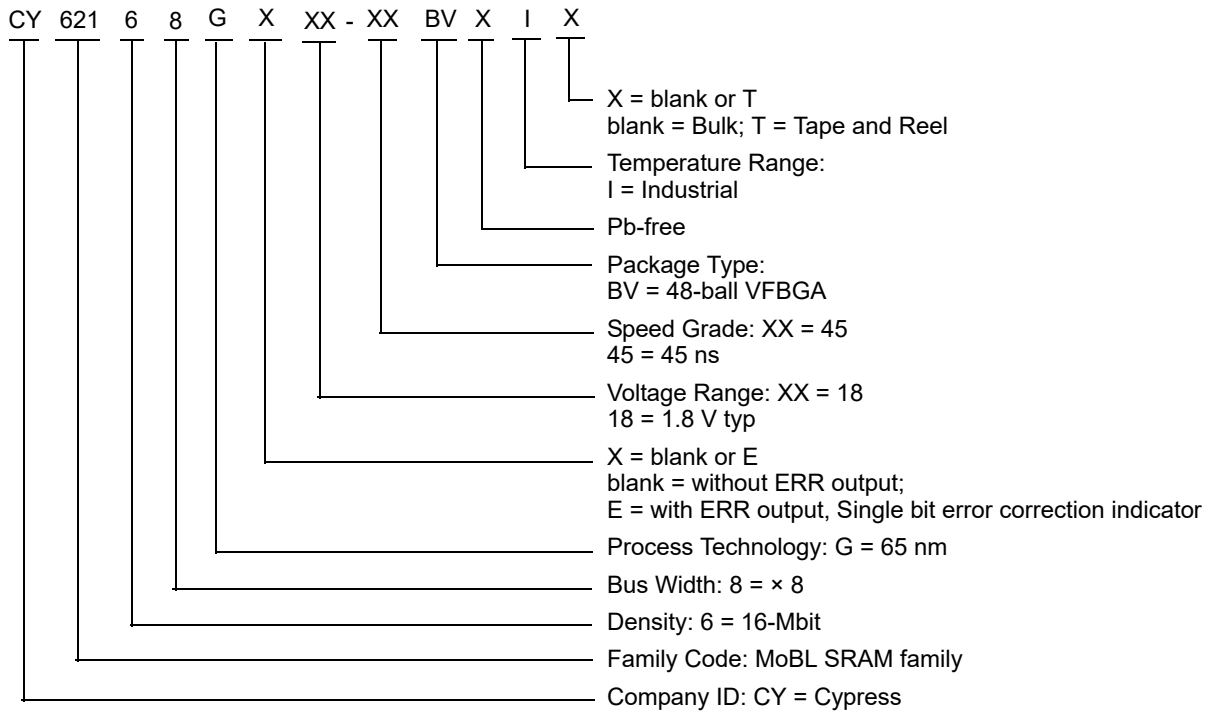
39. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

40. ERR is an Output pin. If not used, this pin should be left floating.

### Ordering Information

| Speed (ns) | Ordering Code      | Package Diagram | Package Type (all Pb-free)   | Operating Range |
|------------|--------------------|-----------------|------------------------------|-----------------|
| 55         | CY62168G18-55BVXI  | 51-85150        | 48-ball VFBGA                | Industrial      |
|            | CY62168G18-55BVXIT |                 | 48-ball VFBGA, Tape and Reel |                 |

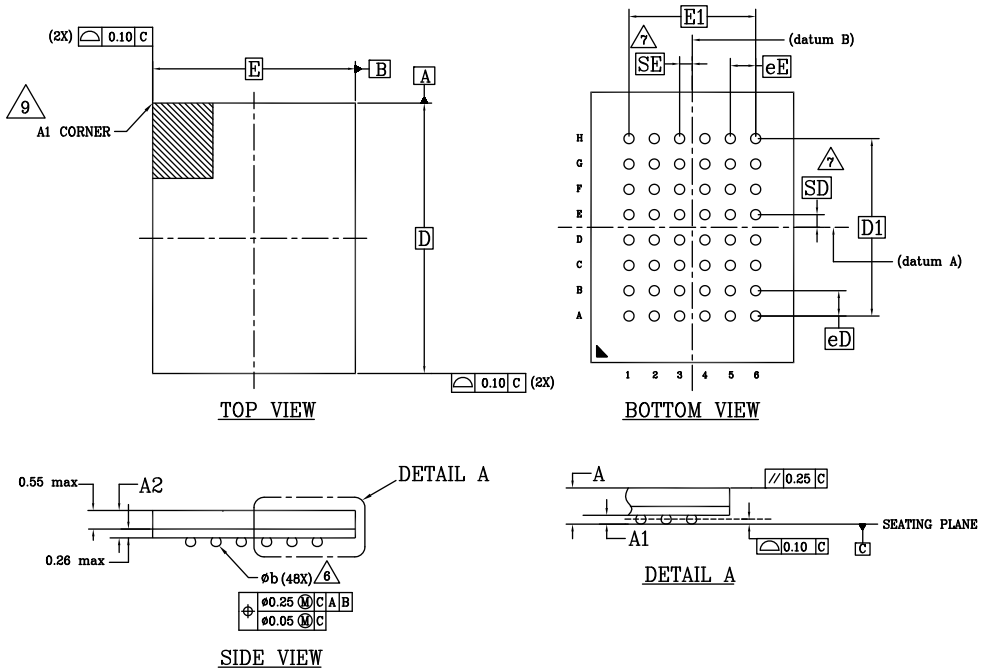
### Ordering Code Definitions





Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



| SYMBOL   | DIMENSIONS |      |      |
|----------|------------|------|------|
|          | MIN.       | NOM. | MAX. |
| A        | -          | -    | 1.00 |
| A1       | 0.16       | -    | -    |
| A2       | -          | -    | 0.81 |
| D        | 8.00 BSC   |      |      |
| E        | 6.00 BSC   |      |      |
| D1       | 5.25 BSC   |      |      |
| E1       | 3.75 BSC   |      |      |
| MD       | 8          |      |      |
| ME       | 6          |      |      |
| n        | 48         |      |      |
| $\phi b$ | 0.25       | 0.30 | 0.35 |
| eE       | 0.75 BSC   |      |      |
| eD       | 0.75 BSC   |      |      |
| SD       | 0.375 BSC  |      |      |
| SE       | 0.375 BSC  |      |      |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4.  $\square$  REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION, SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION, n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "\*" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 \*I

## Acronyms

| Acronym         | Description                             |
|-----------------|---|
| $\overline{CE}$ | Chip Enable                             |
| CMOS            | Complementary Metal Oxide Semiconductor |
| I/O             | Input/Output                            |
| $\overline{OE}$ | Output Enable                           |
| SRAM            | Static Random Access Memory             |
| VFBGA           | Very Fine-Pitch Ball Grid Array         |
| $\overline{WE}$ | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| μs     | microsecond     |
| mA     | milliampere     |
| mm     | millimeter      |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

Document History Page

| Document Title: CY62168G/CY62168GE MoBL, 16-Mbit (2M words × 8 bits) Static RAM with Error-Correcting Code (ECC)<br>Document Number: 001-84771 |         |                 |  |
|--|---------|-----------------|--|
| Rev.   | ECN No. | Submission Date | Description of Change  |
| *G   | 4800984 | 07/31/2015      | Changed status from Preliminary to Final.  |
| *H   | 5449003 | 11/03/2016      | <p>Updated <a href="#">Maximum Ratings</a>:<br/>           Updated Note 5 (Replaced “2 ns” with “20 ns”).<br/>           Updated <a href="#">DC Electrical Characteristics</a>:<br/>           Changed minimum value of V<sub>OH</sub> parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V”.<br/>           Changed minimum value of V<sub>IH</sub> parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”.<br/>           Updated <a href="#">Thermal Resistance</a>:<br/>           Replaced “two-layer” with “four-layer” in “Test Conditions” column.<br/>           Updated <a href="#">Ordering Information</a>:<br/>           Updated part numbers.<br/>           Updated <a href="#">Ordering Code Definitions</a>.<br/>           Updated to new template.<br/>           Completing Sunset Review.</p>   |
| *I   | 6003639 | 12/22/2017      | Updated Cypress Logo and Copyright.  |
| *J   | 6673157 | 09/25/2019      | <p>Updated <a href="#">Product Portfolio</a>:<br/>           Added Note “This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative.” and referred the same note in “CY62168G(E)30”.<br/>           Added Note “For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>.” and referred the same note in “CY62168G(E)30”.<br/>           Updated <a href="#">DC Electrical Characteristics</a>:<br/>           Added Note “This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative.” and referred the same note in I<sub>CC</sub>, I<sub>SB1</sub>, I<sub>SB2</sub> parameters.<br/>           Added Note “For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>.” and referred the same note in I<sub>CC</sub>, I<sub>SB1</sub>, I<sub>SB2</sub> parameters.<br/>           Updated <a href="#">Data Retention Characteristics</a>:<br/>           Added Note “This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative.” and referred the same note in I<sub>CCDR</sub> parameter.<br/>           Added Note “For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>.” and referred the same note in I<sub>CCDR</sub> parameter.<br/>           Updated <a href="#">Package Diagrams</a>:<br/>           spec 51-85150 – Changed revision from *H to *I.<br/>           Updated to new template.</p> |

**Document History Page** (continued)

| Document Title: CY62168G/CY62168GE MoBL, 16-Mbit (2M words × 8 bits) Static RAM with Error-Correcting Code (ECC)<br>Document Number: 001-84771 |         |                 |   |
|--|---------|-----------------|---|
| Rev.   | ECN No. | Submission Date | Description of Change   |
| *K   | 6816924 | 02/26/2020      | Removed CY62168G(E)30 part related information in all instances across the document.<br>Removed 2.2 V to 3.6 V Voltage Range related information in all instances across the document.<br>Updated <a href="#">Ordering Information</a> :<br>Updated part numbers.<br>Updated <a href="#">Ordering Code Definitions</a> .<br>Updated to new template.<br>Completing Sunset Review. |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

|                               |  |
|-------------------------------|--|
| Arm® Cortex® Microcontrollers | <a href="http://cypress.com/arm">cypress.com/arm</a>               |
| Automotive                    | <a href="http://cypress.com/automotive">cypress.com/automotive</a> |
| Clocks & Buffers              | <a href="http://cypress.com/clocks">cypress.com/clocks</a>         |
| Interface                     | <a href="http://cypress.com/interface">cypress.com/interface</a>   |
| Internet of Things            | <a href="http://cypress.com/iot">cypress.com/iot</a>               |
| Memory                        | <a href="http://cypress.com/memory">cypress.com/memory</a>         |
| Microcontrollers              | <a href="http://cypress.com/mcu">cypress.com/mcu</a>               |
| PSoC                          | <a href="http://cypress.com/psoc">cypress.com/psoc</a>             |
| Power Management ICs          | <a href="http://cypress.com/pmhc">cypress.com/pmhc</a>             |
| Touch Sensing                 | <a href="http://cypress.com/touch">cypress.com/touch</a>           |
| USB Controllers               | <a href="http://cypress.com/usb">cypress.com/usb</a>               |
| Wireless Connectivity         | <a href="http://cypress.com/wireless">cypress.com/wireless</a>     |

#### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

#### Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

#### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2012–2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.