OSD335x C-SiP Family

Rev. 9 10/5/2022

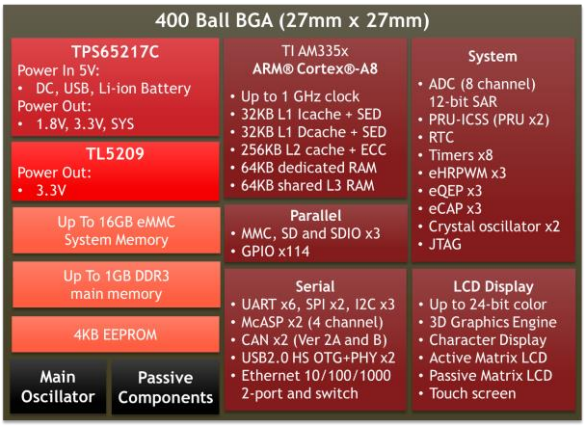
Introduction

The OSD335x C-SiP System-In-Package (SiP) is a self-contained computing system ideal to power the latest embedded applications. It integrates the powerful 1GHz Sitara™ ARM® Cortex®-A8 AM335x Processor from Texas Instruments, up to 1 Gigabyte (GB) of DDR3L memory, up to 16 Gigabytes (GB) of embedded Multimedia Card (eMMC) non-volatile memory, a low power, low jitter MEMs Oscillator, 4 Kilobytes (KB) EEPROM, TPS65217C PMIC, TL5209 LDO, and resistors, capacitors, and inductors into a single 27mm x 27mm easy to use IC package.

With this level of integration, the OSD335x C-SiP has everything needed to build a complete embedded computing platform. It allows designers to focus on the key aspects of their system without spending time on the complications associated with getting the processing core working. It also reduces the overall size and complexity of the design while simplifying the supply chain. The OSD335x C-SiP can significantly decrease the time to market for any embedded computing products.

Features

- TI AM335x, TPS65217C, TL5209, DDR3, EEPROM, eMMC, MEMS Oscillator and passive components integrated into a single package
- TI AM335x Features:
  - ARM® Cortex®-A8 up to 1GHz
  - 8 channel 12-bit SAR ADC
  - Ethernet 10/100/1000 x 2
  - USB 2.0 HS OTG + PHY x2
  - MMC, SD and SDIO x3
  - LCD Controller
  - SGX 3D Graphics Engine
  - PRU Subsystem



OSD335x C-SiP Block Diagram

- Access to all* AM335x Peripherals: CAN, SPI, UART, I2C, GPIO, etc.
- Up to 1GB DDR3
- Up to 16GB eMMC
- Low Power, Low Jitter MEMS Oscillator
- PWR In: AC Adapter, USB or Single cell (1S) Li-Ion / Li-Po Battery
- PWR Out: 1.8V, 3.3V and SYS
- Selectable I/O Voltage: 1.8V or 3.3V

Benefits

- Integrates over 100 components
- Compatible with AM335x development tools and software
- Significantly reduces design time
- 45% reduction in board space vs discrete implementation
- Decreases layout complexity
- Wide BGA ball pitch allows for low-cost assembly
- Simplifies component sourcing
- Increased reliability through reduced number of components

Package

- 400 Ball BGA (27mm X 27mm)
- 20 X 20 grid, 1.27mm pitch
- Temp Range: 0 to 85°C, -40 to 85°C

** Access to All IO except those used for communicating with the eMMC*

Table of Contents

1 Revision History

Revision Number	Revision Date	Changes	Author
1	3/19/2019	Initial Release	Greg Sheridan, Erik Welsh, Eshtaartha Basu
2	3/20/2019	Added VIN_BAT Information; Removed RTC-only information	Erik Welsh
3	3/16/2020	Changed eMMC IO domain	Neeraj Dantu
4	8/10/2020	Updated Oscillator Specs	Greg Sheridan
5	1/1/2020	Added more Reference Documents, Updated Table 5.6 USB descriptions, added information on Landing Pad Sizes	Gene Frantz
6	6/23/2021	Updated Oscillator Specifications	Greg Sheridan
7	11/17/2021	Added Trim Option	Greg Sheridan
8	4/1/2022	Updated Storage Requirements, Added In-rush current and Rise time Requirements, updated SYS_VDD3_3P3V and SYS_VDD_1P8V	Greg Sheridan
9	10/4/2022	Added PMIC I2C address Updated Trim Table Added Notes about using an external oscillator	Eshtaartha Basu Greg Sheridan Erik Welsh

2 Block Diagram

The OSD335x C-SiP devices consist of 7 main components serving 6 distinct functions. The main processor is a 1GHz Texas Instruments Sitara™ AM335x ARM® Cortex®-A8. The power system has 2 devices from Texas Instruments, the TPS65217C Power Management IC (PMIC) and the TL5209 LDO. The system memory includes up to 1GB DDR3. A combination of a 4KB EEPROM and up to 16GB of Embedded Multimedia Card (eMMC) provide nonvolatile memory for configuration and storage. Finally, a low power, low jitter, highly stable MEMS CMOS Oscillator is used for the primary clock input. Figure 2-1 shows a detailed block diagram of the OSD335x C-SiP and breaks out the key functions of the AM335x processor.

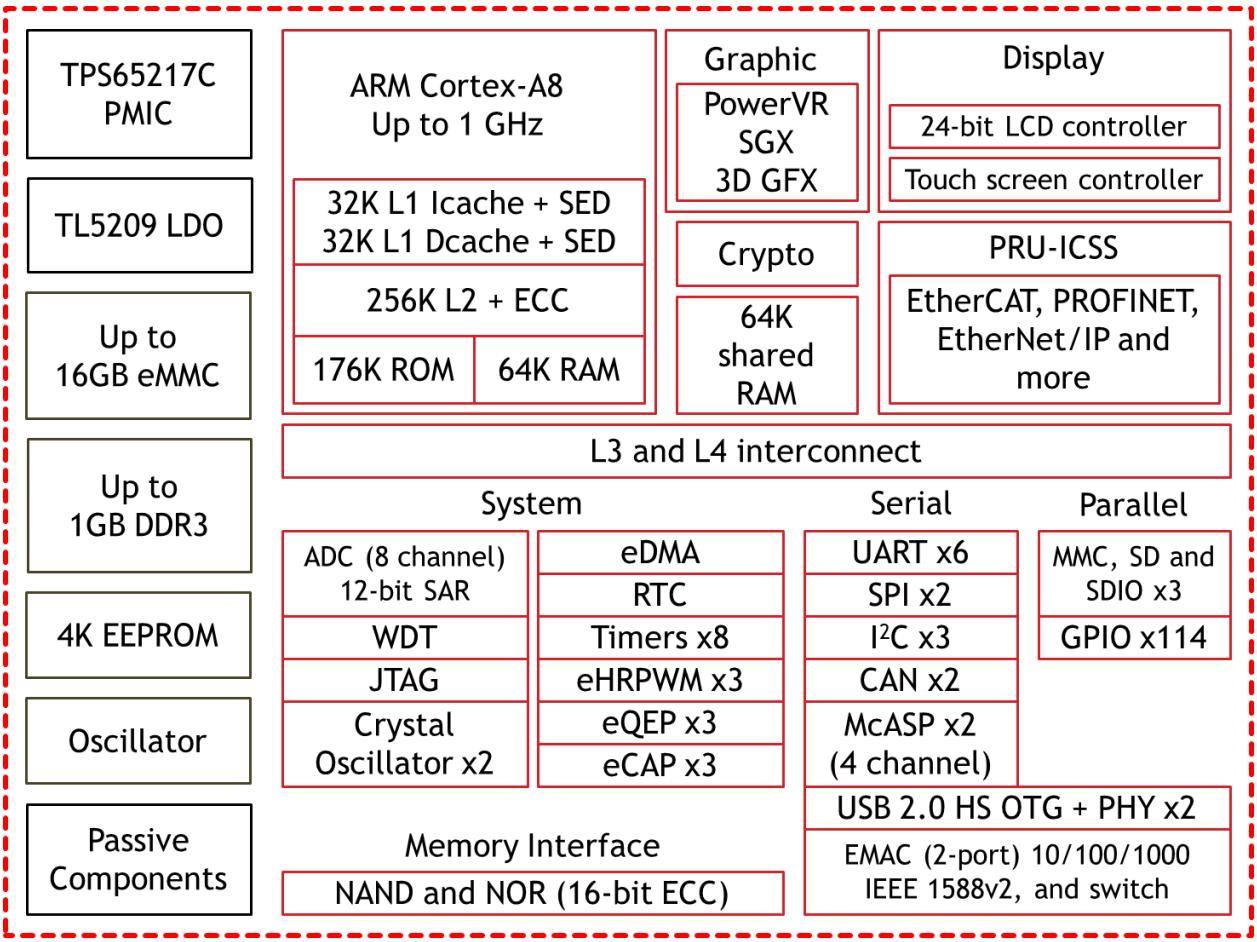


Figure 2-1 - OSD335x C-SiP Detailed Block Diagram

2.1 Passives

Besides the five major components, the OSD335x C-SiP also integrates capacitors, resistors, inductors, and ferrite beads (Passives). Table 2-2 and Table 2-3 lists the equivalent capacitance and resistance integrated into the OSD335x C-SiP. This includes the approximate bulk capacitance on input and output power rails as well as all pull-up resistor locations and values. The OSD335x C-SiP does not require any external decoupling / bypass capacitors in most applications. However, it does require additional bulk capacitance on one of the output power rails.

2.1.1 Additional Required Bulk Capacitance

The following output power rails require additional bulk capacitance to avoid in-rush / power up issues.

Table 2-1 - OSD335x C-SiP Required Additional Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
SYS_VOUT	DGND	TPS65217C	SYS_VOUT output capacitance	C	~50uF

2.1.2 Integrated Bulk Capacitance

The following input and output power rails have bulk capacitance integrated within the SiP. This table is for informative purposes only.

Table 2-2 - OSD335x C-SiP Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
VIN_AC	DGND	TPS65217C	VIN_AC input capacitance	C	10uF
VIN_USB	DGND	TPS65217C	VIN_USB input capacitance	C	10uF
VIN_BAT	DGND	TPS65217C	VIN_BAT input capacitance	C	10uF
SYS_VOUT	DGND	TPS65217C	SYS_VOUT output capacitance	C	20uF
SYS_VDD1_3P3V	DGND	TL5209	SYS_VDD1_3P3V output capacitance	C	2.2uF
SYS_VDD2_3P3V	DGND	TPS65217C	SYS_VDD2_3P3V output capacitance	C	2.2uF
SYS_VDD3_3P3V	DGND	TPS65217C	SYS_VDD3_3P3V output capacitance	C	10uF
SYS_VDD_1P8V	DGND	TPS65217C	SYS_VDD_1P8V output capacitance	C	10uF
SYS_RTC_1P8V	DGND	TPS65217C	SYS_RTC_1P8V output capacitance	C	2.2uF
CAP_VDD_RTC	DGND	AM335x	CAP_VDD_RTC capacitance	C	1uF
EMMC_VCC	DGND	eMMC	EMMC_VCC input capacitance	C	2.2uF
EMMC_VCCQ	DGND	eMMC	EMMC_VCCQ input capacitance	C	2.2uF

2.1.3 Integrated Resistors

The following pins have pull-up or pull-down resistors integrated within the SiP. This table is for informative purposes only.

Table 2-3 - OSD335x C-SiP Resistors (Pull-ups / Pull-downs)

From	To	Device	Description	Type	Value
PMIC_PWR_EN	SYS_RTC_1P8V	TPS65217C	PWR_EN pull-up	R	100K Ohm
EXT_WAKEUP	SYS_RTC_1P8V	AM335x	EXT_WAKEUP input pull-up	R	4.7K Ohm
EXTINTIN	VDDSHV6	AM335x	nNMI pull-up	R	4.7K Ohm
I2C0_SCL	VDDSHV6	AM335x	I2C0 SCL pull-up	R	4.7K Ohm
I2C0_SDA	VDDSHV6	AM335x	I2C0 SDA pull-up	R	4.7K Ohm
LCD_DATA14	VDDSHV6	AM335x	SYSBOOT[14] pull-up	R	100K Ohm
LCD_DATA15	GND	AM335x	SYSBOOT[15] pull-down	R	100K Ohm
PWRONRSTN_OD	VDDSHV6	SN74LVC07G	Open-drain buffered output of PWRONRSTN pull-up	R	10K Ohm
EEPROM_WP	VDDSHV6	EEPROM	EEPROM WP pull-up	R	4.7K Ohm
EMMC_RSTN	EMMC_VCCQ	eMMC	eMMC reset pull-up	R	10K Ohm
SYS_VDD1_CTL	SYS_VDD3_3P3V	TL5209	Enable pull-up	R	100K Ohm
OSC0_CTL	SYS_VDD_1P8V	Oscillator	Enable pull-up	R	10K Ohm

3 Product Number Information

Figure 3-1 shows an example of an orderable product number for the OSD335x C-SiP family. This section explains the different sections of the product number. It will also list the valid entries and their meaning for each designator.

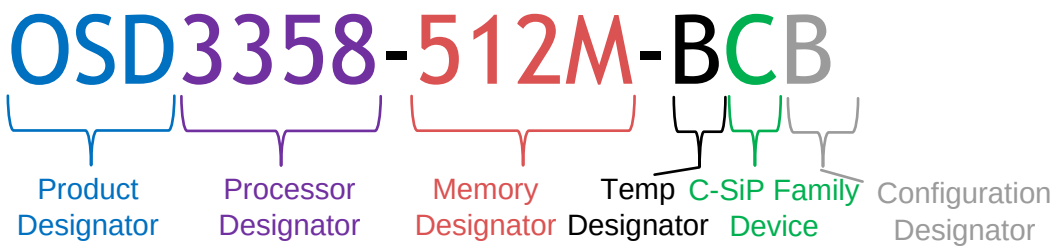


Figure 3-1. Example Product Number

Product Designator – Three letters that designate the family of device.

Table 3-1 - Family Designator

Family Designator	Product Line
OSD	OSD Product Line.

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 3-2 shows the valid values for the Processor Designator.

Table 3-2 - Processor Designators

Processor Designator	Processor
3358	Texas Instruments AM3358

Memory Designator – A set of letters and numbers that designate the DDR3 memory size in the device. Table 3-3 shows the valid values for the Memory Designator.

Table 3-3 - Memory Designator

Memory Designator	DDR Memory Size
1G	1GB DDR3
512M	512 MB DDR3

Temp Designator – A letter or number that designates the temperature range of the device. Table 3-4 shows the valid values for the Temp Designator.

Table 3-4 - Temp Designator

Temp Designator	Temperature Range
B	Commercial: 0 to 85°C
I	Industrial: -40 to 85°C

Configuration Designator – A letter or number that designates the set of features in the device. Table 3-5 shows the valid values for the Configuration Designator unique for the OSD335x C-SiP Family.

Table 3-5 - Trim Designator

Trim Designator	Device Options
B	24MHz Oscillator (Max Freq. Stability: 50 ppm), 4KB EEPROM, 4GB eMMC
C	24MHz Oscillator (Max Freq. Stability: 25 ppm), 4KB EEPROM, 4GB eMMC
E	24MHz Oscillator (Max Freq. Stability: 50 ppm), 4GB eMMC

4 Reference Documents

4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD335x C-SiP. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD335x C-SiP system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD335x C-SiP.

- Processor AM335X http://www.ti.com/product/am3358/datasheet
- PMIC TPS62517C http://www.ti.com/product/TPS65217/datasheet
- LDO TL509 http://www.ti.com/product/TL5209/datasheet
- EEPROM 24LC32A http://www.microchip.com/wwwproducts/en/24LC32A

4.2 Other References

This section contains links to other reference documents that could be helpful when using the OSD335x C-SiP device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations
  http://www.ti.com/lit/snoa550
- OSD335x C-SiP Pin Assignments and Application Differences from TI AM3358
  https://octavosystems.com/app_notes/osd335x-c-sip-family-pin-assignments/
- OSD335x C-SiP Layout Guide
  https://octavosystems.com/app_notes/osd335x-c-sip-layout-guide/
- AM335x DDR PHY register configuration for DDR3 using Software Leveling
  http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling
- AM335x Power Estimation Tool
  http://processors.wiki.ti.com/index.php/AM335x_Power_Estimation_Tool
- Powering the AM335x with the TPS65217x
  http://www.ti.com/lit/slvu551
- OSD3358-SM Reference, Evaluation and Development Platform
  https://octavosystems.com/octavo_products/osd3358-sm-red/
- AM335x and AMIC110 Sitara Processors Technical Reference Manual
  http://www.ti.com/lit/SPRUH73
- Powering the AM335x, AM335x, with LiPo and Li-Ion Batteries
  https://octavosystems.com/app_notes/am335x-battery-applications-with-osd335x-sip/
- OSD335x RTC Use Cases
  https://octavosystems.com/app_notes/osd335x-rtc-use-cases/

5 Ball Map

The pins on the OSD335x C-SiP belong to 4 distinct categories, AM335x Signals, TPS65217C signals, control signals for internal components and Power Domains. The signal names for the AM335x and the TPS65217C have been named so they can be easily cross-referenced to the corresponding pin in the TI Datasheet.

All AM335x signals on the OSD335x C-SiP Ball Map match the signal names of the default functions in the AM335x datasheet.

All the TPS65217C signals have the prefix PMIC_ then the TPS65217C signal name from the TI Datasheet.

NOTE: This is true except for the signal PMIC_POWER_EN which is an AM335x signal.

The arrangement of the signals has been optimized for easy escape of the BGA. Table 5-1 through Table 5-5 show the ball map for the OSD335x C-SiP.

Table 5-1 - OSD335x C-SiP Ball Map Top View (Columns A-D)

	A	B	C	D
20	DGND	VIN_USB	VIN_AC	VIN_BAT
19	PMIC_NRESET	VIN_USB	VIN_AC	VIN_BAT
18	PMIC_PB_IN	VIN_USB	VIN_AC	VIN_BAT
17	GPMC_AD8	WARMRSTN	PWRONRSTN_OD	DGND
16	GPMC_AD11	GPMC_AD10	GPMC_AD9	DGND
15	GPMC_AD14	GPMC_AD13	GPMC_AD12	DGND
14	GPMC_CLK	GPMC_CSN3	GPMC_AD15	PMIC_LDO_PGOOD
13	GPMC_A0	GPMC_A1	GPMC_A2	RTC_PWRONRSTN
12	GPMC_A3	GPMC_A4	GPMC_A5	PMIC_PGOOD
11	GPMC_A6	GPMC_A7	GPMC_A8	PWRONRSTN
10	GPMC_A9	GPMC_A10	GPMC_A11	PMIC_PWR_EN
9	GPMC_WPN	GPMC_WAIT0	GPMC_BEN1	PMIC_POWER_EN
8	NC	NC	NC	NC
7	NC	NC	NC	NC
6	NC	NC	NC	NC
5	NC	NC	NC	DGND
4	EMMC_RSTN	NC	NC	DGND
3	NC	NC	NC	NC
2	NC	NC	NC	NC
1	DGND	NC	NC	NC

Table 5-2 - OSD335x C-SiP Ball Map Top View (Columns E-H)

	E	F	G	H
20	PMIC_TS	NC	NC	NC
19	PMIC_BAT_SENSE	PMIC_MUX_IN	NC	NC
18	NC	SYS_VDD1_CTL	NC	NC
17	DGND	DGND	PMIC_NWAKEUP	EXT_WAKEUP
16	DGND	DGND	DGND	DGND
15	DGND	SYS_VOUT	SYS_VOUT	SYS_VDD1_3P3V
14	DGND	SYS_VOUT	SYS_VOUT	SYS_VDD1_3P3V
13	DGND	SYS_VDD2_3P3V	SYS_VDD2_3P3V	NC
12	DGND	SYS_VDD2_3P3V	SYS_VDD2_3P3V	NC
11	DGND	DGND	NC	NC
10	DGND	DGND	NC	NC
9	DGND	EMMC_VCC	EMMC_VCC	NC
8	DGND	EMMC_VCC	EMMC_VCC	EMMC_VCCQ
7	DGND	NC	NC	EMMC_VCCQ
6	DGND	NC	NC	NC
5	DGND	DGND	DGND	DGND
4	DGND	NC	NC	NC
3	NC	NC	NC	USB1_DRVVBUS
2	NC	NC	NC	USB1_DM
1	NC	NC	NC	USB1_VBUS

Table 5-3 - OSD335x C-SiP Ball Map Top View (Columns J-M)

	J	K	L	M
20	NC	GPMC_CSN0	GPMC_BEN0_CLE	LCD_DATA14
19	NC	GPMC_OEN_REN	GPMC_ADVN_ALE	LCD_DATA13
18	NC	GPMC_WEN	LCD_DATA15	LCD_DATA12
17	PMIC_NINT	EXTINTN	NC	NC
16	DGND	DGND	DGND	DGND
15	SYS_VDD1_3P3V	DGND	DGND	DGND
14	SYS_VDD1_3P3V	SYS_RTC_1P8V	SYS_RTC_1P8V	VDDS
13	DGND	SYS_RTC_1P8V	SYS_RTC_1P8V	VDDS_RTC
12	DGND	DGND	SYS_VDD3_3P3V	VDDSHV6
11	DGND	SYS_VDD3_3P3V	SYS_VDD3_3P3V	VDDSHV1
10	DGND	SYS_VDD3_3P3V	SYS_VDD3_3P3V	VDDSHV2
9	DGND	DGND	SYS_VDD3_3P3V	VDDSHV3
8	EMMC_VCCQ	DGND	SYS_VDD3_3P3V	VDDSHV5
7	EMMC_VCCQ	DGND	SYS_VDD3_3P3V	VDDSHV4
6	NC	DGND	DGND	OSC0_TP
5	DGND	DGND	DGND	DGND
4	NC	NC	NC	NC
3	USB1_CE	USB0_DRVVBUS	USB0_CE	RMII1_REF_CLK
2	USB1_DP	USB0_DM	USB0_DP	EEPROM_WP
1	USB1_ID	USB0_VBUS	USB0_ID	OSC0_CTL

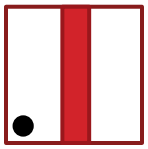


Table 5-4 - OSD335x C-SiP Ball Map Top View (Columns N-T)

	N	P	R	T
20	LCD_DATA11	LCD_DATA8	LCD_DATA5	LCD_DATA2
19	LCD_DATA10	LCD_DATA7	LCD_DATA4	LCD_DATA1
18	LCD_DATA9	LCD_DATA6	LCD_DATA3	LCD_DATA0
17	NC	NC	NC	DGND
16	DGND	DGND	DGND	DGND
15	DGND	DGND	NC	DGND
14	SYS_VDD_1P8V	DGND	NC	DGND
13	SYS_VDD_1P8V	DGND	VPP	DGND
12	SYS_VDD_1P8V	DGND	DGND	DGND
11	SYS_VDD_1P8V	SYS_VDD_1P8V	DGND	DGND
10	SYS_VDD_1P8V	SYS_VDD_1P8V	DGND	DGND
9	SYS_VDD_1P8V	DGND	DGND	DGND
8	SYS_VDD_1P8V	DGND	NC	DGND
7	SYS_VDD_1P8V	DGND	NC	DGND
6	DGND	DGND	NC	DGND
5	DGND	DGND	DGND	DGND
4	NC	NC	NC	DGND
3	MII1_TXD1	MII1_TX_EN	MII1_CRS	MII1_RXD0
2	MII1_TXD0	MII1_TXD3	MII1_COL	MII1_RX_ER
1	MII1_TX_CLK	MII1_TXD2	MII1_RX_DV	MII1_RX_CLK

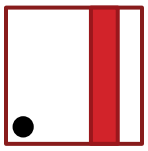
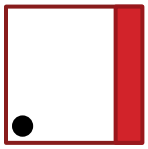


Table 5-5 - OSD335x C-SiP Ball Map Top View (Columns U-Y)

	U	V	W	Y
20	LCD_PCLK	LCD_AC_BIAS_EN	TRSTN	DGND
19	LCD_HSYNC	EMU1	TMS	TCK
18	LCD_VSYNC	EMU0	TDO	TDI
17	DGND	MCASP0_AXR1	MCASP0_AHCLKR	MCASP0_ACLKX
16	DGND	MCASP0_AHCLKX	MCASP0_AXR0	MCASP0_FSX
15	RTC_KALDO_ENN	ECAP0_IN_PWM0_OUT	MCASP0_FSR	MCASP0_ACLKR
14	VDDS_RTC	XDMA_EVENT_INTR1	XDMA_EVENT_INTR0	OSC1_OUT
13	VDD_CORE	CAP_VDD_RTC	OSC1_GND	OSC1_IN
12	PMIC_MUX_OUT	AIN7	VREFP	SYS_ADC_1P8V
11	NC	AIN6	AIN5	AIN4
10	VDDS_PLL	AIN2	AIN1	AIN0
9	VDDS_DDR	AIN3	VREFN	AGND_ADC
8	PMIC_SCL	I2C0_SCL	UART1_CTSN	UART1_RTSN
7	PMIC_SDA	I2C0_SDA	UART1_TXD	UART1_RXD
6	VDD_MPU	UART0_CTSN	UART0_TXD	UART0_RXD
5	DGND	UART0_RTSN	SPI0_D0	SPI0_SCLK
4	DGND	SPI0_CS1	SPI0_D1	SPI0_CS0
3	MII1_RXD3	MMC0_DAT1	MMC0_CLK	MMC0_DAT0
2	MII1_RXD2	MMC0_DAT2	MMC0_CMD	MMC0_DAT3
1	MII1_RXD1	MDIO	MDC	DGND



5.1 Ball Description

Table 5-6 lists all the unique balls of the OSD335x C-SiP and gives their primary, i.e. pin mux mode 0, function. Most pins have multiple functions muxed together which can be selected by setting the appropriate pin muxing mode. The table also lists the equivalent pin number for the signal on the OSD335x C-SiP package and the AM335x ZCZ package. For more detail please refer to the appropriate datasheet in section 4.1. Also, please refer to the AM335x datasheet Table 4-1 for more information on the different pin muxing modes.

Table 5-6 - OSD335x C-SiP Ball Descriptions

Pin Name	Description	Pin Number	
		OSD335x C-SiP	AM335x (ZCZ)
AGND_ADC	Analog Ground (VSSA_ADC in AM335x)	Y9	E8
AIN0	Analog Input / Output	Y10	B6
AIN1	Analog Input / Output	W10	C7
AIN2	Analog Input / Output	V10	B7
AIN3	Analog Input / Output	V9	A7
AIN4	Analog Input / Output	Y11	C8
AIN5	Analog Input	W11	B8
AIN6	Analog Input	V11	A8
AIN7	Analog Input	V12	C9
CAP_VDD_RTC	RTC Supply Voltage Input	V13	D6
DGND	Digital Ground (VSS in AM335x)	See Ball Map for all DGND instances	See VSS pin in AM335x datasheet.
ECAP0_IN_PWM0_OUT	Enhanced Capture 0 Input or PWM0 Output	V15	C18
EEPROM_WP	EEPROM Write Protect Pin	M2	N/A
EMMC_RSTN	eMMC RESETN Input	A4	N/A
EMMC_VCC	eMMC VCC Input (3.3V)	F9, F8, G9, G8	N/A
EMMC_VCCQ	eMMC VCC I/O Input (3.3V)	H8, H7, J8, J7	N/A
EMU0	Miscellaneous Emulation Pin	V18	C14
EMU1	Miscellaneous Emulation Pin	V19	B14
EXTINTN	AM335x External Interrupt to ARM Cortex-A8	K17	B18
EXT_WAKEUP	AM335x EXT_WAKEUP Input	H17	C5
GPMC_A0	GPMC Address	A13	R13
GPMC_A1	GPMC Address	B13	V14
GPMC_A2	GPMC Address	C13	U14
GPMC_A3	GPMC Address	A12	T14
GPMC_A4	GPMC Address	B12	R14
GPMC_A5	GPMC Address	C12	V15
GPMC_A6	GPMC Address	A11	U15
GPMC_A7	GPMC Address	B11	T15
GPMC_A8	GPMC Address	C11	V16
GPMC_A9	GPMC Address	A10	U16
GPMC_A10	GPMC Address	B10	T16
GPMC_A11	GPMC Address	C10	V17
GPMC_AD8	GPMC Address and Data	A17	U10
GPMC_AD9	GPMC Address and Data	C16	T10
GPMC_AD10	GPMC Address and Data	B16	T11
GPMC_AD11	GPMC Address and Data	A16	U12
GPMC_AD12	GPMC Address and Data	C15	T12
GPMC_AD13	GPMC Address and Data	B15	R12
GPMC_AD14	GPMC Address and Data	A15	V13
GPMC_AD15	GPMC Address and Data	C14	U13
GPMC_ADVN_ALE	GPMC Address Valid / Address Latch Enable	L19	R7
GPMC_BEN0_CLE	GPMC Byte Enable 0 / Command Latch Enable	L20	T6
GPMC_BEN1	GPMC Byte Enable 1	C9	U18
GPMC_CLK	GPMC Clock	A14	V12
GPMC_CSN0	GPMC Chip Select	K20	V6
GPMC_CSN3	GPMC Chip Select	B14	T13

GPMC_OEN_REN	GPMC Output Enable / Read Enable	K19	T7
GPMC_WAIT0	GPMC Wait 0	B9	T17
GPMC_WEN	GPMC Write Enable	K18	U6
GPMC_WPN	GPMC Write Protect	A9	U17
I2C0_SCL	I2C Clock	V8	C16
I2C0_SDA	I2C Data	V7	C17
LCD_AC_BIAS_EN	LCD AC Bias Enable Chip Select	V20	R6
LCD_DATA0	LCD Data Bus	T18	R1
LCD_DATA1	LCD Data Bus	T19	R2
LCD_DATA2	LCD Data Bus	T20	R3
LCD_DATA3	LCD Data Bus	R18	R4
LCD_DATA4	LCD Data Bus	R19	T1
LCD_DATA5	LCD Data Bus	R20	T2
LCD_DATA6	LCD Data Bus	P18	T3
LCD_DATA7	LCD Data Bus	P19	T4
LCD_DATA8	LCD Data Bus	P20	U1
LCD_DATA9	LCD Data Bus	N18	U2
LCD_DATA10	LCD Data Bus	N19	U3
LCD_DATA11	LCD Data Bus	N20	U4
LCD_DATA12	LCD Data Bus	M18	V2
LCD_DATA13	LCD Data Bus	M19	V3
LCD_DATA14	LCD Data Bus	M20	V4
LCD_DATA15	LCD Data Bus	L18	T5
LCD_HSYNC	LCD Horizontal Sync	U19	R5
LCD_PCLK	LCD Pixel Clock	U20	V5
LCD_VSYNC	LCD Vertical Sync	U18	U5
MCASP0_ACLKR	McASP0 Receive Bit Clock	Y15	B12
MCASP0_ACLKX	McASP0 Transmit Bit Clock	Y17	A13
MCASP0_AHCLKR	McASP0 Receive Master Clock	W17	C12
MCASP0_AHCLKX	McASP0 Transmit Master Clock	V16	A14
MCASP0_AXR0	McASP0 Serial Data	W16	D12
MCASP0_AXR1	McASP0 Serial Data	V17	D13
MCASP0_FSR	McASP0 Receive Frame Sync	W15	C13
MCASP0_FSX	McASP0 Transmit Frame Sync	Y16	B13
MDC	MDIO Clock	W1	M18
MDIO	MDIO Data	V1	M17
MII1_COL	MII Collision	R2	H16
MII1_CRS	MII Carrier Sense	R3	H17
MII1_RX_CLK	MII Receive Clock	T1	L18
MII1_RX_DV	MII Receive Data Valid	R1	J17
MII1_RX_ER	MII Receive Data Error	T2	J15
MII1_RXD0	MII Receive Data	T3	M16
MII1_RXD1	MII Receive Data	U1	L15
MII1_RXD2	MII Receive Data	U2	L16
MII1_RXD3	MII Receive Data	U3	L17
MII1_TX_CLK	MII Transmit Clock	N1	K18
MII1_TX_EN	MII Transmit Enable	P3	J16
MII1_TXD0	MII Transmit Data	N2	K17
MII1_TXD1	MII Transmit Data	N3	K16
MII1_TXD2	MII Transmit Data	P1	K15
MII1_TXD3	MII Transmit Data	P2	J18
MMC0_CLK	MMC/SD/SDIO Clock	W3	G17
MMC0_CMD	MMC/SD/SDIO Command	W2	G18
MMC0_DAT0	MMC/SD/SDIO Data	Y3	G16
MMC0_DAT1	MMC/SD/SDIO Data	V3	G15
MMC0_DAT2	MMC/SD/SDIO Data	V2	F18
MMC0_DAT3	MMC/SD/SDIO Data	Y2	F17
NC	Do Not Connect	See Ball Map for all NC instances	N/A
OSC0_CTL	High Frequency Oscillator enable (Pulled High)	M1	N/A
OSC0_TP	Internal Oscillator Test Point	M6	N/A
OSC1_GND	Real Time Clock Oscillator Ground (VSS_RTC)	W13	A5
OSC1_IN	Real Time Clock Oscillator Input (RTC_XTALIN)	Y13	A6

OSC1_OUT	Real Time Clock Oscillator Output (RTC_XTALOUT)	Y14	A4
PMIC_BAT_SENSE	TPS65217C BAT_SENSE Input	E19	N/A
PMIC_LDO_PGOOD	TPS65217C LDO_PGOOD Output	D14	N/A
PMIC_MUX_IN	TPS65217C MUX_IN Input	F19	N/A
PMIC_MUX_OUT	TPS65217C MUX_OUT Output	U12	N/A
PMIC_NINT	TPS65217C NINT Output	J17	N/A
PMIC_NRESET	TPS65217C NRESET Input	A19	N/A
PMIC_NWAKEUP	TPS65217C NWAKEUP Output	G17	N/A
PMIC_PB_IN	TPS65217C PB_IN Input	A18	N/A
PMIC_PGOOD	TPS65217C PGOOD Output	D12	N/A
PMIC_POWER_EN	AM335x PMIC_POWER_EN Output	D9	C6
PMIC_PWR_EN	TPS65217C PWR_EN Input	D10	N/A
PMIC_SCL	TPS65217C SCL Input	U8	N/A
PMIC_SDA	TPS65217C SDA Input / Output	U7	N/A
PMIC_TS	TPS65217C TS Input	E20	N/A
PWRONRSTN	Power On Reset Input (Active Low)	D11	B15
PWRONRSTN_OD	Open-Drain buffer output (Pulled High)	C17	N/A
RMII1_REF_CLK	RMII Reference Clock	M3	H18
RTC_KALDO_ENN	Enable input for internal CAP_VDD_RTC voltage regulator (Active Low)	U15	B4
RTC_PWRONRSTN	RTC Reset Input (Active Low)	D13	B5
SPI0_CS0	SPI Chip Select	Y4	A16
SPI0_CS1	SPI Chip Select	V4	C15
SPI0_D0	SPI Data	W5	B17
SPI0_D1	SPI Data	W4	B16
SPI0_SCLK	SPI Clock	Y5	A17
SYS_ADC_1P8V	Output Power Supply, Analog, 1.8VDC	Y12	N/A
SYS_RTC_1P8V	Output Power Supply, RTC, 1.8VDC	K14, K13, L14, L13	N/A
SYS_VDD_1P8V	Output Power Supply, Digital, 1.8VDC	N14, N13, N12, N11, N10, N9, N8, N7, P11, P10	N/A
SYS_VDD1_CTL	SYS_VDD1_3P3V enable (Pulled High)	F18	N/A
SYS_VDD1_3P3V	Output Power Supply, Primary, 3.3VDC	H15, H14, J15, J14	N/A
SYS_VDD2_3P3V	Output Power Supply, Secondary, 3.3VDC	F13, F12, G13, G12	N/A
SYS_VDD3_3P3V	Output Power Supply, I/O, 3.3VDC	K11, K10, L12, L11, L10, L9, L8, L7	N/A
SYS_VOUT	TPS65217C SYS Output	F15, F14, G15, G14	N/A
TCK	JTAG Test Clock	Y19	A12
TDI	JTAG Test Data Input	Y18	B11
TDO	JTAG Test Data Output	W18	A11
TMS	JTAG Test Mode Select	W19	C11
TRSTN	JTAG Test Reset	W20	B10
UART0_CTSN	UART Clear to Send	V6	E18
UART0_RTSN	UART Request to Send	V5	E17
UART0_RXD	UART Receive Data	Y6	E15
UART0_TXD	UART Transmit Data	W6	E16
UART1_CTSN	UART Clear to Send	W8	D18
UART1_RTSN	UART Request to Send	Y8	D17
UART1_RXD	UART Receive Data	Y7	D16
UART1_TXD	UART Transmit Data	W7	D15
USB0_CE	USB0 Charger Enable Output	L3	M15
USB0_DM	USB0 Data (-)	K2	N18
USB0_DP	USB0 Data (+)	L2	N17
USB0_DRVVBUS	USB0 VBUS Control Output. Driven high to enable external power logic in Host mode. Requires valid input on USB0_VBUS. Checks USB0_VBUS every 100ms and generates VBUS error interrupt if USB0_VBUS is not valid.	K3	F16
USB0_ID	USB0 OTG ID	L1	P16
USB0_VBUS	USB0 VBUS	K1	P15
USB1_CE	USB1 Charger Enable Output	J3	P18

USB1_DM	USB1 Data (-)	H2	R18
USB1_DP	USB1 Data (+)	J2	R17
USB1_DRVVBUS	USB1 VBUS Control Output. Driven high to enable external power logic in Host mode. Requires valid input on USB1_VBUS. Checks USB1_VBUS every 100ms and generates VBUS error interrupt if USB1_VBUS is not valid.	H3	F15
USB1_ID	USB1 OTG ID	J1	P17
USB1_VBUS	USB1 VBUS	H1	T18
VDD_CORE	Internal Power Supply Test Point	U13	N/A
VDD_MPU	Internal Power Supply Test Point	U6	N/A
VDDS_DDR	Internal Power Supply Test Point	U9	N/A
VDDS_PLL	Internal Power Supply Test Point	U10	N/A
VDDS_RTC	Supply voltage for RTC domain	M13, U14	D7
VDDS	Supply voltage for 1.8V IO domain	M14	E6, E14, F9, K13, N6, P9, P14
VDDSHV1	Supply voltage for the dual-voltage IO domain	M11	P7, P8
VDDSHV2	Supply voltage for the dual-voltage IO domain	M10	P10, P11
VDDSHV3	Supply voltage for the dual-voltage IO domain	M9	P12, P13
VDDSHV4	Supply voltage for the dual-voltage IO domain	M7	H14, J14
VDDSHV5	Supply voltage for the dual-voltage IO domain	M8	K14, L14
VDDSHV6	Supply voltage for the dual-voltage IO domain	M12	E10, E11, E12, E13, F14, G14, N5, P5, P6
VIN_AC	TPS65217C AC Input	C20, C19, C18	N/A
VIN_BAT	TPS65217C BAT Input / Output	D20, D19, D18	N/A
VIN_USB	TPS65217C USB Input	B20, B19, B18	N/A
VPP	Reserved	R13	M5
VREFN	Analog Negative Reference Input	W9	A9
VREFP	Analog Positive Reference Input	W12	B9
WARMRSTN	Warm Reset (Active Low)	B17	A10
XDMA_EVENT_INTR0	External DMA Event or Interrupt 0	W14	A15
XDMA_EVENT_INTR1	External DMA Event or Interrupt 1	V14	D14

5.2 Internal Use Only AM335x Signal Pins

The following signal pins of the AM335x ZCZ package are for internal use only within the OSD335x and are not made accessible to the user. These pins are connected to the eMMC module within the OSD335x C-SiP.

Table 5-7 - Internal Use Only AM335x Pins

Pin Name	Description	Pin Number	
		OSD335x C-SiP	AM335x (ZCZ)
GPMC_AD0	GPMC Address and Data	N/A	U7
GPMC_AD1	GPMC Address and Data	N/A	V7
GPMC_AD2	GPMC Address and Data	N/A	R8
GPMC_AD3	GPMC Address and Data	N/A	T8
GPMC_AD4	GPMC Address and Data	N/A	U8
GPMC_AD5	GPMC Address and Data	N/A	V8
GPMC_AD6	GPMC Address and Data	N/A	R9
GPMC_AD7	GPMC Address and Data	N/A	T9
GPMC_CSN1	GPMC Chip Select	N/A	U9
GPMC_CSN2	GPMC Chip Select	N/A	V9

5.3 Not Connected Balls

The OSD335x C-SiP ball map contains balls which are marked NC (No Connect). These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of the OSD335x C-SiP.

5.4 Reserved Signals

There is a subset of signals that are available on the OSD335x C-SiP ball map but ***should not be*** used externally to the device. These signals are used internally to the OSD335x C-SiP and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5-8.

Table 5-8 - Reserved Signals

Reserved Signals
VPP
VDD_CORE
VDD_MPU
VDDS_DDR
VDDS_PLL

6 OSD335x C-SiP Components

The OSD335x C-SiP integrates the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 GB of DDR3 Memory, a 4KB EEPROM and up to 16GB of eMMC memory for non-volatile storage, a MEMS Oscillator for the primary clock input, and the resistors, capacitors, and inductors into a single design-in-ready package. The following section contains any specific device information needed for the integrated components to design your system with the OSD335x C-SiP. Specifics on the Power Management System will be covered in Section 7.

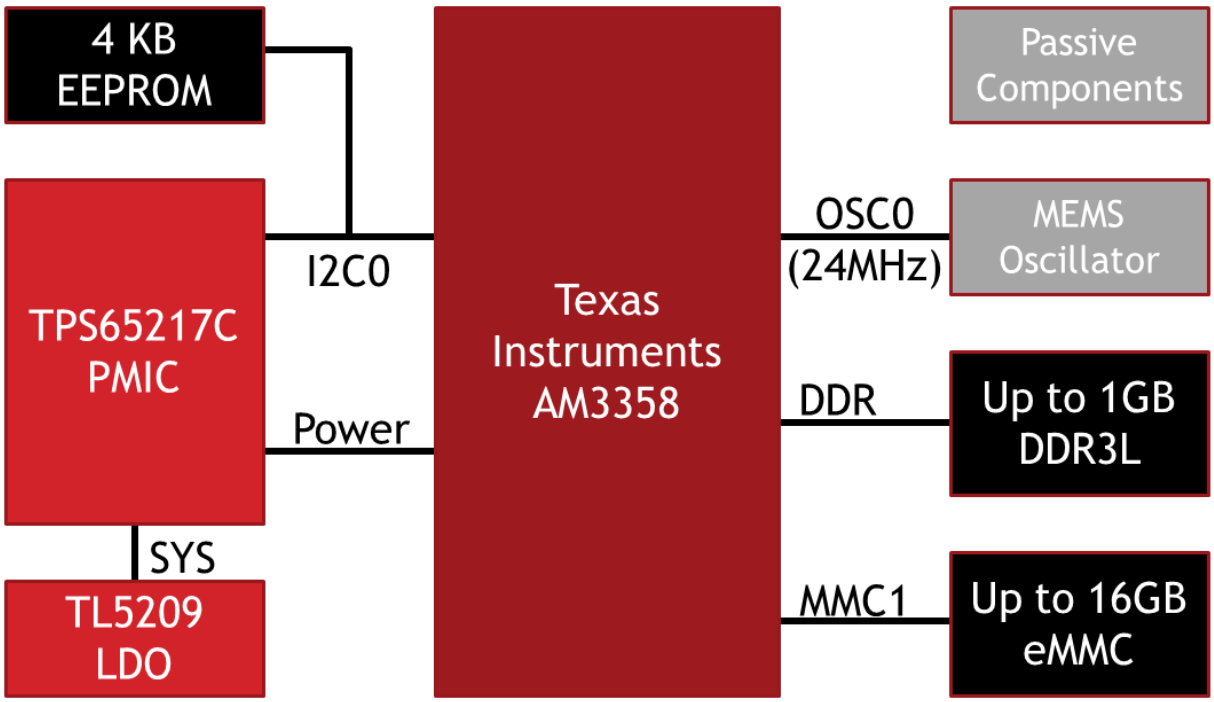


Figure 6-1 - OSD335x C-SiP Internal Connections Block Diagram

6.1 AM335x Processor

The heart of the OSD335x C-SiP is the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor. The processor in the OSD335x C-SiP is configured to perform identically to a standalone device. Please refer to the data sheet in the Reference Documents section for details on using the AM335x processor.

6.1.1 I/O Voltages

The OSD335x C-SiP allows the I/O voltage domains (VDDSHVx) of the AM335x to be set to either 1.8V or 3.3V. The VDDSHVx pins of the OSD335x C-SiP (ie VDDSHV1 thru VDDSHV6), which can be found in Table 5-6, must be connected to either a 1.8V or 3.3V power source in order to provide power to the I/Os. Recommendations on how to connect the I/O voltage domain pins is in section 7.5.2.

See the AM335x datasheet in the Reference Documents section for more information on the pins associated with each I/O voltage domain.

6.1.2 Reset Circuitry

The OSD335x C-SiP contains a SN74LVC1G07 open-drain buffer whose input is PWRONRSTN and whose output PWRONRSTN_OD is pulled to VDDHSV6 via a resistor (see Table 2-3 for more information). The PMIC_PGOOD, PWRONRSTN, PWRONRSTN_OD, and WARMRSTN signals can be connected as recommended in the AM335x Technical Reference Manual (see “External Buffer for nRESETIN_OUT” figure). This component is not required to be used, or can be used in conjunction with an external reset supervisor. Figure 6-2 shows the AM335x reset connections brought out to pins of the OSD335x C-SiP.

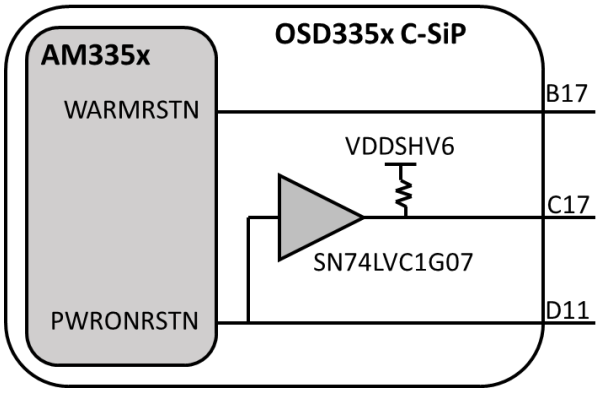


Figure 6-2 - OSD335x C-SiP Reset Circuitry

6.2 DDR3 Memory

The OSD335x C-SiP integrates a DDR3 memory into the device and handles all the connections needed between the AM335x and the DDR3. You will still have to set the proper registers to configure the AM335x DDR PHY to work correctly with the memory included in the OSD335x C-SiP. Typically, this would require you to run through the procedure outlined in the AM335x DDR PHY register configuration for DDR3 using Software Leveling referred to in the Reference Documents section of this document. This procedure has been run for the OSD335x C-SiP and a list of the recommended values for the registers is provided in Table 6-1. It is recommended that you use this set of values for optimal performance.

Table 6-1 - AM335x DDR EMIF, PHY and Control Module Register Settings

Register Name	Peripheral	Recommended Value
DDR_CMDx_IOCTRL(1)	Control Module	0x0000018B
DDR_DATAx_IOCTRL(2)	Control Module	0x0000018B
SDRAM_CONFIG	EMIF	0x61C05332
SDRAM_CONFIG_2	EMIF	0x00000000
SDRAM_REF_CTRL	EMIF	0x00000C30
SDRAM_TIM_1	EMIF	0x0AAAD4DB
SDRAM_TIM_2	EMIF	0x266B7FDA
SDRAM_TIM_3	EMIF	0x501F867F
ZQ_CONFIG	EMIF	0x50074BE4
DDR_PHY_CTRL_1	EMIF	0x00100007
CMDx_REG_PHY_CTRL_SLAVE_RATIO_0(1)	DDR PHY	0x00000080
CMDx_REG_PHY_INVERT_CLKOUT_0(1)	DDR PHY	0x00000000
DATAx_REG_PHY_RD_DQS_SLAVE_RATIO_0(2)	DDR PHY	0x0000003A
DATAx_REG_PHY_WR_DQS_SLAVE_RATIO_0(2)	DDR PHY	0x00000045
DATAx_REG_PHY_FIFO_WE_SLAVE_RATIO_0(2)	DDR PHY	0x00000095
DATAx_REG_PHY_WR_DATA_SLAVE_RATIO_0(2)	DDR PHY	0x0000007F

(1) "CMDx" refers to registers where x is in [0, 1, 2]
(2) "DATAx" refers to registers where x is in [0, 1]

Settings in Table 6-1 are recommended and supported. Other values may work but are not guaranteed. If you want to rerun the calibration yourself the seed values provided in Table 6-2 should be used.

Table 6-2 - AM335x DDR PHY Calibration Seed Values

DATAx_PHY_RD_DQS_SLAVE_RATIO	40
DATAx_PHY_FIFO_WE_SLAVE_RATIO	64
DATAx_PHY_WR_DQS_SLAVE_RATIO	0

6.3 MEMS Oscillator

The OSD335x C-SiP integrates a low power, low jitter MEMS Oscillator that provides the main input clock to the AM335x on OSC0. Oscillator parameters can be found in Table 6-3.

Table 6-3 - MEMS Oscillator Parameters

Parameter	Trim	Min	Typ	Max	Units	Notes
Active Supply Current			3.0	5.0	mA	
Frequency Stability	B\E			±50	ppm	All temp ranges
	C			±25		
Aging				±5	ppm	First year @ 25C
				±1	ppm	Per year after first year
Period Jitter, RMS				15	ps_{RMS}	
Cycle-to-Cycle Jitter				100	ps	
Frequency			24		MHz	

The MEMS Oscillator is the primary clock source for the AM335x. The boot mode resistors (SYSBOOT[15:14]) have already been set appropriately to match the oscillator frequency within the device (i.e. a value of 0b01 to signify a 24 MHz input). See Table 2-3 for more information on boot mode resistor values.

6.3.1 Using External Clock Source

If an application requires a different oscillator than the integrated MEMs Oscillator that is integrated within the OSD335x C-SiP, the oscillator can be disabled and an external oscillator can provide the clock source for the AM335x.

6.3.1.1 Disable the Internal MEMS Oscillator

Disable the internal MEMS oscillator by connecting the OSC_CTL pin to GND. This will set the output state of the internal MEMS oscillator to high impedance.

6.3.1.2 Connect External Oscillator

Connect a single ended oscillator that meets the specifications of the AM335x (See Section 6.2.2.2 OSC0 LVCMOS Digital Clock Source of the AM335x Datasheet) to the OSC0_TP pin.

NOTE: There is not access to XTALOUT of the AM335x so a crystal cannot be used as a clock source when the internal MEMS oscillator is not used.

NOTE: OSC0_TP is directly connected to XTALIN of the AM335x and there are no additional components on that connection except for the internal MEMS oscillator in the high impedance state, so any additional required components for the external oscillator should be also placed external to the OSD335x C-SiP.

6.3.1.3 Set oscillator Frequency

By default the OSD335x C-SiP is configured to use a 24MHz input clock by integrating 100k Ohm pull resistors on LCD_DATA15 and LCD_DATA14 that set the value of SYSBOOT[15:14] to "01".

If the clock frequency of the external clock is not 24MHz, then external 10k Ohm resistors should be used to change the value of LCD_DATA15 or LCD_DATA14.

For example, to use a 25MHz clock requires SYSBOOT[15:14] to be "10", so a 10k Ohm pull-up resistor would need to be added to LCD_DATA15 and a 10k ohm pull-down resistor would need to be added to LCD_DATA14 in order to set the value correctly.

NOTE: 10k Ohm external resistors will satisfy the VIH and VIL thresholds for the LCD data pins regardless of the corresponding VDDSHV voltage (See Section 5.7 DC Electrical Characteristics of the AM335x Datasheet). However, external components connected to LCD_DATA15 and LCD_DATA14 should be checked to ensure proper operation with the divided static values.

6.4 eMMC

The OSD335x C-SiP contains an Embedded Multimedia Card (eMMC) device connected to the MMC1 interface of the AM335x (See Table 5-7 for more information on the pins used to connect the eMMC). The AM335x supports version 4.3 of the MMC specification which is also supported by the eMMC. This large non-volatile storage medium can be used as the primary storage medium and boot device for the AM335x. It can hold an operating system such as Linux and/or be used for data storage.

The size of the eMMC is defined per the configuration outlined in Section 3. See the Minimum Connections section for required connections to use the eMMC.

6.4.1 Powering the eMMC

Both the EMMC_VCC and EMCC_VCCQ power inputs should be connected to SYS_VDD1_3P3V.

6.4.2 Booting from the eMMC

The eMMC is connected to the MMC1 interface of the AM335x. This interface is a boot source, meaning an operating system can be loaded onto the eMMC making it a completely self-contained computing device. To use the integrated eMMC as a boot source the boot resistors (SYSBOOT[4:0]) need to be set the following way:

Table 6-4 - eMMC Boot Modes

SYSBOOT[4:0]	**Boot Sequence**			
	1st	2nd	3rd	4th
11100b	MMC1	MMC0	UART0	USB0

This table does not represent all the options for the boot mode resistors. For more information on the Boot Mode resistors and the different boot mode options please refer to Booting Section in the AM335x and AMIC110 Sitara Processors Technical Reference Manual in the Other References Section.

It is not required that the integrated eMMC be used to boot the device. The OSD335x C-SiP supports all of the boot modes outlined in the AM335x and AMIC110 Sitara Processors Technical Reference Manual.

6.5 EEPROM

The OSD335x C-SiP contains a 4KB EEPROM for non-volatile storage of configuration information. The EEPROM is connected to I2C0 at the 7-bit I2C address 0x50 (0b1010000). Please refer to the data sheet in the Reference Documents section for details on using the EEPROM.

6.5.1 EEPROM Contents

EEPROM address space 0x000 to 0xEFF is empty and can be used for board specific information during system boot. The final 256 bytes of the EEPROM (0xF00 to 0xFFF) are reserved for device specific information. The reserved space contents of the EEPROM can be found in Table 6-5

Table 6-5 - EEPROM Contents Programmed by Octavo Systems

Name	Description	Size (bytes)	Start address	End address	Contents
RSVD	Reserved for Future Use	256	0xF00	0xFFF	All 0xFF

6.5.2 EEPROM Write Protection

By default, the EEPROM is write protected (ie. the EEPROM_WP pin is pulled high as seen in Table 2-2). To program values into the EEPROM, it is required to drive the EEPROM_WP pin to a logic low. See the OSD335x C-SiP Layout Guide in the Reference Documents section for layout / manufacturing recommendations for the EEPROM_WP pin.

7 Power Management

The power management portion of the OSD335x C-SiP consists of two devices, the TPS65217C (PMIC) and the TL5209 (LDO). The PMIC provides the necessary power rails to the AM335x and the DDR3 while the LDO is not used inside the SiP. Both devices provide power supply outputs that may be used to power circuitry external to the OSD335x C-SiP. The PMIC is connected to I2C0 at the 7-bit I2C address 0x24 (0b100100). This section describes how to power the OSD335x C-SiP in a system and the outputs that can be used.

7.1 Input Power

The OSD335x C-SiP may be powered by any combination of the following input power supplies. Please refer to the TPS65217C datasheet for details.

The maximum risetime for input rails VIN_AC and VIN_USB (defined as time for the input voltage to rise from 100 mV to 4.5 V) is 50 ms. The device may fail to power up properly if this requirement is not met.

7.1.1 VIN_AC

The OSD335x C-SiP may be powered by an external AC Adaptor at 5.0 VDC. If input is unused, it should be connected to DGND.

7.1.2 VIN_USB

The OSD335x C-SiP may be powered by a USB port at 5.0 VDC. If input is unused, it should be connected to DGND.

7.1.3 VIN_BAT

The OSD335x C-SiP may be powered by a single cell (1S) Li-Ion or Li-Polymer Battery nominally at 3.7 VDC.

Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS_VDD1_3P3V cannot be used once VIN_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.

When VIN_BAT is not used, it must be connected to PMIC_BAT_SENSE.

7.2 Output Power

The OSD335x C-SiP produces the following output power supplies.

7.2.1 SYS_VOUT: Switched VIN_AC, VIN_USB, or VIN_BAT

The OSD335x C-SiP contains a shared supply to power the AM335x, DDR3, and TL5209 which is also used to power external circuitry. This is supplied by the TPS65217C SYS output. The SYS output is a switched connection to one of the input power supplies selected by the TPS65217C as described in the datasheet for that device.

SYS_VOUT requires ~50uF of additional capacitance to maintain stability. This must be added externally.

7.2.2 SYS_VDD1_3P3V

The OSD335x C-SiP contains a dedicated 3.25 VDC supply[1] to power external circuitry. This is supplied by the TL5209, powered by the TPS65217C SYS output, and enabled by the TPS65217C LDO4.

Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS_VDD1_3P3V cannot be used once VIN_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.

7.2.3 SYS_VDD2_3P3V

The OSD335x C-SiP contains a dedicated 3.3 VDC supply to power external circuitry. This is supplied by the TPS65217C LDO2.

7.2.4 SYS_VDD3_3P3V

The OSD335x-SM contains a shared 3.3 VDC supply. It internally provides power to VDDA3P3V_USB0 and VDDA3P3V_USB1. It can also be used to power the AM335x I/O domains (VDDSHVx). This is supplied by the TPS65217C LDO4.

7.2.5 SYS_RTC_1P8V

The OSD335x-SM contains a shared 1.8 VDC supply to power the AM335x RTC, VDDA3P3V_USB0, and VDDA3P3V_USB1. It may also be used to power external circuitry. This is supplied by the TPS65217C LDO1.

Please note that the AM335x in the OSD335x is powered by TPS65217 PMIC **version C**. RTC-Only mode cannot be supported at this time.

7.2.6 SYS_VDD_1P8V

The OSD335x C-SiP contains a shared 1.8 VDC supply that may be used to power the AM335x I/O domains (VDDSHVx) and external circuitry. It also supplies power to the AM335x SRAM, PLLs and USB. This is supplied by the TPS65217C LDO3.

7.2.7 SYS_ADC_1P8V

The OSD335x C-SiP contains a shared 1.8 VDC supply to power the AM335x ADC which may also be used to power external analog circuitry. This is supplied by the TPS65217C LDO3 and filtered for analog applications.

7.3 Internal Power

The OSD335x C-SiP has internal power supplies that are not available to power external circuitry. To do so will prevent the OSD335x C-SiP from functioning properly. The power supplies are accessible externally for monitoring purposes only.

[1] The LDO has an accuracy of 1 – 2% depending on the ambient temperature which will also affect the nominal voltage. See the TL5209 datasheet for more information.

7.3.1 VDDS_DDR

The OSD335x C-SiP contains a dedicated 1.5 VDC supply to power the AM335x DDR3 interface and the DDR3 device. This is supplied by the TPS65217C DCDC1.

7.3.2 VDD_MPU

The OSD335x C-SiP contains a dedicated 1.1 VDC supply to power the AM335x MPU domain. This is supplied by the TPS65217C DCDC2.

7.3.3 VDD_CORE

The OSD335x C-SiP contains a dedicated 1.1 VDC supply to power the AM335x CORE domain. This is supplied by the TPS65217C DCDC3.

7.3.4 VDDS_PLL

The OSD335x C-SiP contains a filtered 1.8 VDC supply to power the AM335x PLLs and oscillators. This is supplied by the TPS65217C LDO3.

7.4 Total Current Consideration

The total current consumption of all power rails must not exceed the recommended input currents described in Table 8-2. This includes power consumption within the SiP from the AM335x and the DDR3, as well as all external loads on the output power rails from Section 7.2.

The power consumed by the AM335x can be estimated using the *AM335x Power Estimation Tool* found in the Reference Documents section of this document. When estimating power consumption, the efficiencies and types of the OSD335x C-SiP internal power supplies must be considered. Refer to the "*Connections Diagram for TPS65217C and AM335x*" section of *Powering the AM335x with the TPS65217x* found in the Reference Documents section of this document for more information on the power supplies providing power to the AM335x.

7.5 Minimum Connections

In order to use the OSD335x C-SiP, a minimum set of connections must be made between pins of the OSD335x C-SiP for proper operation. These include pins for: eMMC power, IO voltage domains, Processor – PMIC interface, RTC.

7.5.1 Minimum eMMC power connections

The eMMC power inputs EMMC_VCC and EMMC_VCCQ should be connected to SYS_VDD1_3P3V.

7.5.2 Minimum IO voltage domain connections

The IO pins of AM335x are divided into 6 pin groups. The IO voltage levels of a pin group can be configured by connecting the voltage domain pins to the required voltage level. Table 7-1 lists recommended connections for each VDDSHV pin according to the voltage level required. These connections are required for IO pins of OSD335x C-SiP to function properly.

Table 7-1 - VDDSHVx connections for OSD335x C-SiP

Voltage Domain	Pin	Voltage Level	Recommended pin connection
VDDSHV1	M11	3.3V	L11
		Must be 3.3V to support eMMC.	
VDDSHV2	M10	3.3V	L10
		1.8V	N10
VDDSHV3	M9	3.3V	L9
		1.8V	N9
VDDSHV4	M7	3.3V	L7
		1.8V	N7
VDDSHV5	M8	3.3V	L8
		1.8V	N8
VDDSHV6	M12	3.3V	L12
		1.8V	N12

7.5.3 Minimum Processor-PMIC interface Connections

Table 7-2 lists the signals required to coordinate the operation of the AM335x and TPS65217C. Figure 7-1 and Figure 7-2 illustrate the required connections between the AM335x and the TPS65217C with the RTC subsystem disabled and the RTC subsystem enabled without the RTC-only power mode, respectively. These connections are the minimum required to operate the device in corresponding mode. The accessibility of these signals enables other uses of reset, power control, power status, interrupt, wakeup, and serial communication signals.

Figure 7-1 and Figure 7-2 illustrate the interface between the AM335x and TPS65217C.

Table 7-2 - AM335x and TPS65217C Signal Descriptions

Signal	Description	Notes
PMIC_POWER_EN	PMIC Power Enable from AM335x	
PMIC_PWR_EN	PMIC Power Enable to TPS65217C	1
I2C0_SCL	I2C0 SCL from AM335x	1
PMIC_SCL	I2C SCL to TPS65217C	
I2C0_SDA	I2C0 SDA from AM335x	1
PMIC_SDA	I2C SDA to TPS65217C	
PMIC_PGOOD	PGOOD from TPS65217C	
PWRONRSTN	PWRONRSTN to AM335x	
PMIC_LDO_PGOOD	LDO_PGOOD from TPS65217C	
RTC_PWRONRSTN	RTC_PWRONRSTN to AM335x	
PMIC_NINT	NINT from TPS65217C	
EXTINTN	EXTINTN to AM335x	1
PMIC_NWAKEUP	NWAKEUP from TPS65217C	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2-2 for pull up on this signal

When the RTC is disabled, the following signal connections should be used:

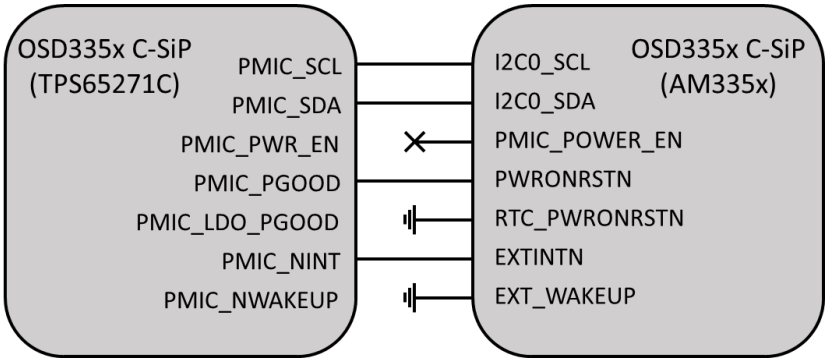


Figure 7-1 - OSD335x C-SiP Minimum Signal Connections with RTC disabled

When the RTC is enabled and the RTC-only power mode does not need to be supported, the following signal connections should be used:

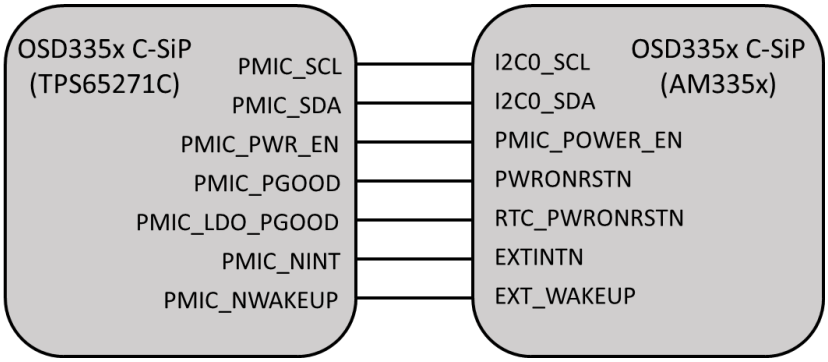


Figure 7-2 - OSD335x C-SiP Minimum Signal Connections with RTC enabled

7.5.4 Minimum RTC Power Connections

Table 7-3 lists RTC power domain signals required to operate the OSD335x C-SiP. In addition to the required connections described in Section 7.5.3, Figure 7-3, Figure 7-4, and Figure 7-5 illustrate power connections with RTC subsystem enabled and disabled. These connections are also included in the minimum required circuitry to operate the device.

Table 7-3. OSD335x C-SiP RTC Signal Descriptions

Signal	Description	Notes
CAP_VDD_RTC	Supply voltage for the RTC core domain	
RTC_KALDO_ENN	Active low enable input for internal CAP_VDD_RTC voltage regulator	
RTC_PWRONRSTN	RTC_PWRONRSTN to AM335x	2
PMIC_POWER_EN	PMIC Power Enable from AM335x	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1
VDDS_RTC	Supply for RTC power domain	
VDDS	Supply for 1.8V IO voltage domain	2

1. See Table 2-2 for pull up on this signal
2. RTC_PWRONRSTN must be pulled up by the same power source as VDDS_RTC when being powered externally.

When the RTC is disabled, the following connections should be used for the internal LDO:

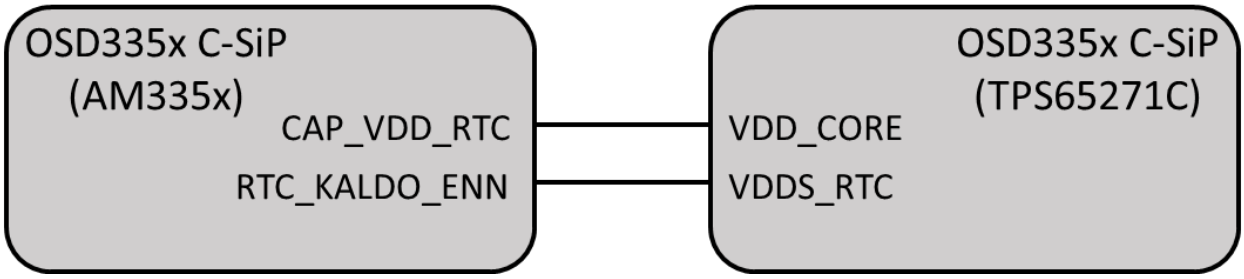


Figure 7-3 - Additional connections for OSD335x C-SiP with RTC disabled

When the RTC is enabled, the following connections should be used for the internal LDO:

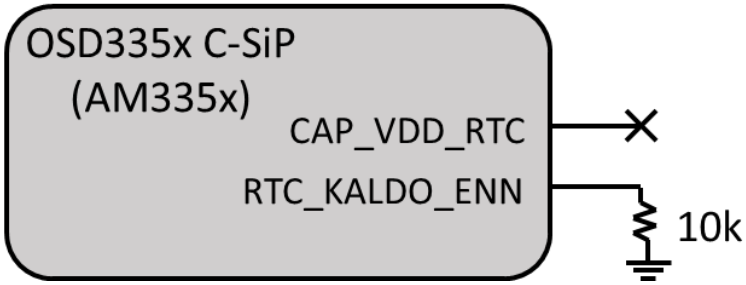


Figure 7-4 - Additional connections for OSD335x C-SiP with RTC enabled

When the RTC is disabled or the RTC is enabled and the RTC-only power mode does not need to be supported, the following connections should be used:

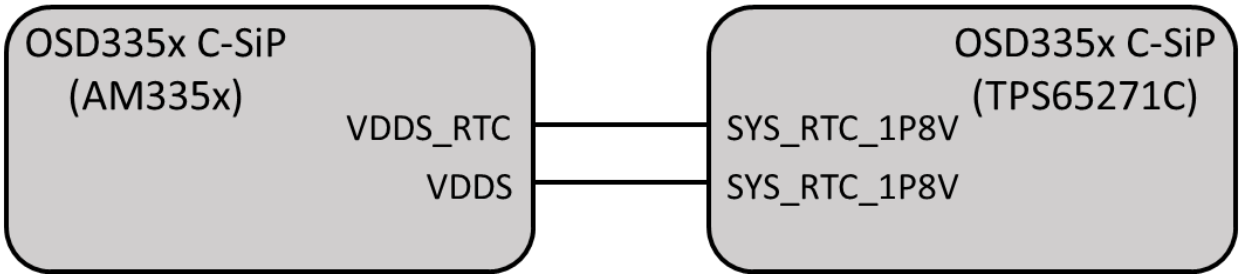


Figure 7-5 - VDDS_RTC and VDDS Power Connections for RTC-only Power Mode Disabled

8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of OSD335x C-SiP.

Table 8-1. OSD335x C-SiP Absolute Maximum Ratings over operating free-air temperature range (unless noted) [(1) (2)]

		Value	Unit
Supply voltage range (with respect to VSS)	VIN_BAT	-0.3 to 7	V
	VIN_USB, VIN_AC	-0.3 to 7	
Input/Output voltage range (with respect to VSS)	All pins unless specified separately	-0.3 to 3.6	V
Terminal current	SYS_VOUT, VIN_USB, VIN_BAT	3000	mA
T_C Operating case temperature	Commercial (B)	0 to 85	°C
	Industrial (I)	-40 to 85	°C
T_{stg} Storage temperature		-55 to 125	°C
ESD rating	(HBM) Human body model	±2000	V
	(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

Table 8-2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
Supply voltage, VIN_USB, VIN_AC	4.3		5.8	V
In-rush current, VIN_AC			2.1	A
In-rush current, VIN_USB			500	mA
Supply voltage Rise Time, VIN_USB, VIN_AC (100mV to 4.5V)			50	ms
Supply voltage, VIN_BAT	3.5		5.5	V
Input current from VIN_AC			2.0	A
Input current from VIN_USB			1.3	A
VIN_BAT current			2.0	A
Output voltage range for SYS_VDD1_3P3V		3.25		V
Output voltage range for SYS_VDD2_3P3V		3.3		V
Output voltage range for SYS_VDD3_3P3V		3.3		V
Output voltage range for SYS_RTC_1P8V		1.8		V
Output voltage range for SYS_VDD_1P8V		1.8		V
Output voltage range for SYS_ADC_1P8V		1.8		V
Output voltage range for VDDS_DDR[1]		1.5		V
Output voltage range for VDD_MPU[1]		1.1		V
Output voltage range for VDD_CORE[1]		1.1		V
Output voltage range for VDDS_PLL[1]		1.8		V
Output current for SYS_VOUT[2]	0		500	mA
Output current for SYS_VDD1_3P3V[2,3]	0		300	mA
Output current for SYS_VDD2_3P3V[2]	0		100	mA
Output current for SYS_VDD3_3P3V[2]	0		50	mA
Output current for SYS_RTC_1P8V[2]	0		100	mA
Output current for SYS_VDD_1P8V[2]	0		250	mA
Output current for SYS_ADC_1P8V[2]	0		25	mA

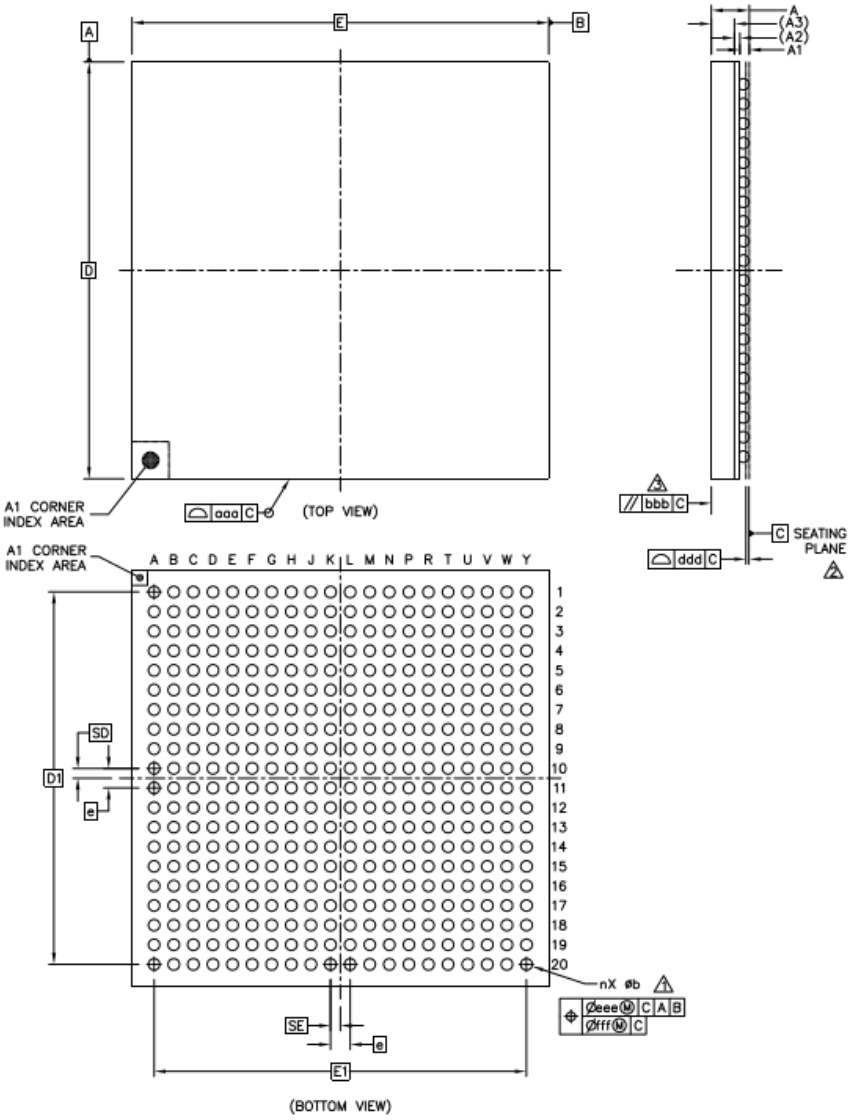
(1) *These voltage rails are for reference only and should not be used to power anything on the PCB.*
(2) *Please note that the total input current on VIN_AC, VIN_USB or VIN_BAT must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.4 for more details.*
(3) *Maximum current assumes that eMMC (EMMC_VCC and EMMC_VCCQ) are connected to SYS_VDD1_3P3V.*

9 Packaging Information

The OSD335x C-SiP is packaged in a 400 ball, Ball Grid Array (BGA). The package size is 27 X 27 millimeters with a ball pitch of 1.27 millimeters. This section will give you the specifics on the package.

9.1 Mechanical Dimensions

The mechanical drawings of the OSD335x C-SiP show pin A1 in the lower left-hand corner when looking at the top view of the device. Pin A1 is in the upper left-hand corner if looking at the balls from the bottom view of the package. The PCB layout should have pin A1 in the lower left-hand corner when looking at the top side of the PCB where the OSD335x C-SiP will be attached.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.6
STAND OFF	A1	0.5	---	0.7
SUBSTRATE THICKNESS	A2		0.35	REF
MOLD THICKNESS	A3		1.5	REF
BODY SIZE	D		27	BSC
	E		27	BSC
BALL DIAMETER			0.75	
BALL OPENING			0.6	
BALL WIDTH	b	0.6	---	0.9
BALL PITCH	e		1.27	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		24.13	BSC
	E1		24.13	BSC
BODY CENTER TO CONTACT BALL	SD		0.635	BSC
	SE		0.635	BSC
PACKAGE EDGE TOLERANCE	aaa		0.2	
MOLD FLATNESS	bbb		0.35	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.3	
BALL OFFSET (BALL)	fff		0.15	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

9.1.1 Landing Pad Sizing

For the nominal ball diameter of 0.75mm, specification IPC-7351A states that for NSMD pads, the nominal land diameter is 0.55mm with a land variation of 0.60mm to 0.50mm. Footprints provided by Octavo Systems generally use the minimum land pad size to enable lower cost routing (see Layout Guide in the Reference Documents section for more information). However, some applications may require a larger land pad size to enable a more robust structural

connection to the circuit board or for other manufacturing constraints. Check the requirements of the application and manufacturer to determine the appropriate land pad size.

9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

9.3 Storage Requirements

The OSD335x Family of devices are sensitive to moisture and need to be handled in specific ways to make sure they function properly during and after the manufacturing process. The OSD335x Family of devices are rated with a Moisture Sensitivity Level (MSL) of 4. This means that they are typically stored in a sealed Dry Pack.

Once the sealed Dry Pack is opened the OSD335x needs to be used within 72 hours to avoid further processing. If the OSD335x has been exposed for more than 72 hours, then it is required that you bake the device for 34 hours at 125°C before using.

Alternatively, the devices could be stored in a dry cabinet with humidity <10% to avoid the baking requirement.

For more information, please refer to the Texas Instruments AN-2029 which can be found in the Reference Documents section of this document.