

N-Ch MOSFET

General Description

The WSC5N20A is the highest performance trench N-ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSC5N20A meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Product Summery

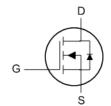
BVDSS	RDSON	ID			
200V	0.6Ω	5A			

Applications

Telecom 48V input Forward Converters

TO-251/ I-Pak Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	200	V
V _{GS} Gate-Source Voltage		±20	V
I _D Continuous Drain Current		5	Α
I _{DM} Pulsed Drain Current		20	Α
P _D Total Power Dissipation		43	W
TJ,T _{STG} Operating Junction and storage Temperature Range		-55 to 175	$^{\circ}$

Thermal Data

Symbol	Parameter		Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹		50	°C/W
$R_{ heta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤10s)		35	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹		3.5	°C/W

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Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	200			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25℃ , I _D =1mA		0.23		V/℃
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =30A		0.52	0.6	Ω
$V_{GS(th)}$	Gate Threshold Voltage		1.2	1.7	2.5	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient			-6.16		mV/℃
lead	Drain-Source Leakage Current	V_{DS} =200V , V_{GS} =0V , T_J =25 $^{\circ}$ C			25	uA
I _{DSS}	Dialif-Source Leakage Current	V_{DS} =160V , V_{GS} =0V , T_{J} =55 $^{\circ}$ C			200	uA
I _{GSS}	Gate-Source Leakage Current	V_{GS} = $\pm 30 V$, V_{DS} = $0 V$			±100	nA

Dynamic @ TJ = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
gfs	Forward Transconductance	V _{DS} =50V , I _D =2.9A	2.6			S
Q_g	Total Gate Charge (4.5V)	V _{DS} =160V ,		15		
Q_gs	Gate-Source Charge	V _{GS} =10V ,		2.4		nC
Q_{gd}	Gate-Drain Charge	I _D =2.9A		6.1		
T _{d(on)}	Turn-On Delay Time	V _{DD} =100V		6.4		
Tr	Rise Time	V _{GS} =10V		11		20
T _{d(off)}	Turn-Off Delay Time	$R_G=24\Omega$		20		ns
T _f	Fall Time	I _D =2.9A		12		
C _{iss}	Input Capacitance	V _{DS} =25V		300		
Coss	Output Capacitance	V _{GS} =0V		53		pF
C _{rss}	Reverse Transfer Capacitance	f=1MHz		15		

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current	V _G =V _D =0V , Force Current			5	Α
V_{SD}	Diode Forward Voltage	V_{GS} =0V , I_{S} =2.9A , T_{J} =25 $^{\circ}$ C			1.2	V

Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
E _{AS}	Single Pulse Avalanche Energy	VGS=10V,L=0.1mH,IAS=2.9A			46	mJ
E _{AR}	Repetitive Avalanche Energy	VGS=10V,L=0.1mH,IAS=2.9A			4.3	mJ

Note

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper,t<10sec.
- 2.The data tested by pulsed , pulse width $\,\leq\,300\text{us}$, duty cycle $\,\leq\,2\%$
- 3. The EAS data shows Max. rating . The test condition is V_{DD} =100V, V_{GS} =10V,L=0.1mH, I_{AS} =2.9A
- 5. The Min. value is 100% EAS tested guarantee.
- 6. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics

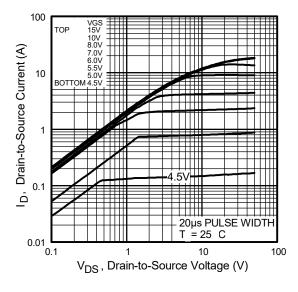


Fig 1. Typical Output Characteristics

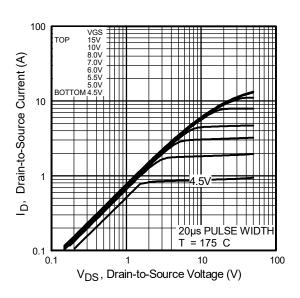


Fig 2. Typical Output Characteristics

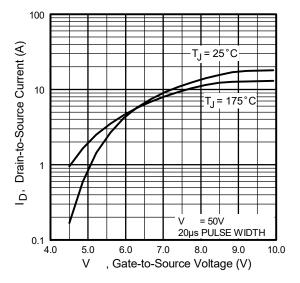


Fig 3. Typical Transfer Characteristics

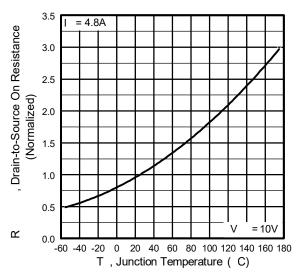


Fig 4. Normalized On-Resistance Vs. Temperature



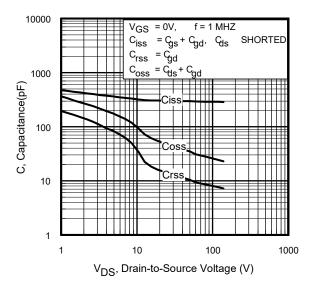


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

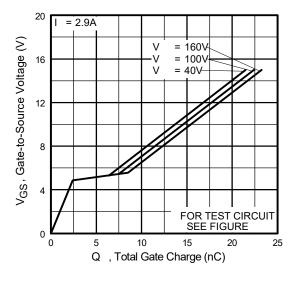


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

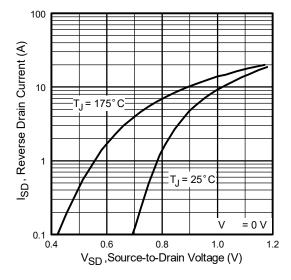


Fig 7. Typical Source-Drain Diode Forward Voltage

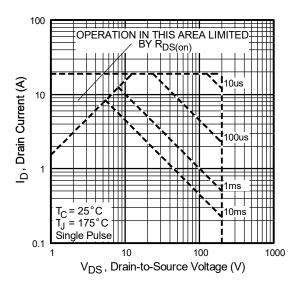


Fig 8. Maximum Safe Operating Area



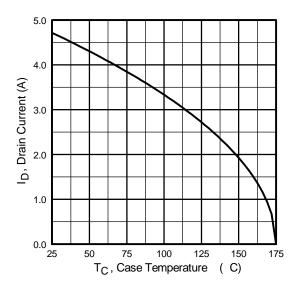


Fig 9. Maximum Drain Current Vs. Case Temperature

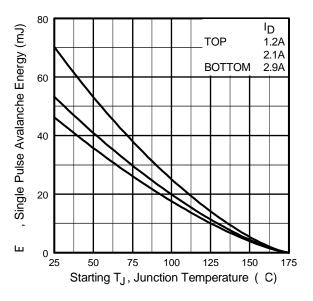


Fig 10. Maximum Avalanche Energy Vs. Drain Current

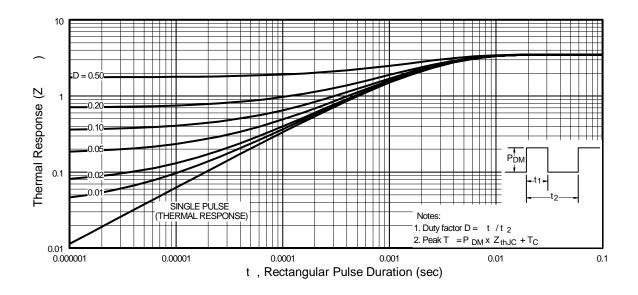


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



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