# SY6818

## High Current Overvoltage Protection Switch With Integrated Reverse Blocking FET

## General Description

The SY6818 is an over voltage protection switch with high current capability to prevent damage to the downstream system with low voltage rating. It achieves wide input voltage range from 2.5$V_{DC}$ to 30$V_{DC}$. Programmable OVP is available with simple external resistor divider. Integrated reverse blocking FET up to 20V rating prevents the leakage current from output side to input side when the input power supply is removed, but without output discharging. Extremely low power path resistance $R_{PWPT}$ helps to reduce power loss during the normal operation. Enable control is available to cut off the energy path. High accuracy current indicator is employed internally. It integrates the over-temperature protection shutdown and auto-recovery with hysteresis to protect against over temperature events. It has a default 5A, max 8A over current protection and auto-recovery once over load condition is removed. Each auto-recovery process is composed of deglitch time $T_{DG}$ and switch turn-on time $T_{ON}$. This IC along with CSP-12, 1.73mm×1.73mm footprint provides small PCB area application.

## Features

- $V_{IN}$=2.5V to 30V
- Integrated Reverse Blocking FET up to 20V Rating for High Voltage Charging Mode
- Extremely Low Power Path Resistance $R_{PWPT}$
  - $R_{PWPT}$=53mΩ typ.
- Programmable OVP thru External Resistor Divider, Accuracy up to ±3%
- Internal Soft-start to Prevent In-rush Current
- Thermal Shutdown Protection & Auto-recovery
- Current Indicator with High Accuracy up to ±5%
- RoHS Compliant and Halogen Free
- Compact Package: CSP-12 (1.73mm×1.73mm)

## Applications

- Smart Phone
- Tablet PCs
- Mobile Device

## Ordering Information

SY6818 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

| Ordering Number | Package Type | Note |
|---|---|---|
| SY6818PLC | CSP1.73×1.73-12 | |

## Typical Applications

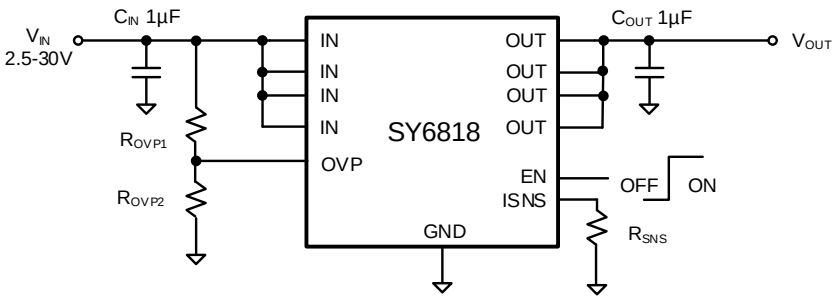
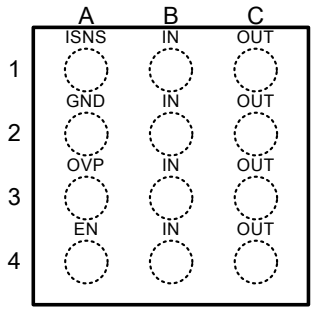



Figure 1. Schematic Diagram

## Pinout (top view)

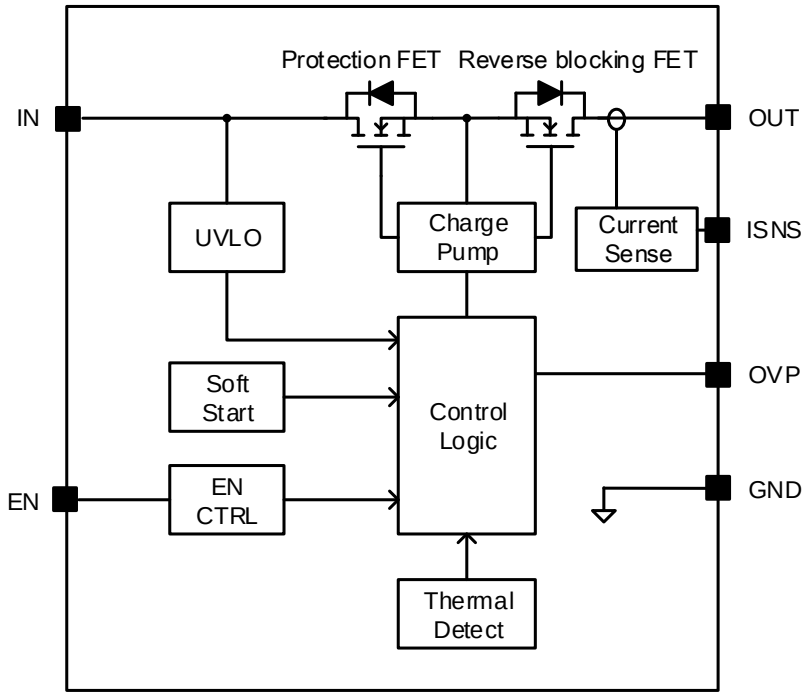



| Part Number | Package type | Top Mark① |
|---|---|---|
| SY6818PLC | CSP1.73×1.73-12 | **ZQ*xyz*** |

*Note①：* ***x=year code, y=week code, z= lot number code.***

| Pin Name | Pin Number | Pin Description |
|---|---|---|
| IN | B1,B2,B3,B4 | Power input pin. Connect IN pin together. Decouple high frequency noise by connecting at least a 0.1μF MLCC to ground. |
| OUT | C1,C2,C3,C4 | Output voltage pin. Connect the OUT pins together for normal operation. |
| ISNS | A1 | Current indicator pin. Connect a resister $R_{SNS}$ from this pin to ground. The current flow is mirrored internally to charge $R_{SNS}$ for the indication. The ratio of power current to mirrored current is 2.5k. The voltage on the ISNS pin equals to $V_{ISNS}=(I_{OUT}/2.5k)\times R_{SNS}$. |
| EN | A4 | EN control pin. High logic enables all the internal circuit; low logic disables the internal energy flow path. |
| OVP | A3 | External OVP program pin. Connect resistor divider to this pin to program the OVP threshold. The internal reference is at 1.26V. Pull down this pin to ground to disable external program function. |
| GND | A2 | Power ground pin. |

## Block Diagram




## Absolute Maximum Ratings (Note 1)

IN, EN, OVP ---------- 30V
OUT ---------- 20V
ISNS ---------- 6V
Continues IN, OUT Current ---------- 3A
Peak IN, OUT Current (10ms) ---------- 5A
Power Dissipation, $P_D$ @ $T_A$ = 25°C CSP, ---------- 1.67 W
Package Thermal Resistance (Note 2)
$\theta_{JA}$ ----------60 °C/W
$\theta_{JC}$ ---------- 7 °C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

## Recommended Operating Conditions (Note 3)

IN, EN, OVP ---------- less than 30V
OUT ---------- less than 20V
ISNS ---------- less than 6V
Continues IN, OUT Current ---------- less than 3A
Peak IN, OUT Current (10ms) ---------- less than 5A
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

# Electrical Characteristics

($V_{IN}$ = 2.5V to 30V, $R_{ISNS}$=1k, $C_{IN}$=1μF, $C_{OUT}$=1μF, TA = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 2.5 | | 30 | V |
| Input UVLO Threshold | $V_{UVLO}$ | | | | 2.4 | V |
| UVLO Hysteresis | $V_{HYS}$ | | | 0.1 | | V |
| Reverse Blocking Range | $V_{RB}$ | | | | 20 | V |
| Bias Current | $I_{BIAS}$ | $V_{IN}$=5V | | 100 | | μA |
| Reverse Blocking Current | $I_{RB}$ | $V_{IN}$=0V, $V_{OUT}$=16V, EN=0V | | 2 | 5 | μA |
| Shutdown Current | $I_{SD}$ | $V_{IN}$=5V, EN=0V | | 6 | 10 | μA |
| | | $V_{IN}$=30V, EN=0V | | 9 | 15 | μA |
| Enable Threshold | $V_{EN}$ | Rising | 1.2 | | | V |
| | | Falling | | | 0.5 | V |
| OVP Program Threshold | $V_{OVP}$ | | 1.22 | 1.26 | 1.30 | V |
| Resistance of Power Path | $R_{PWPT}$ | $V_{IN}$=5V, $I_{OUT}$=200mA, from IN to OUT | 30 | 53 | 70 | mΩ |
| Current Indicator Accuracy | $V_{ISNS}$ | $I_{OUT}$=0.5A, $R_{SNS}$=1k | 186 | 200 | 214 | mV |
| | | $I_{OUT}$=1.0A, $R_{SNS}$=1k | 380 | 400 | 420 | mV |
| Maximum Current Capability (Note 4) | $I_{MAX}$ | | | 5 | | A |
| Output Load Capacitance | $C_{OUT}$ | $V_{IN}$=5V | | | 1000 | μF |
| Deglitch Time | $t_{DG}$ | Time from 2.5V<$V_{IN}$<$V_{OVP}$ to $V_{OUT}$=10% of $V_{IN}$ | 6 | 11 | 16 | ms |
| Switch Turn-on Time | $t_{ON}$ | $V_{IN}$=5V, $V_{OUT}$=10% of $V_{IN}$ to 90% $V_{IN}$ | 0.7 | 1.2 | 1.7 | ms |
| Thermal Shutdown Temperature | $T_{SD}$ | | | 150 | | °C |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 20 | | °C |

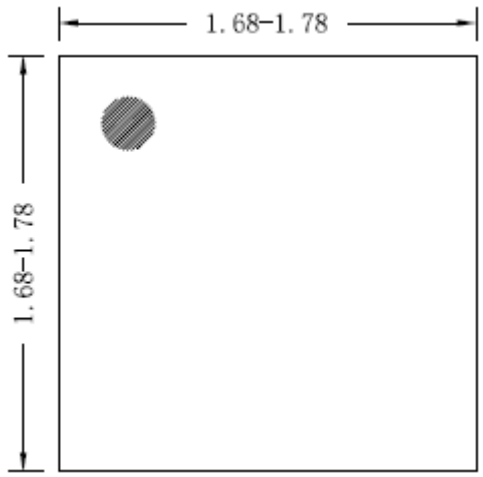
**Note 1**: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

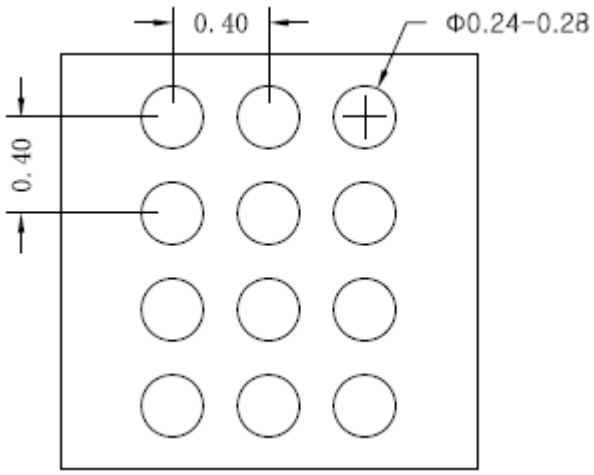
**Note 3**: The device is not guaranteed to function outside its operating conditions.

**Note 4**: These characteristics are design guaranteed, not test items.

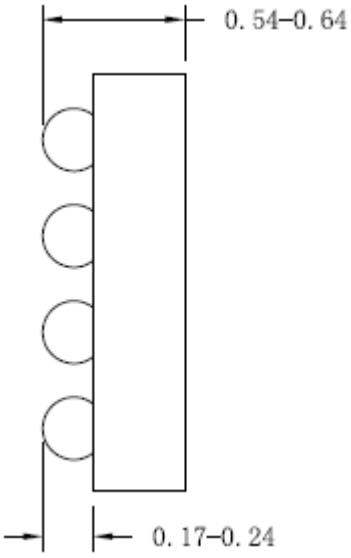
# CSP1.73×1.73-12 Outline Drawing



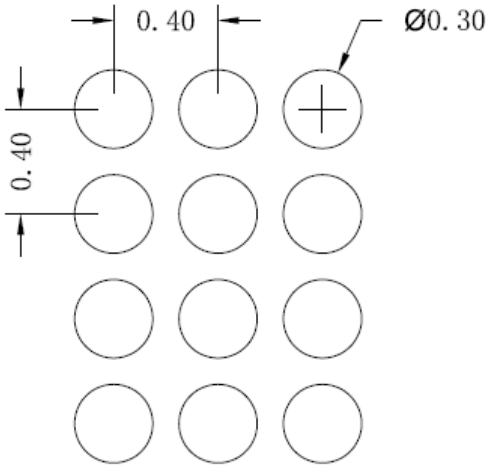

Top View




Bottom View




Side View

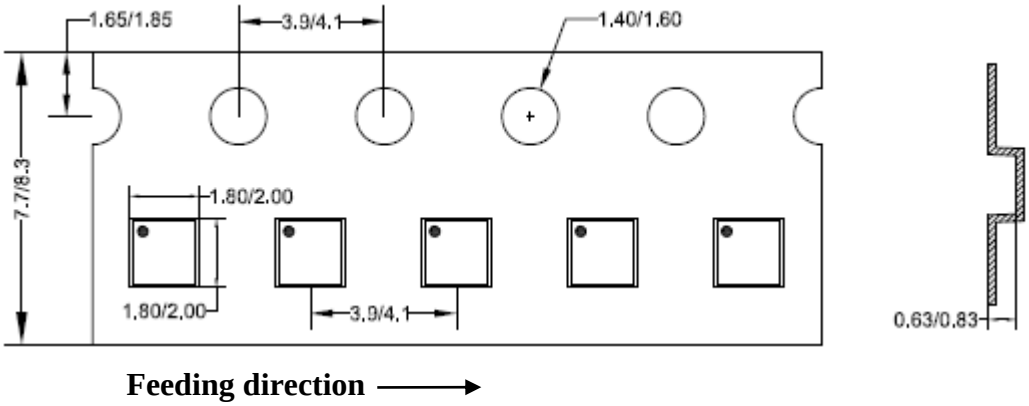



Recommended PCB layout

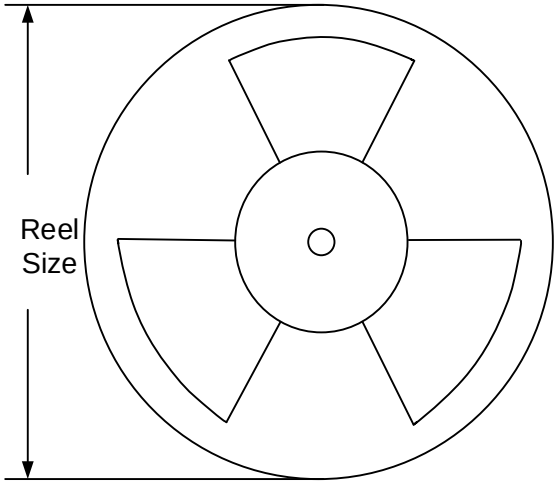
**Notes: All dimension in millimeter and exclude mold flash & metal burr**

# Taping & Reel Specification

## 1. CSP1.73×1.73 taping orientation




## 2. Carrier Tape & Reel specification for packages




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| CSP1.73×1.73 | 8 | 4 | 7" | 400 | 400 | 3000 |

## 3. Others: NA