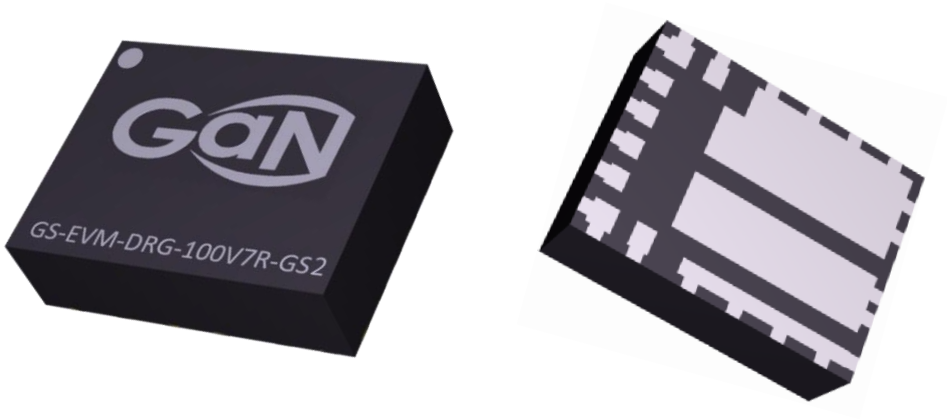
GS-EVM-DRG-100V7R-GS2

100 V Driver GaN Fully Integrated 7mΩ DC/DC Power Stage

Technical Manual



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WARNING:
PCB surface can become hot. Contact may cause burns. Do not touch!

CAUTION!
This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

Please refer to the Evaluation Board/Kit Important Notice on page 13

Overview

GS-EVM-DRG-100V7R-GS2 is fully-integrated 100V GaN Half-Bridge power stage for use in multiple high-efficiency small form-factor 48V Applications. Module construction embeds all components without using bond wires, minimizing inductance, achieving ultra-low voltage spikes on gate and switch nodes, and minimizing RFI. This DrGaN thermal design achieves ultra-low Junction-to-Case thermal resistance which reduces junction operating temperature. GS-EVM-DRG-100V7R-GS2 "Drop-In" GaN power stages create designs with high efficiency and power density for 48V DC-DC applications. GS-EVM-DRG-100V7R-GS2 is intended and made available for testing and evaluation purposes only.

Features

- Integrated 7mΩ half-bridge power stage
- 10 x 7.8 mm² SMT surface mount technology package
- Includes two GS61008 Die (100V 7mW E-mode GaN) onboard
- Dual PWM input
- Ultra-low R_{QJC}
- Ultra-fast rise/fall time
- High power density at 1MHz+ f_{SW} operation
- High efficiency for 48V board power
- Small footprint

Applications

- 48 V Step Down Converters
- CPU/GPU/DDR
- High-performance Class D Audio systems
- Forward Converter, ZVS, Buck/Boost topologies

Contents and Requirements

The GS-EVM-DRG-100V7R-GS2 includes the following hardware.

Table 1 GS-EVM-DRG-100V7R-GS2 Evaluation Kit Contents

Quantity	Description
1	GS-EVM-DRG-100V7R-GS2 100V Driver GaN – Integrated 7mΩ DC/DC half-bridge power stage

Figure 1 DrGaN Power Stage

Please refer to the Evaluation Board/Kit Important Notice on page 13

Technical Specifications

Absolute Maximum Ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional Operation should be restricted to the conditions specified in the Normal Operating section of this technical manual.

Table 2 Absolute Macximum Ratings (T_{CASE} = 25 °C)

Parameter	Sym.	Value	Unit
Max Input Voltage (GaN Devices, V_{IN} to V_{SW}, V_{SW} to PGND)	V_{DS_MAX}	100	V
Max Input Voltage (Drive circuit, V_{IN} to V_{SW})	V_{IN_MAX}	6.2 to 85	V
Max Output Voltage (Drive circuit, V_{SW} to PGND)	V_{OUT_MAX}	0.9 to 85	V
Continuous I_{DS} Current (T_{JUNC} = 25 °C)	$I_{DS\_MAX\_25C}$	90	A
Continuous I_{DS} Current (T_{JUNC} = 100 °C)	$I_{DS\_MAX\_100C}$	65	A
Max Driver-side Voltages to GND (V_{CC}, DLH, DHL, PWM)	V_{CC_MAX} V_{IO_MAX}	–0.3 to +7.0	V
Maximum Junction Temperature (GaN)	T_{JUNC_MAX}	150	°C
Maximum Operating Temperature (Module)	T_{CASE}	–40 to +125	°C
Maximum Storage Temperature Range (Module)	T_{STOR}	–55 to +150	°C

Thermal Characteristics

GS-EVM-DRG-100V7R-GS2 is Surface Mount Device (SMD) with Bottom-side Cu Pads for Surface Mount PCB attach. $R_{\Theta\_JUNC\text{-}AMB}$ value based on recommended Via Pattern with multi-layer FR4 PCB. No Airflow (zero LFM) and no Top-side Heat Sink required to meet $R_{\Theta\_JUNC\text{-}AMB}$ (Conduction Heat Transfer). GS-EVM-DRG-100V7R-GS2 has a much more effective competitive thermal design.

Table 3 Thermal Characterictics

Parameter	Sym.	Min.	Typ.	Max.	Unit
Thermal Resistance (Junction to Board)	$R_{\Theta\_JUNC\text{-}BRD}$	-	0.6	-	°C/W
Thermal Resistance (Junction to Ambient)	$R_{\Theta\_JUNC\text{-}AMB}$	-	8.4	-	°C/W
Maximum Soldering Temperature (MSL2 rated)	T_{SOLDER}	-	-	260	°C

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Normal Operation Conditions

GS-EVM-DRG-100V7R-GS2 is surface mount device with bottom-side Cu pads for surface mount PCB attach. $R_{\Theta\_JC\text{-}AMB}$ value based on recommended via pattern with multi-layer FR4 PCB. No airflow (zero LFM) and no top-side heat sink required to meet $R_{\Theta JC\text{-}AMB}$ (conduction heat transfer).

Table 4 Normal Operation Conditions (T_{JUNC} = 25 °C, and V_{CC} = V_{GS} = 6.0V)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Nominal V_{IN} Range	V_{IN_NOM}	6.2	-	100	V	
Nominal V_{SW} Range	V_{OUT_NOM}	0.9	-	80	V	
Nominal V_{CC} Range	V_{CC_NOM}	5.0	-	6.0	V	
Nominal I/O Voltage	V_{IO_NOM}	0	-	5.5	V	DLH, DHL, PWM
Continuous I_{OUT} (T_{JUNC} = 100 °C)	I_{DS_NOM}	-	-	16.6	A	V_{OUT} = 12V, T_{JUNC} = 100^0C
Operating Temp (Module)	T_{CASE}	–40	-	+105	°C	

Block Diagram

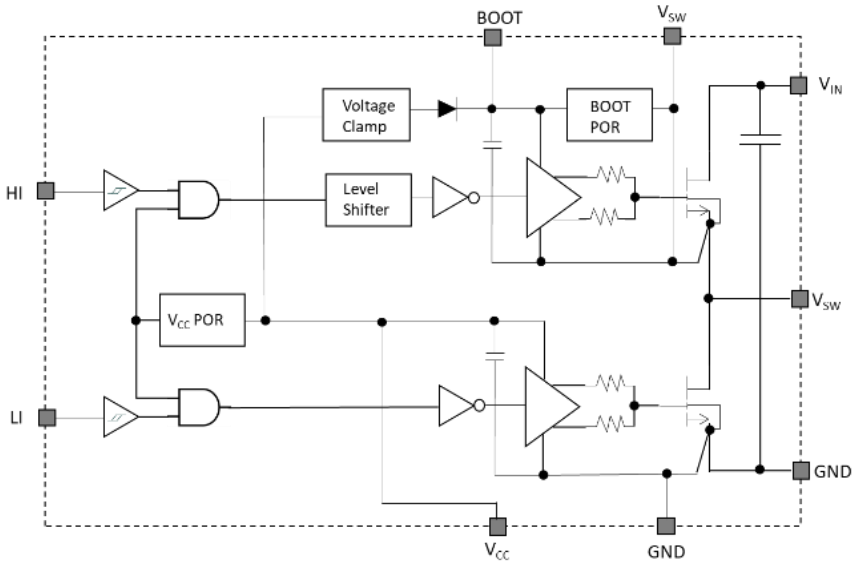

Figure 2 DrGaN Power Module Block Diagram

Pin

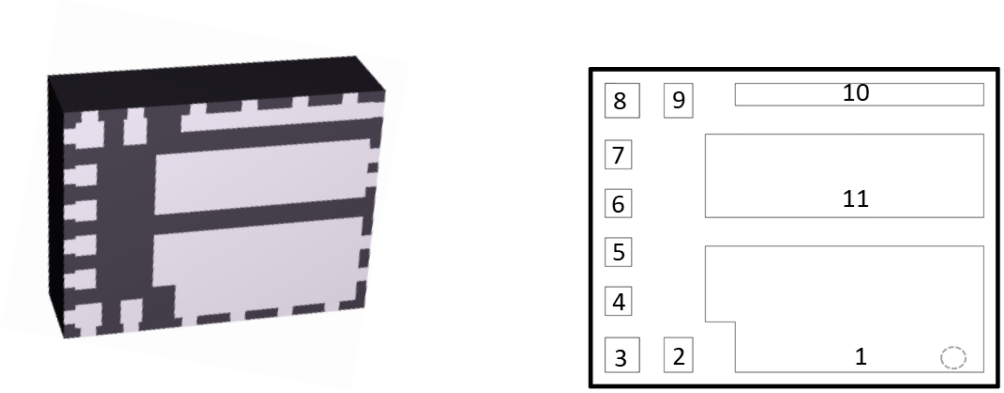

Figure 3 DrGaN Power Module Bottom View

Table 5 Pinout Table

Pinout		I/O Type	Description and Operation
#	Name GS2		
1 , 2	GND	Power GND	Connect to PCB GND thru multiple Via's
3	V_{CC}	Supply	Gate Drive power supply, connect to Regulated 5.5V or 6.0V
4	LI	Input	Dual PWM Low Side Gate Input
5	HI	Input	Dual PWM High Side Gate Input
6	N/C	Input	No Connect
7	N/C	-	No Connect
8	BOOT	Supply	Floating High Side Gate Drive power supply
9 , 11	V_{SW}	Power Output	Half-Bridge power stage output (switching node)
10	V_{IN}	Power Input	Supply Voltage to Half-Bridge power stage

Application Specifications

Integrated GaN Gate Drive

- GaN E-mode Gate Drive Voltage (V_{GS}) is nominally 0V to +6.0V for optimal RDS_{ON} performance and Lifetime Reliability. Absolute Maximum V_{GS} Rating is +7.0V (DC voltage), but GaN E-modes are Rated for transients up to +10V and –20V for pulses up to 1µs. In order to simplify system-level power design, these specifications for GaN E-mode V_{GS} are incorporated into the DrGaN design. Connect V_{CC} Pin to +6V (optimal), or +5V (optional), to provide for GaN Gate Drive.
- While +6.0V Gate Drive voltage puts the Enhancement Mode High Electron Mobility Transistors full Enhancement (i.e., optimal efficiency), +5.0V Gate Drive supply can also be used, resulting in slightly lower DrGaN Efficiency.
- Gate and Commutation loop inductances are minimized in the DrGaN design, and DC Link is decoupled, providing for fastest Gate dV/dt (lowest Switching Loss) and optimized Switching Waveforms at high-FSW , full-Load operation.

- Driver Latch-Up Immunity (ΔV_{LATCH}) supports ultra-fast Gate dV/dt in an ultra-low inductance module.
- Rise Time, Fall Time, Prop Delay, and Prop Delay Matching are designed for sub-20 ns Dead Time.
- Integrated Gate Resistors for High Side and Low Side Gates for Turn-On and Turn-Off, and a Zener
- Diode in the Bootstrap, are optimized for highest Efficiency (fastest dV/dt with reliable Switching Waveforms).

GaN reverse conduction

- GaN E-modes do not have a parasitic Body Diode or a parasitic Bi-Polar in their Substrate, therefore the GaN E-mode has Zero QRR and extremely high dV/dt Ruggedness. But despite not having a Body Diode, the GaN E-mode will inherently conduct in Reverse Current flow (Source-to-Drain) through the 2DEG Channel, when Source-to-Drain potential (V_{SD}) is greater than V_{TH} (approximately 1.3V)
- During reverse conduction, V_{GS} can be zero Volts (no Gate Bias is required for Reverse Conduction operation), and anti-parallel Diodes are not required for reverse conduction.
- For optimal efficiency Dead Time should be minimized, with Synchronous Rectification operation.

GaN blocking voltage

- GaN E-HEMT Blocking Voltage (BV_{DS}) is defined by the value of Drain Leakage Current (I_{DSS}). Hard Breakdown (unrecoverable) will occur above the Rated BV_{DS} value, similar to Si MOSFET or IGBT. As a general practice, the applied Drain voltage should be de-rated in a similar manner as Si MOSFET or IGBT.
- All GaN power transistors do not Avalanche and thus do not have an Avalanche Breakdown Rating.
- The maximum Drain-to-Source Rating does not change if negative Gate voltage is applied.

Please refer to the Evaluation Board/Kit Important Notice on page 13

Full-Bridge or 3-phase operation

- GS-EVM-DRG-100VR7-GS2 can easily be interleaved for Full-Bridge or 3-phase operation by using a Controller IC with multiple PWM outputs and separate Control Loops.

Boost mode operation

- For Boost Mode operation, Start-Up Timing is critical due to the fact that when Low Side Gate is "H" level as VCC clears POR, a short circuit path can be created: Input voltage → Inductor → LS GaN → GND. Start-Up Sequence for VCC must assert LAST during Power On Reset (POR), and de-assert FIRST during Power Off.
- GS-EVM-DRG-100VR7-GS2 can easily be interleaved for Full-Bridge or 3-phase operation by using a Controller IC with multiple PWM outputs and separate Control Loops.

Dead time design and operation

- Typical Delay Matching Time is 1.5ns which limits minimum Dead Time to 1.5ns, however, at least a 10ns Dead Time is recommended for switching reliability. Because the Dual PWM DrGaN version has HI and LI PWM inputs, switching control is feasible especially in ZVS Mode and in Pulse Skip or power save mode during light load operation.
- In ZVS operation, controlling Dead Time low-to-high ($T_{DT,LH}$) can be achieved using output inductor and the C_{OSS} of the GaN Switch to generate a resonant period, using HI and LI to adjust $T_{DT,LH}$.

Thermal design

- DrGaN µModule designed using ***PowerCore™*** technology has ultra-low Thermal Resistance Junction-to-Case. GS-EVM-DRG-100V7R-GS2 has $R_{\Theta\_JUNC\text{-}CASE}$ value < 0.6 ^{0}C/W, many times lower than other DrGaN solutions.
- The GaN E-mode devices in GS-EVM-DRG-100V7R-GS2 are Rated to T_{JUNC} = 150 ^{0}, however, the DrGaN µModule and integrated Gate Driver circuit have a Normal Operating temperature range of –40 ^{0}C to +105 0^{0}C.

PCB layout

- GS-EVM-DRG-100V7R-GS2 is designed to accommodate the high dV/dt of GaN switches, and commutation and gate loop inductances are ultra-low. Additionally, $R_{\Theta\_JUNC\text{-}CASE}$ is ultra-low, allowing tight Layout and small Footprint. PCB Layout example is shown below. ***Utilize multiple Via's to connect PCB Power and GND Planes to the DrGaN Pads.***

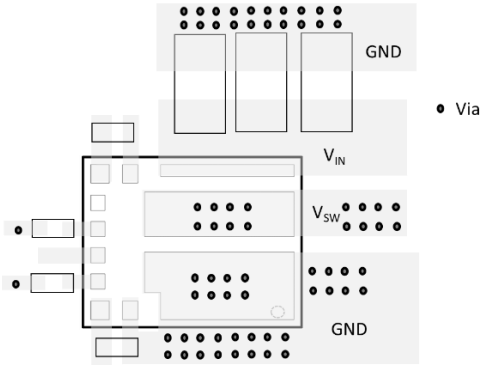

Figure 4 PCB Layout Example

Typical Switching Waveforms

(48V V_{IN}, Duty Cycle = 25%, I_{OUT} = 10A, 1GHz B.W. measurement)

Figure 5 Switching Node (10V per Division)

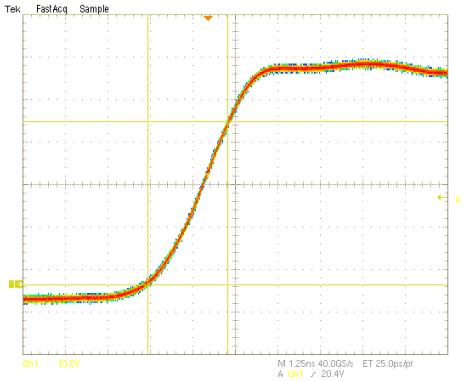

Figure 6 Rise Time (10V per Division)

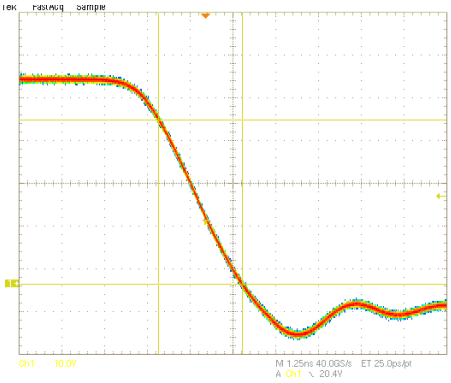

Figure 7 Fall Time (10V per Division)

SMT manufacturing

IPC/JEDED J-STD Reflow Profile is recommended for Surface Mount (SMT) manufacturing

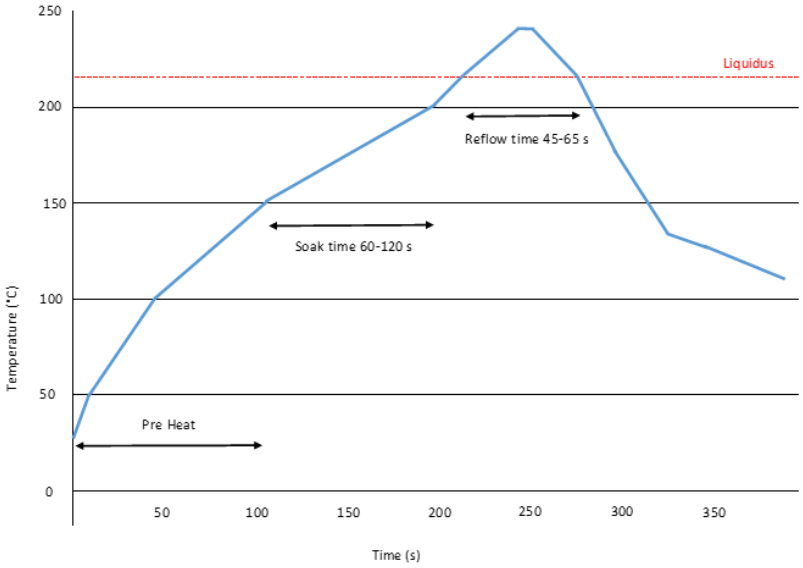

Figure 8 SMT Manufacturing

Electrical Specifications

All Parameters listed apply to each GaN Device in the DrGaN Half-Bridge power stage.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{IN} to V_{SW}, and V_{SW} to PGND Blocking Voltage	BV_{DS}	100	-	-	V	I_{DSS} = 50 µA, V_{GS} = 0 V
Drain to Source ON Resistance	$R_{DS(ON)}$	-	7	9.5	mΩ	T_{JUNC} = 25 °C, I_{DS} = 36 A
Drain to Source ON Resistance	$R_{DS(ON)}$	-	16.8	-	mΩ	T_{JUNC} = 150 °C, I_{DS} = 36 A
Drain to Source Leakage Current	I_{DSS}	-	0.5	50	µA	V_{DS} = 100 V, V_{GS} = 0 V, T_{JUNC} = 25 ^{0}C
Drain to Source Leakage Current	I_{DSS}	-	100	-	µA	V_{DS} = 100 V, V_{GS} = 0 V, T_{JUNC} = 150 ^{0}C
Switching Characteristics (each GaN Device in the Half-Bridge power stage)**:**						
Input Capacitance	C_{ISS}	-	588	-	pF	V_{DS} = 50 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}	-	254	-	pF	
Reverse Transfer Capacitance	C_{RSS}	-	9.9	-	pF	
Total Gate Charge	Q_{G_TOT}	-	12	-	nC	V_{DS} = 50V V_{GS} = 0 V to 6.0 V I_{DS} = 80 A
Gate to Source Charge	Q_{GS}	-	4.5	-	nC	
Gate to Drain Charge	Q_{GD}	-	1.5	-	nC	
Output Charge	Q_{OSS}	-	21.3	-	nC	V_{DS} = 50 V, V_{GS} = 0 V
Reverse Recovery Charge	Q_{RR}	-	Zero	-	nC	
Turn-On Prop Delay	$t_{PD(ON)}$	-	15	-	ns	V_{IN} = 48 V and V_{OUT} = 5 V I_{DS} = 20 A, V_{GS} = 0 V to 6.0 V $R_{GATE\_ON\_HS/LS}$ = 2.2 Ω $R_{GATE\_OFF\_HS/LS}$ = 0 Ω C_{LOAD} = C_{ISS} = 588 pF
Rise Time (Driver)	t_{RISE}	-	4	-	ns	
Turn-Off Prop Delay	$t_{PD(OFF)}$	-	15	20	ns	
Fall Time (Driver)	t_{FALL}	-	4	-	ns	
Prop Delay Matching (Dual PWM)	$t_{PD(HB)}$	-	1.5	-	ns	
Driver Block Characteristics:						
UVLO High Threshold	$UVLO_{HI}$	3.8	4.0	4.2	V	VCC to GND, Rising Edge
UVLO Hysteresis	$UVLO_{HYS}$	-	350	-	mV	VCC to GND
PWM High Threshold (Single PWM)	PWM_{HI}	2.0	2.2	2.4	V	PWM to GND, Rising Edge

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PWM Low Threshold (Single PWM)	PWM_{LO}	0.8	1.0	1.2	V	PWM to GND, Falling Edge
PWM Tri-State (Single PWM)	PWM_{TRI}	1.2	1.6	2.0	V	PWM to GND, Tri-State
Tri-State S/D Hold-Off (Single PWM)	TRI_{OFF}	-	25	40	ns	Time to Shut-Down during T/S
PWM Input Current (Single PWM)	I_{PWM}	-	–120	–240	µA	PWM = 0V
		-	120	240		PWM = 3.3V
		-	120	240		PWM = 5V
PWM High Threshold (Dual PWM)	PWM_{HI}	2.3	-	-	V	PWM to GND, Rising Edge
PWM Low Threshold (Dual PWM)	PWM_{LO}	-	-	0.5	V	PWM to GND, Falling Edge
PWM Pull-Down (Dual PWM)	R_{PWM}	-	200	-	kΩ	
PWM Hysteresis (Dual PWM)	PWM_{HYS}	-	400	-	mV	PWM to GND
Driver Latch-Up Immunity	ΔV_{LATCH}	-	-	100	V/ns	V_{IN} = 48 V and V_{OUT} = 5 V I_{DS} = 20 A, V_{GS} = 0 V to 6.0 V C_{LOAD} = 588 pF, F_{SW} = 1 MHz
Driver-side Quiescent Current	$I_{CC(Q)}$	-	550	1000	µA	RP007U1, PWM = 0V
		-	120	-	µA	RP007U2, PWM = 0V

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Mechanical Drawings

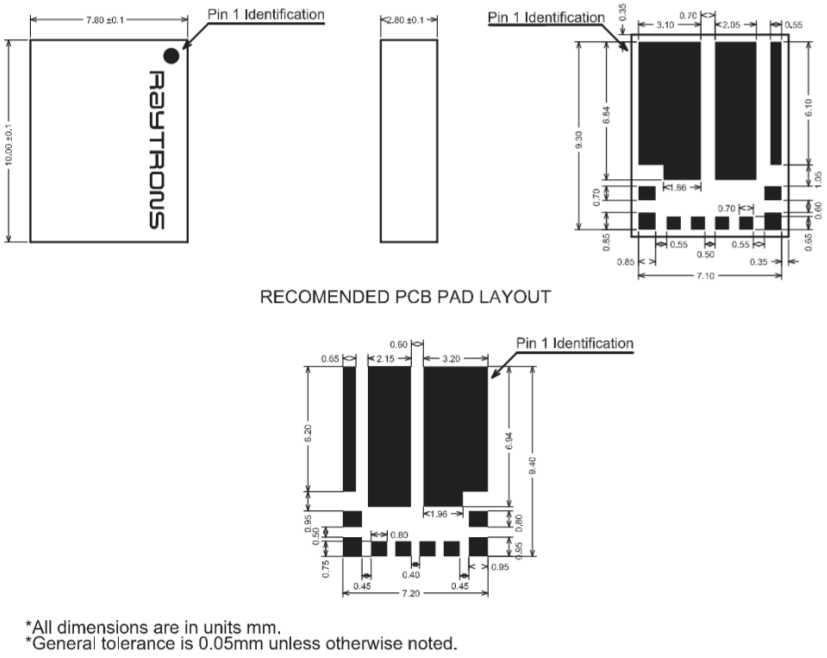

Figure 9 Mechanical Drawing

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