March 1997

FAIRCHILD
SEMICONDUCTOR™

ML2031, ML2032

Tone Detector

GENERAL DESCRIPTION

The ML2031 and ML2032 are monolithic tone detectors intended for telecommunication applications utilizing 4-wire loopback capability. The device meets or exceeds the 4-wire Maintenance Terminating Unit (MTU) requirements outlined in BELL PUB 43004.

These devices incorporate a 2713 Hz tone detector, clock oscillator, and uncommitted op amp in an 8-pin DIP. No external components are required.

The ML2031 or ML2032 can be used to detect frequencies of 1004 Hz or 2600 Hz, as the tone detector frequency template from 1000 Hz to 4000 Hz is proportional to the frequency of the external clock.

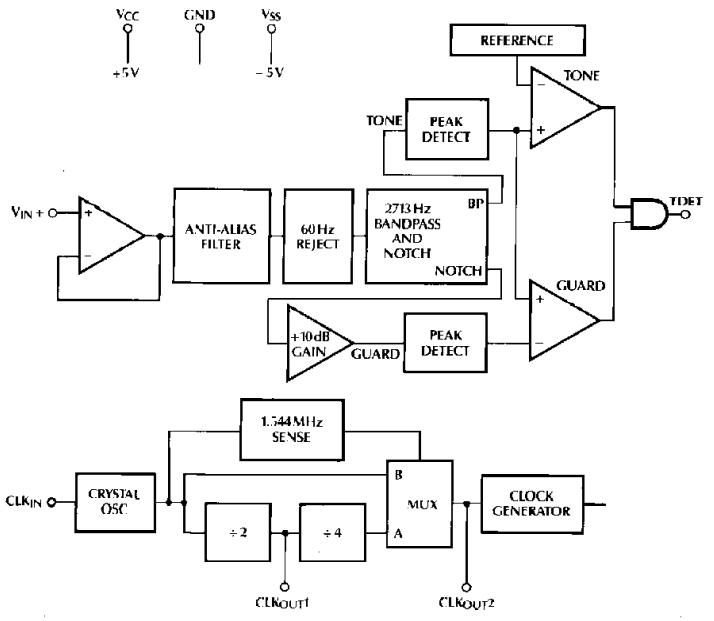
The ML2031 has two clock outputs. $CLK_{OUT}1$ is one half the frequency of CLK_{IN}, while $CLK_{OUT}2$ is one eighth of the frequency of CLK_{IN}. The ML2032 has an uncommitted op amp instead of the clock outputs.

FEATURES

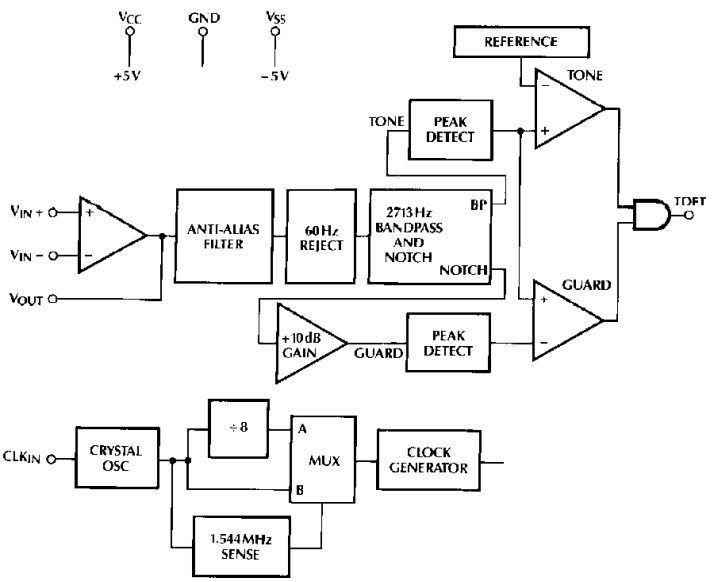
- Meets or exceeds BELL PUB 43004 requirements
- Extended dynamic range detect −34 dBm to +6 dBm
  no detect ⩽ −40 dBm
- Frequency template ($f_{CLK\ IN}$ = 12MHz)
  detect 2713 ± 10Hz
  no detect 2713 ± 36Hz
- General purpose tone detect range of 1000Hz to 4000Hz
- Signal-to-guard ratio 8 dB to 13 dB
- No external components required
- Continuous anti-alias filter
- 60 Hz reject filter
- ±5 V supplies
- Clock input 12.352 MHz, 1.544 MHz, or a 12.352 MHz crystal
- ML2031 has clock outputs of 1.544 MHz and 6.176 MHz
- Tone detection of 1000 Hz to 4000 Hz proportional to external clock
- ML2032 has uncommitted op amp

BLOCK DIAGRAMS

ML2031

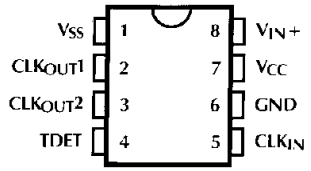


ML2032



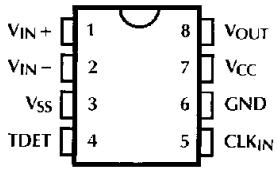
PIN CONNECTIONS

ML2031



TOP VIEW

ML2032



TOP VIEW

PIN DESCRIPTIONS

ML2031

PIN NO.	NAME	FUNCTION
1	V_{SS}	Negative supply. −5V ± 10%
2	$CLK_{OUT}1$	Clock output. Digital output from oscillator divided by 2.
3	$CLK_{OUT}2$	Clock output. Digital output from oscillator divided by 8.
4	TDET	Tone detect output. Digital output which indicates when valid 2713 Hz tone is present on analog input.
5	CLK_{IN}	Clock input. Internal clock can be generated by tying a 12.352 MHz crystal between this pin and GND, or by applying a 12.352 MHz or 1.544 MHz clock to this pin.
6	GND	Ground. Analog and digital inputs and outputs are referenced to this point.
7	V_{CC}	Positive supply. +5V ± 10%
8	$V_{IN}+$	Analog input.

ML2032

PIN NO.	NAME	FUNCTION
1	$V_{IN}+$	Positive Analog input. Positive input to the uncommitted op amp.
2	$V_{IN}-$	Negative Analog input. Negative input to the uncommitted op amp.
3	V_{SS}	Negative supply. −5V ± 10%
4	TDET	Tone detect output. Digital output which indicates when valid 2713 Hz tone is present on analog input.
5	CLK_{IN}	Clock input. Internal clock can be generated by tying a 12.352 MHz crystal between this pin and GND, or by applying a 12.352 MHz or 1.544 MHz clock to this pin.
6	GND	Ground. Analog and digital inputs and outputs are referenced to this point.
7	V_{CC}	Positive supply. +5V ± 10%
8	V_{OUT}	Analog output. Output of the uncommitted op amp.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... +6.5V
- V_{SS} ..... –6.5V

AGND with respect to GND ..... ±.5V
Analog Input and Output ..... V_{SS} –0.3V to V_{CC} +0.3V
Digital Input and Outputs ..... GND –0.3V to V_{CC} +0.3V
Input Current Per Pin ..... ±25mA
Power Dissipation 750mW
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

OPERATING CONDITIONS

Temperature Range (Note 2)
- ML2031CP, ML2032CP ..... 0°C to 70°C
- ML2031IP, ML2032IP ..... –40°C to 85°C

Supply Voltage
- V_{CC} ..... 4V to 6V
- V_{SS} ..... –4V to –6V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $CLK_{IN} = 12.352MHz \pm 1200Hz$, or $CLK_{IN} = 1.544MHz \pm 150Hz$, $C_L = 100pF$, dBm measurements use 600Ω as reference load, uncommitted op amp in unity gain configuration.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
TONE DETECT							
f_{TD}	Tone Detection Frequency	4	V_{IN} = +6dBm to –34dBm	2703		2723	Hz
f_{TR}	Tone Rejection Frequency	4		2679		2747	Hz
A_{TD}	Tone Detection Amplitude	4	V_{IN} = 2703 Hz to 2723 Hz	–34		+6	dBm
A_{TR}	Tone Rejection Amplitude	4		–40			dBm
SGM	Signal to Guard Margin	4	800 Hz 1400 Hz 2000 Hz 2450 Hz Signal = –13 dBm, 2713 Hz. See BELL PUB 43004 sec. 2.4 for test method	8 8 8 8		13 13 13 13	dB dB dB dB
SFI	SF Tone Immunity	5	V_{IN} + = 2600 Hz No tone detect			+6	dBm
t_{TD}	Tone Detect Delay	4	V_{IN}+ = –8dBm, 2713 Hz Figure 1	0	10	30	ms
t_{TR}	Tone Removal Delay	4	V_{IN}+ = –8dBm, 2713 Hz Figure 1	0	4	30	ms
OP AMP							
V_{INR}	Input Voltage Range	5		±3			V
V_{OSW}	Output Voltage Swing	4	ML2032 Only	±3			V
V_{OS}	Input Offset Voltage	4	ML2032 Only			±20	mV
Z_{IN}	Input Impedance	4		1			MΩ
A_{VOL}	DC Open Loop Gain	4		1k	5k		V/V
f_{UG}	Unity Gain Frequency	5		0.5	1		MHz
I_{CN}	Noise- Input Referred	5	C msg weighted 1kHz		–9	–3 375	dBrnc $nv/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = 5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $CLK_{IN} = 12.352MHz \pm 1200Hz$, or $CLK_{IN} = 1.544MHz \pm 150Hz$, $C_L = 100pF$, dBm measurements use 600Ω as reference load, uncommitted op amp in unity gain configuration.

SYMBOL	PARAMETER	NOTES	CONDITIONS	MIN	TYP NOTE 3	MAX	UNITS
DIGITAL AND DC							
V_{IL}	Input Low Voltage, CLK_{IN}	4				1.5	V
V_{IH}	Input High Voltage, CLK_{IN}	4		3.5			V
I_{IN}	Input Current, CLK_{IN}	4	CLK_{IN} = 1.5V to 3.5V		10	60	μA
			CLK_{IN} = 0 to 1.5V; 3.5V to V_{CC}		150	500	μA
C_{IN}	Input Capacitance, CLK_{IN}	5			11		pF
V_{OL}	Output Low Voltage	4	I_{OL} = -2mA			0.4	V
V_{OH}	Output High Voltage	4	I_{OH} = 2mA	4.0			V
I_{CC}	V_{CC} Supply Current	4	No output load			7.5	mA
I_{SS}	V_{SS} Supply Current	4	No output load			-4.5	mA
CLOCK OUTPUT							
$f_{CLK}1$	$CLK_{OUT}1$ Output Frequency	4	Figure 2	½		½	$f_{CLK}1$
$f_{CLK}2$	$CLK_{OUT}2$ Output Frequency	4	Figure 2	⅛		⅛	$f_{CLK}1$
t_{1R}	$CLK_{OUT}1$ Output Rise Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{1F}	$CLK_{OUT}1$ Output Fall Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{2R}	$CLK_{OUT}2$ Output Rise Time	4	Figure 2, C_L = 50pF	0		20	ns
t_{2F}	$CLK_{OUT}2$ Output Fall Time	4	Figure 2, C_L = 50pF	0		20	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

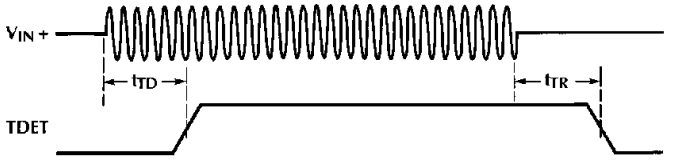
Note 2: 0°C to +70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 3: Typicals are parametric norm at 25°C.

Note 4: Parameter guaranteed and 100% production tested.

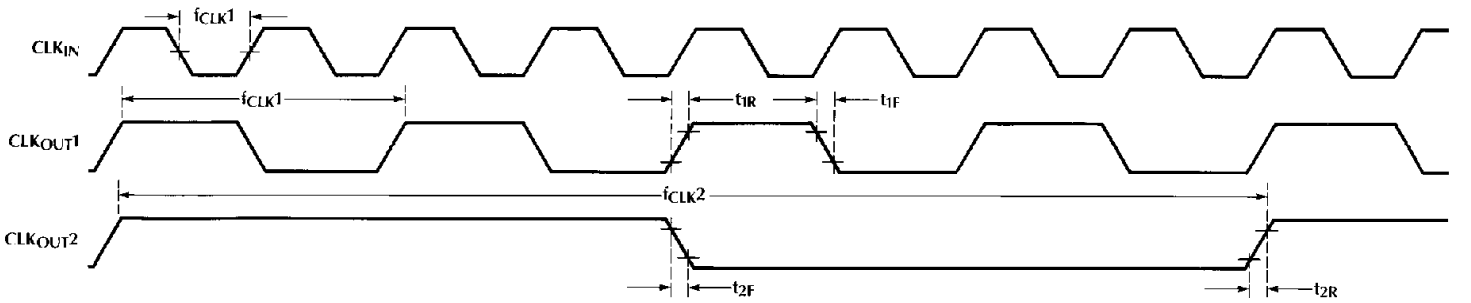
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

TIMING DIAGRAMS



t_{TD} MEASURED FROM V_{IN} + ZERO CROSSING TO 1.4V MIDPOINT ON TDET
t_{TR} MEASURED FROM 1.4V MIDPOINT ON TDET TO ZERO CROSSING ON V_{IN} +

Figure 1. Tone Detect Timing



t_{1F}, t_{1R}, t_{2F}, t_{2R} MEASURED BETWEEN 0.8 and 2.0 VOLT TRANSITION POINTS
ALL OTHER PARAMETERS REFERRED TO 1.4V MIDPOINT

Figure 2. Digital Clock Output Timing

TYPICAL PERFORMANCE CURVE

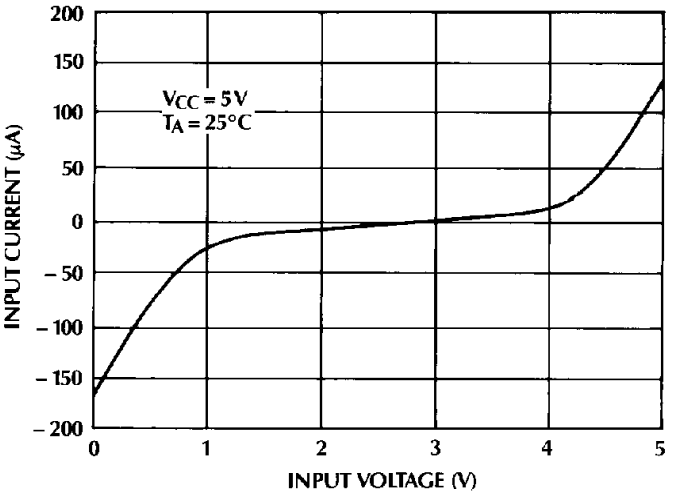


Figure 3. CLK_{IN} Input Current vs. Input Voltage

1.0 FUNCTIONAL DESCRIPTION

The ML2031 has a divide by 2 and divide by 8 clock output to drive external devices. The ML2032 has an uncommitted op amp. Refer to the block diagram.

1.1 Uncommitted Op Amp

The ML2032 features an uncommitted op amp. The ML2031 has the op amp connected in the unity gain configuration (V_{IN} – internally tied to V_{OUT}).

The uncommitted op amp is a general purpose amplifier that can be used to interface the device with the analog telephone line. It has a high impedance input, a 0.5 MHz unity gain bandwidth, will drive a 1k, 100 pF load, and the input and output can swing within 1.5 V of the supplies.

1.2 Anti-Alias Filter

The anti-alias filter is a continuous second order low pass designed to prevent high frequency signals at the input from being aliased into the passband by the sampling action of the switched capacitor filters. The typical 3 dB corner frequency is 25 kHz and the typical rejection at 124 kHz is –30 dB.

1.3 60 Hz Reject Filter

The 60 Hz reject filter is a switched capacitor second order high pass designed to reject 60 Hz line interference on the analog input. The typical 3 dB corner frequency is 300 Hz and the typical rejection at 60 Hz is –24 dB.

1.4 Tone Detector

The tone detector is a monolithic block designed to indicate when a valid 2713 Hz tone is present on the analog input. A tone is valid if the following criteria are met:

1. 2713 Hz tone satisfies amplitude vs. frequency tone detector template shown in *Figure 4*.
2. The non-2713 Hz out of band energy present on the input is sufficiently small enough compared to the 2713 Hz tone (signal to guard margin).

The tone detector consists of 2713 Hz bandpass and notch filters, tone and guard peak detectors, tone and guard comparators, reference, and digital output buffer.

The analog signal first goes through the 2713 Hz bandpass and notch switched capacitor filters. The bandpass filter outputs any 2713 Hz signal (tone), and the notch filter outputs any non-2713 Hz signals (guard) in the range of 300–4500 Hz, respectively.

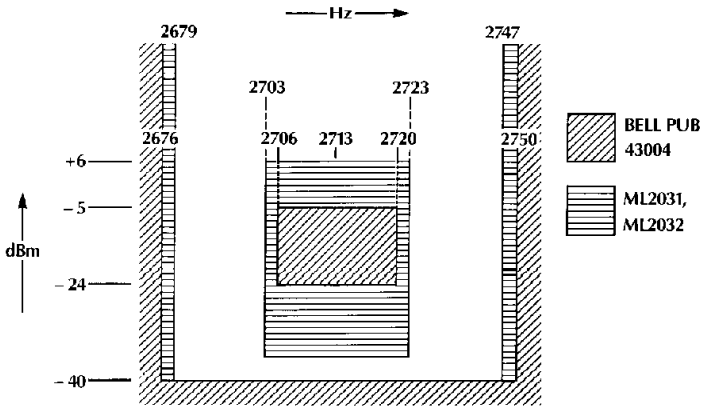


Figure 4. Tone Detector Template

The tone and guard signals then go to peak detectors which output a DC voltage proportional to the 2713 Hz and non-2713 Hz energy present on the analog input.

The tone comparator compares the tone energy to a fixed reference value to determine if it meets the amplitude requirements for tone detection shown in *Figure 4*.

The guard comparator compares the tone energy to the guard energy to determine if the signal to guard margin is met.

If both comparators indicate that a 2713 Hz tone and no out of band energy exists, the TDET output goes high indicating valid tone detection. If the signal comparator indicates insufficient signal energy or the guard comparator indicates too much out of band energy, then the TDET output stays low indicating invalid tone output.

1.5 Crystal Oscillator/Clock Generator

The crystal oscillator/clock generator generates the necessary internal clocks from either an external clock or an external crystal.

If an external clock input is used to drive CLK_{IN}, the input frequency can either be 12.352 MHz or 1.544 MHz in order to meet the frequency template. The device has an internal frequency sense circuit that can sense the difference between 12.352 MHz and 1.544 MHz and makes the necessary changes in the clock generator to accomodate either frequency at the input.

If a crystal is used, a 12.352 MHz crystal must be connected between CLK_{IN} and GND. This unique 1-pin crystal oscillator does not generally require any external capacitors or other external components to meet the frequency template. The crystal should be physically placed as close as possible to the CLK_{IN} pin to minimize stray inductances and capacitances.

The crystal must have the following characteristics:

1. Parallel resonant type
2. Frequency: 12.352000 MHz
3. Tolerance: ±0.005% @ 25°C
4. Less than 0.005% variation over desired temperature range
5. Maximum equivalent series resistance of 15 Ω at a drive level of 1 µW to 200 µW
6. Maximum equivalent series resistance of 30 Ω at drive levels of 10 nW to 1 µW
7. Typical load capacitance: 18 pF
8. Maximum case capacitance: 5 pF

The frequency of oscillation will be a function of the crystal parameters and board capacitance. If the final oscillation frequency is different than the ideal 12.352 MHz, the template frequencies will change according to the formulas outlined in section 1.6. If the crystal meets the above recommended parameters and typical PC board capacitance from CLK_{IN} to GND is 2 pF, then the device will meet the template specifications. Crystals that meet these requirements are M-tron 3709-010 12.352 for 0°C to +70°C and 3709-020 12.352 for –40°C to +85°C operation.

1.0 FUNCTIONAL DESCRIPTION (Continued)

The ML2031 has two clock outputs that can be used to drive other external devices. The $CLK_{OUT}1$ output is a buffered output from the oscillator divided by 2. The $CLK_{OUT}2$ output is a buffered output from the oscillator divided by 8. If a 12.352MHz clock or crystal is used, $CLK_{OUT}1 = 6.176$MHz and $CLK_{OUT}2 = 1.544$MHz.

1.6 Detecting Tones from 1000 Hz to 4000 Hz

The tone detector frequency template shown in *Figure 5* is proportional to the frequency of CLK_{IN}. Thus, the device can be set to a center frequency (other than 2713Hz) by adjusting CLK_{IN} frequency.

The external clock frequency, $fCLK_{IN}$, needed to produce a given center frequency, can be calculated by:

$$fCLK_{IN} = f_C \times 4552.893$$

once $fCLK_{IN}$ has been determined, the other template frequency points shown in *Figure 5* can be calculated by:

$$f_{DL} = fCLK_{IN} \times 2.18831 \times 10^{-4}$$

$$f_{DU} = fCLK_{IN} \times 2.20450 \times 10^{-4}$$

$$f_{RL} = fCLK_{IN} \times 2.16888 \times 10^{-4}$$

$$f_{RU} = fCLK_{IN} \times 2.22393 \times 10^{-4}$$

The above formulas are valid for center frequencies with the range of 1000Hz to 4000Hz. The internal divide by 8 circuitry may be bypassed by applying a clock that is one eighth of the above calculated values.

When the required CLK_{IN} frequency calculated above is less than 6MHz, the internal frequency sense circuit may become enabled causing the detection of an erroneous center frequency. In this case, the divide by 8 function cannot be used and only the lower clock frequency may be used. For example, for a 1004Hz tone detector, the clock frequency applied must be 571kHz.

1.7 Power Supplies

The analog circuits in the device run from +5 to −5 (V_{CC} to V_{SS}) and are referenced to GND.

The digital circuits in the device run from +5 to 0 (V_{CC} to GND).

It is recommended that the power supplies to the device be bypassed by placing decoupling capacitors from V_{CC} to GND and V_{SS} to GND as physically close to the device as possible.

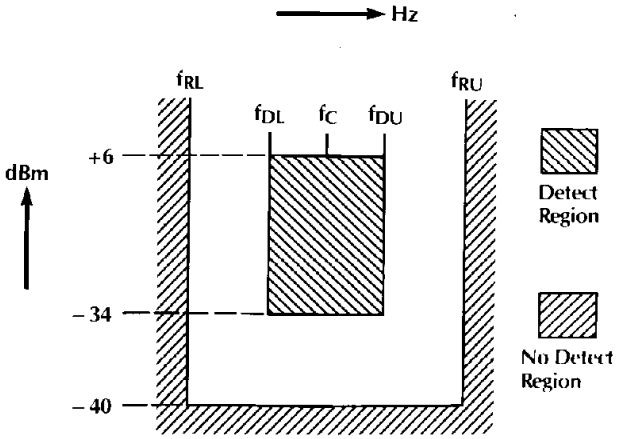


Figure 5. Tone Detector Template

2.0 APPLICATIONS

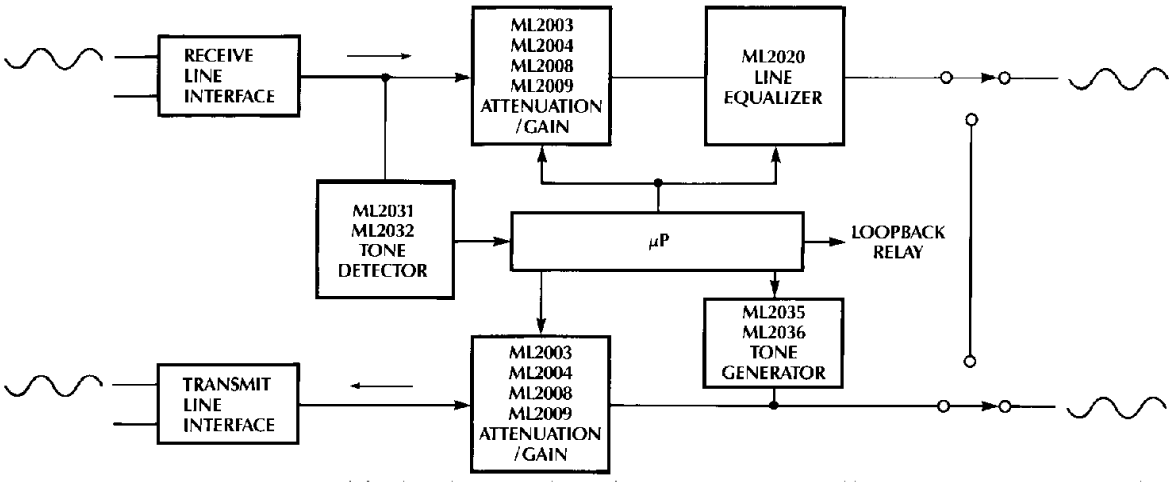


Figure 6. 4-Wire Termination Equipment

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML2031CP	0°C to +70°C	MOLDED DIP (P08)
ML2031IP	-40°C to +85°C	MOLDED DIP (P08)
ML2032CP	0°C to +70°C	MOLDED DIP (P08)
ML2032IP	-40°C to +85°C	MOLDED DIP (P08)