

General Description

The WSP4410 is the highest performance trench N-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSP4410 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

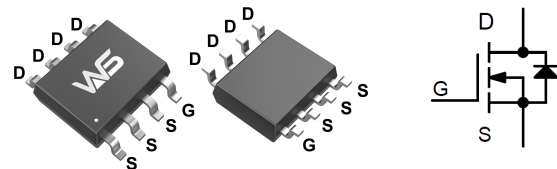
Product Summary

BVDSS	RDSON	ID
30V	4mΩ	20A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOP-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	20	A
$I_D@T_c=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	15.8	A
I_{DM}	Pulsed Drain Current ²	80	A
EAS	Single Pulse Avalanche Energy ³	31	mJ
I_{AS}	Avalanche Current	25	A
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	4.2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	65	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	25	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.028	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	---	4.0	5.5	mΩ
		V _{GS} =4.5V, I _D =14A	---	6.0	6.8	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.3	1.8	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-6.16	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =12A	---	18	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.4	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =20A	---	12.9	---	nC
Q _{gs}	Gate-Source Charge		---	4.22	---	
Q _{gd}	Gate-Drain Charge		---	7.3	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GS} =10V, R _G =6Ω I _D =10A, R _L =15Ω	---	14	26	ns
T _r	Rise Time		---	10	19	
T _{d(off)}	Turn-Off Delay Time		---	44	80	
T _f	Fall Time		---	12	23	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1700	---	pF
C _{oss}	Output Capacitance		---	265	---	
C _{riss}	Reverse Transfer Capacitance		---	165	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =25V, L=0.1mH, I _{AS} =25A	28	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V, Force Current	---	---	20	A
I _{SM}	Pulsed Source Current ^{2,6}		---	---	80	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =5A, T _J =25°C	---	---	1.1	V
t _{rr}	Reverse Recovery Time	I _F =20A, dI/dt=100A/μs, T _J =25°C	---	10	---	nS
Q _{rr}	Reverse Recovery Charge		---	3	---	nC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10sec.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=25A
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

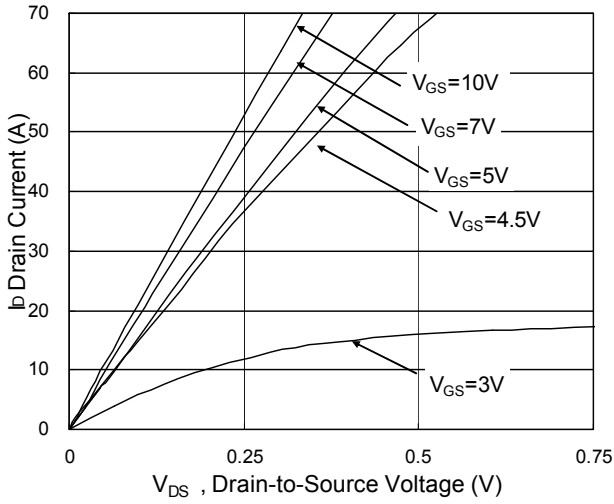


Fig.1 Typical Output Characteristics

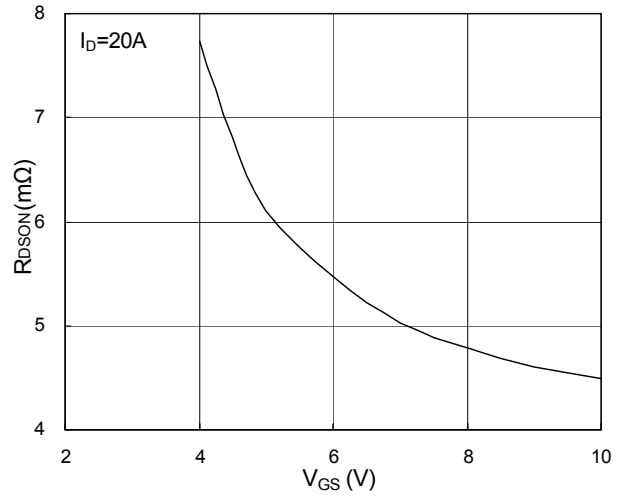


Fig.2 On-Resistance vs. Gate-Source

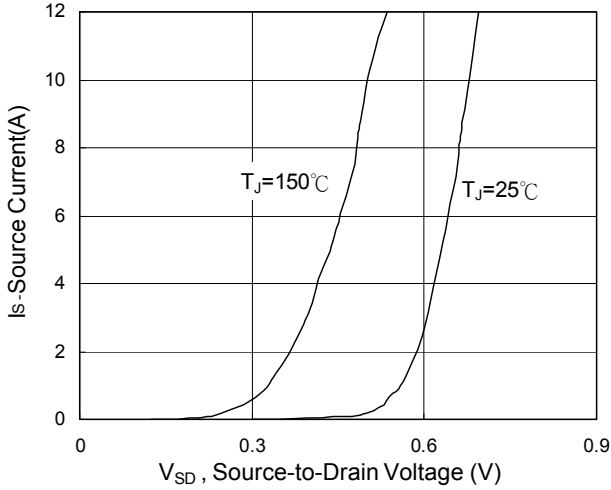


Fig.3 Forward Characteristics of Reverse

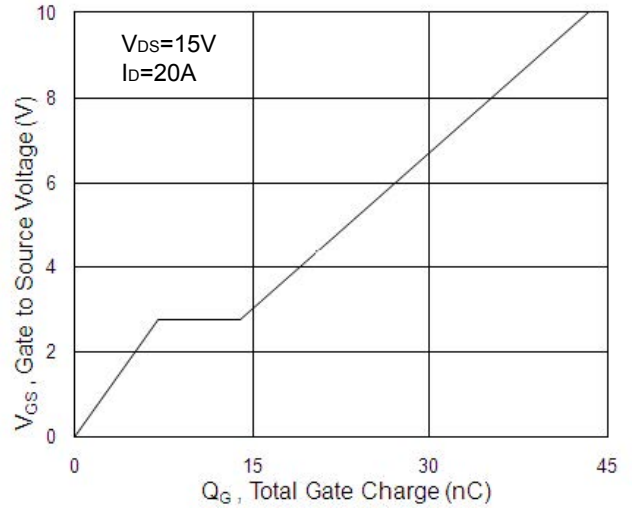


Fig.4 Gate-Charge Characteristics

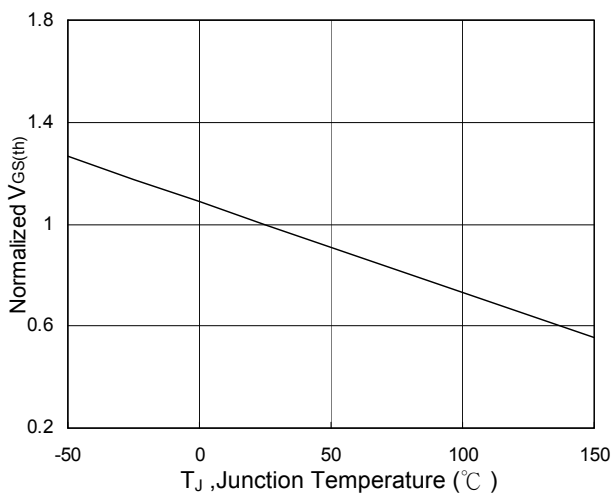


Fig.5 Normalized V_{GS(th)} vs. T_J

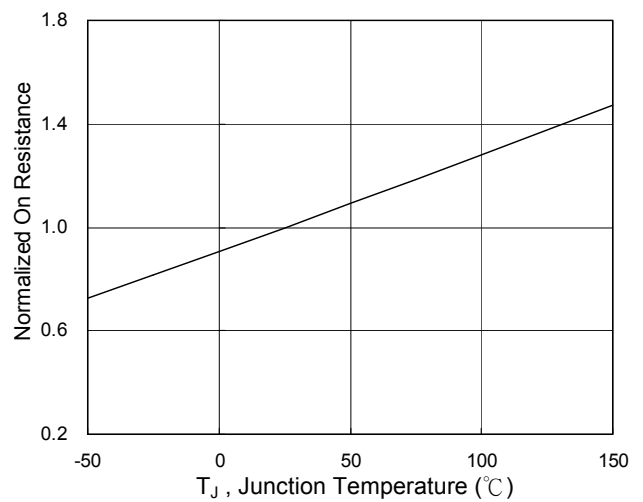


Fig.6 Normalized R_{DS(on)} vs. T_J

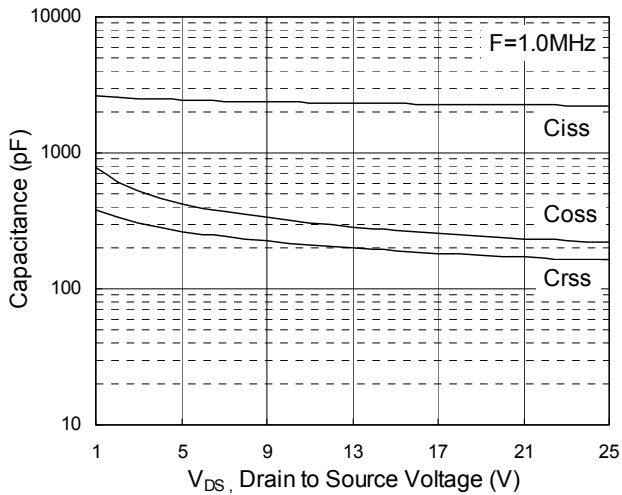


Fig.7 Capacitance

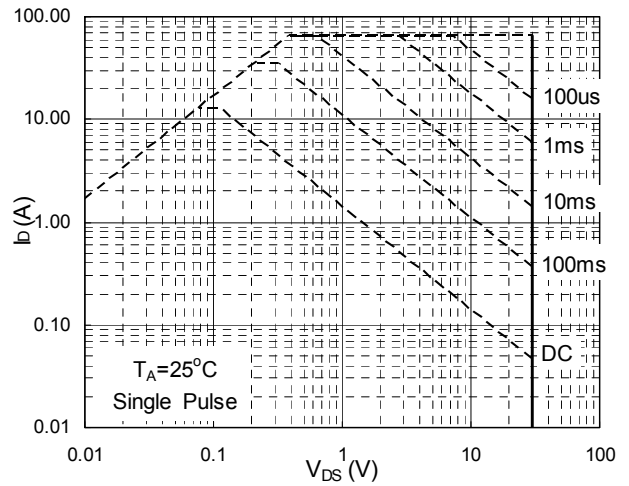


Fig.8 Safe Operating Area

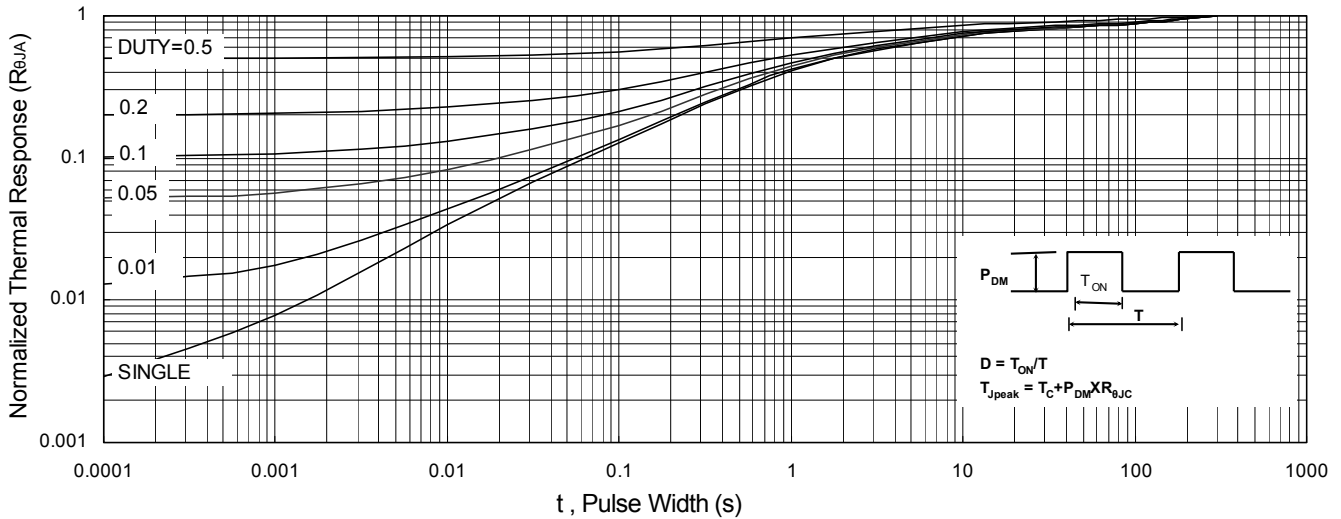


Fig.9 Normalized Maximum Transient Thermal Impedance

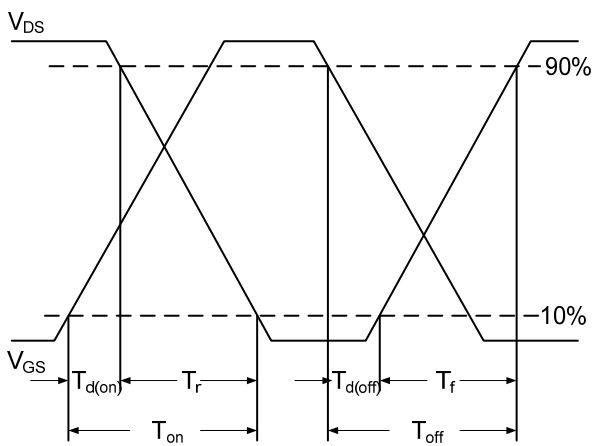


Fig.10 Switching Time Waveform

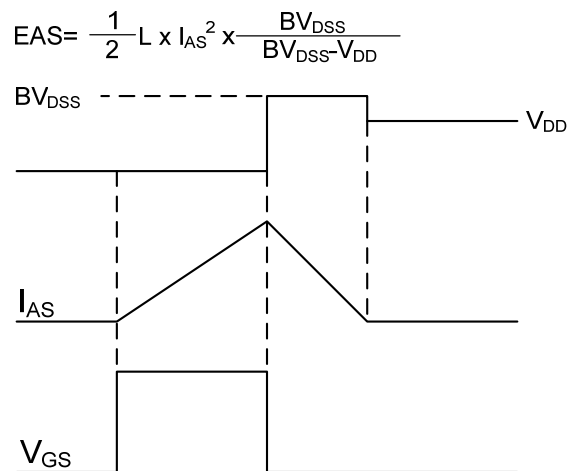


Fig.11 Unclamped Inductive Switching Waveform



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