

General Description

The WST3417 is the highest performance trench P-ch MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST3417 meet the RoHS and Green Product requirement, with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

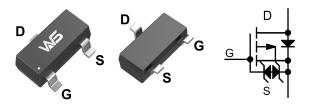
Product Summery

BVDSS	RDSON	ID	
-20V	47mΩ	-4.6A	

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- ESD:3KV

SOT-23N Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	
V_{DS}	Drain-Source Voltage	-20	V	
V_{GS}	Gate-Source Voltage	±12	V	
I _D @T _C =25℃	Continuous Drain Current, V _{GS} @ -4.5V ¹	-4.6	А	
I _D @T _C =70°C	Continuous Drain Current, V _{GS} @ -4.5V ¹	-3.0	Α	
I _{DM}	Pulsed Drain Current ²	-17	Α	
P _D @T _A =25℃	Total Power Dissipation ³	1.0	W	
T _{STG}	Storage Temperature Range	Storage Temperature Range -55 to 150		
T _J	Operating Junction Temperature Range	-55 to 150	${\mathbb C}$	

Thermal Data

Symbol	Parameter	Тур.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹		110	°C/W
ReJC	Thermal Resistance Junction-Case ¹		70	°C/W

P-Ch MOSFET

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	-20			V
$\triangle BV_{DSS}/\triangle T_{J}$	BV _{DSS} Temperature Coefficient	Reference to 25°C , I _D =-1mA		-0.016		V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V , I _D =-3A		47	55	mΩ
		V _{GS} =-2.5V , I _D =-2A		55	70	
		V _{GS} =-1.8V , I _D =-1A		68	85	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.3	-0.75	-1.0	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient			3.97		mV/℃
	Drain-Source Leakage Current $ \frac{V_{DS}\text{=-}16V \text{ , } V_{GS}\text{=}0V \text{ , } T_{J}\text{=}25 ^{\circ}\text{C} }{V_{DS}\text{=-}16V \text{ , } V_{GS}\text{=}0V \text{ , } T_{J}\text{=}55 ^{\circ}\text{C} } $	V _{DS} =-16V , V _{GS} =0V , T _J =25℃			1	
I _{DSS}				5	- uA	
I _{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 8V$, V_{DS} =0V			±100	nA
gfs	Forward Transconductance	V _{DS} =-5V , I _D =-3A		14		S
Q_{g}	Total Gate Charge (-4.5V)			6.2	9	nC
Q_gs	Gate-Source Charge	V _{DS} =-15V , V _{GS} =-4.5V , I _D =-3A		2.2	2.5	
Q _{gd}	Gate-Drain Charge			1.8	2.6	
T _{d(on)}	Turn-On Delay Time			2.7	5.5	
Tr	Rise Time	V_{DD} =-10V , V_{GS} =-4.5V , R_{G} =3.3 Ω , I_{D} =-3A		8.4	15	
$T_{d(off)}$	Turn-Off Delay Time			38	78	ns
T _f	Fall Time			6	12	
C _{iss}	Input Capacitance	V _{DS} =-15V , V _{GS} =0V , f=1MHz		575	810	
C _{oss}	Output Capacitance			98	135	pF
C _{rss}	Reverse Transfer Capacitance			75	110	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current ^{1,4}	V_G = V_D = $0V$, Force Current			-1	Α
I _{SM}	Pulsed Source Current ^{2,4}				-17	Α
V _{SD}	Diode Forward Voltage ²	/ _{GS} =0V , I _S =-1A , T _J =25℃			-1	V
t _{rr}	Reverse Recovery Time			28		nS
Q _{rr}	Reverse Recovery Charge	F=-3A,dI/dt=100A/µs,Tյ=25℃		25		nC

Note:

- 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10 sec.
- 2.The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%
- 3.The power dissipation is limited by 150 $^{\circ}$ C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics

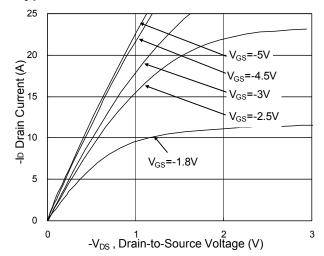


Fig.1 Typical Output Characteristics

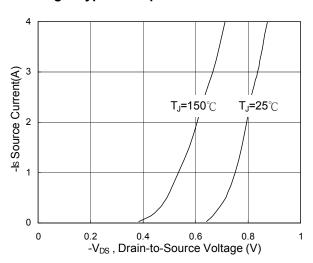


Fig.3 Forward Characteristics of Reverse

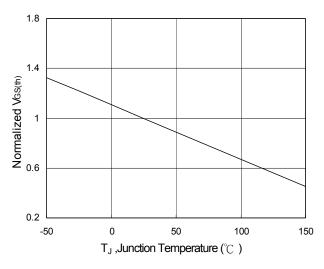


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

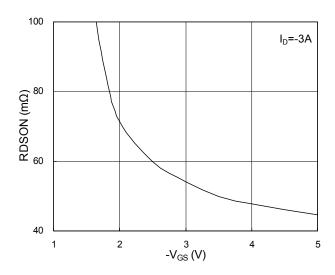


Fig.2 On-Resistance vs. G-S Voltage

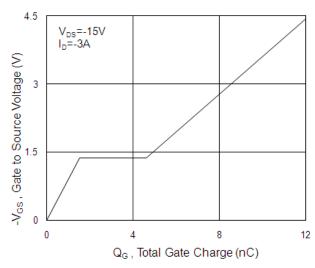


Fig.4 Gate-Charge Characteristics

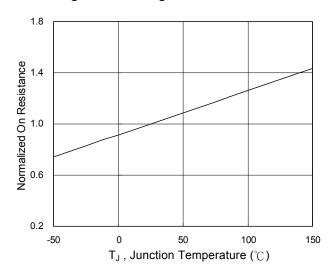
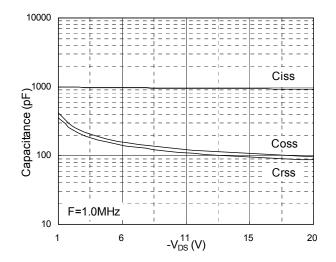


Fig.6 Normalized R_{DSON} vs. T_J







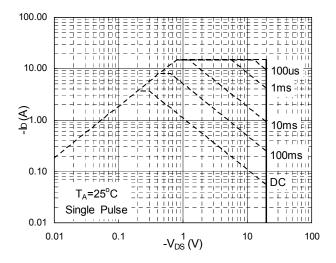


Fig.7 Capacitance

Fig.8 Safe Operating Area

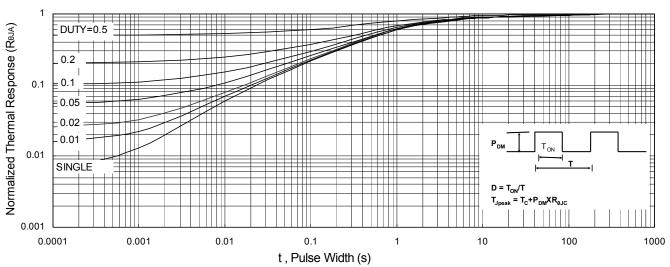
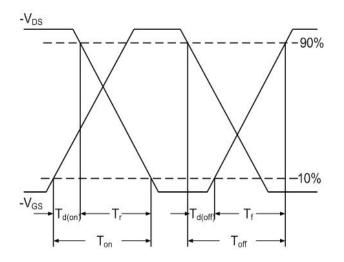


Fig.9 Normalized Maximum Transient Thermal Impedance



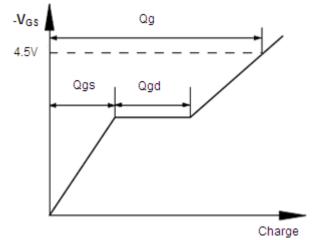


Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform



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