



SGM6501

12-Input, 9-Output Video Switch Matrix with Output Drivers, Input Clamp, and Bias Circuitry

GENERAL DESCRIPTION

The SGM6501 is a video switch matrix which features 12 input channels and 9 output channels. The architecture allows any of the 12 inputs to be routed to any of the 9 outputs, and it supports one input to one output or one input to more outputs switching. The routing map is configured by I²C-compatible serial interface.

The SGM6501 has the input clamp function and bias circuitry, the input clamp or bias mode is selectable through I²C interface. Integrated clamp is supported by each input. The function is to set video output sync level to approximately 600mV. If sync signal (Chroma, Pb, Pr) is absent, the input is biased by approximately 1.3V, which is the center of input voltage range.

The SGM6501 is available in Green SSOP-28 and TSSOP-28 packages. It operates over an ambient temperature range of -40°C to +85°C.

FEATURES

- **Single-Supply Voltage Range: 3.1V to 5.5V**
- **12 × 9 Crosspoint Switch Matrix**
- **Supports Standard Definition (SD), Progressive Scan (PS), and High Definition (HD) Video**
- **-3dB Bandwidth: 84MHz**
- **Low Crosstalk: -74dB at 1MHz**
- **Programmable Gain Options:
6dB, 7dB, 8dB, or 9dB**
- **Input Bias Circuitry and Input Clamp Function**
- **Supports I²C Serial Interface**
- **Double-Load 75Ω Output Drivers**
- **AC- or DC-Coupled Inputs and Outputs**
- **Available in Green SSOP-28 and TSSOP-28 Packages**

APPLICATIONS

Security and Surveillance
TV and HDTV
Automotive Entertainment System
Media Centers
Video Routing
Cable and Satellite Set-Top Boxes

12-Input, 9-Output Video Switch Matrix with Output Drivers, Input Clamp, and Bias Circuitry

SGM6501

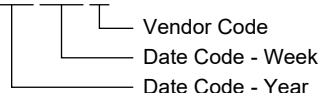
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6501	SSOP-28	-40°C to +85°C	SGM6501YSS28G/TR	SGM6501 YSS28 XXXXX	Tape and Reel, 2000
	TSSOP-28	-40°C to +85°C	SGM6501YTS28G/TR	SGM6501 YTS28 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

XXXXX = Date Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (DC).....	-0.3V to 6V
Analog and Digital Input/Output Voltage Range-0.3V to $V_{CC} + 0.3V$
Output Current per Channel.....	40mA (MAX)
Junction Temperature.....	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s).....	+260°C
ESD Susceptibility	
HBM (SSOP-28)	8000V
HBM (TSSOP-28)	7000V
CDM	2000V
MM.....	400V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range	-40°C to +85°C
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OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

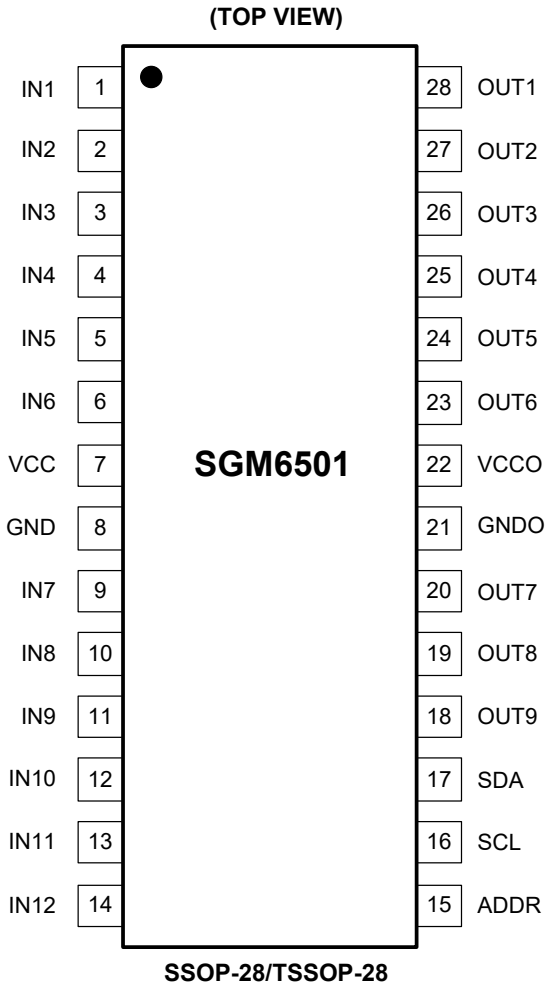
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN1	Input Pin (Channel 1).
2	IN2	Input Pin (Channel 2).
3	IN3	Input Pin (Channel 3).
4	IN4	Input Pin (Channel 4).
5	IN5	Input Pin (Channel 5).
6	IN6	Input Pin (Channel 6).
7	VCC	Positive Power Supply.
8	GND	Ground.
9	IN7	Input Pin (Channel 7).
10	IN8	Input Pin (Channel 8).
11	IN9	Input Pin (Channel 9).
12	IN10	Input Pin (Channel 10).
13	IN11	Input Pin (Channel 11).
14	IN12	Input Pin (Channel 12).
15	ADDR	I ² C Address Selection Pin. "0" = 0x06 (0000 0110) "1" = 0x86 (1000 0110)
16	SCL	I ² C Clock Signal.
17	SDA	I ² C Data Signal.
18	OUT9	Output Pin (Channel 9).
19	OUT8	Output Pin (Channel 8).
20	OUT7	Output Pin (Channel 7).
21	GNDO	Ground.
22	VCCO	Positive Power Supply for Output Drivers.
23	OUT6	Output Pin (Channel 6).
24	OUT5	Output Pin (Channel 5).
25	OUT4	Output Pin (Channel 4).
26	OUT3	Output Pin (Channel 3).
27	OUT2	Output Pin (Channel 2).
28	OUT1	Output Pin (Channel 1).

12-Input, 9-Output Video Switch Matrix with SGM6501 Output Drivers, Input Clamp, and Bias Circuitry

ELECTRICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{IN} = 1V_{PP}$, input bias mode, one-to-one routing, 6dB gain, all inputs AC-coupled with $0.1\mu\text{F}$, unused inputs AC-terminated through 75Ω to GND, all outputs AC-coupled with $220\mu\text{F}$ into 150Ω loads, referenced to 400kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General						
Supply Voltage Range	V_{CC}		3.1	5	5.5	V
DC Performance						
Video Output Range	V_{OUT}			2.8		V_{PP}
Supply Current	I_Q	No load, all outputs enabled		92	127	mA
DC Output Level	V_{clamp}	Clamp mode, input floating, 6dB gain setting		0.86		V
DC Output Level	V_{bias}	Bias mode, input floating, 6dB gain setting		1.3		V
Power Supply Rejection Ratio	PSRR	All channels, DC input = 0.5V		60		dB
Off Channel Output Impedance	R_{OFF}	Output disabled		3		k Ω
AC Performance						
Channel Gain Error	AV_{SD}	All channels, all gain setting, DC	-0.2	0	0.2	dB
Gain Step	AV_{STEP}	All channels, DC	0.9	1	1.1	dB
-1dB Bandwidth	f_{-1dB}	$V_{OUT} = 1.4V_{PP}$		59		MHz
-3dB Bandwidth	f_C	$V_{OUT} = 1.4V_{PP}$		84		MHz
Differential Gain	DG	$V_{CC} = 5\text{V}$, 4.43MHz		0.1		%
Differential Phase	DP	$V_{CC} = 5\text{V}$, 4.43MHz		0.3		$^\circ$
SD Output Distortion	THD_{SD}	$V_{OUT} = 1.4V_{PP}$, 5MHz, $V_{CC} = 5\text{V}$		0.2		%
HD Output Distortion	THD_{HD}	$V_{OUT} = 1.4V_{PP}$, 22MHz, $V_{CC} = 5\text{V}$		0.9		%
Input Crosstalk	X_{TALK1}	1MHz, $V_{OUT} = 2V_{PP}$		-74		dB
	X_{TALK2}	15MHz, $V_{OUT} = 2V_{PP}$		-51		dB
Output Crosstalk	X_{TALK3}	1MHz, $V_{OUT} = 2V_{PP}$		-70		dB
	X_{TALK4}	15MHz, $V_{OUT} = 2V_{PP}$		-47		dB
Multi-Channel Crosstalk	X_{TALK5}	4.43MHz, $V_{OUT} = 2V_{PP}$		-52		dB
	X_{TALK6}	6.5MHz, $V_{OUT} = 2V_{PP}$		-49		dB
	X_{TALK7}	9MHz, $V_{OUT} = 2V_{PP}$		-47		dB
Signal-to-Noise Ratio	SNR_{SD}	NTC-7 weighting, 4.2MHz LP, 100kHz HP		77		dB
Channel Noise	V_{NOISE}	400kHz to 100MHz, input referred		20		nV/ $\sqrt{\text{Hz}}$
Amplifier Recovery Time	AMP_{ON}	Post I ² C programming		200		ns

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I²C BUS CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Low	V _{IL}	SDA, SCL, ADDR	0		1.5	V
Digital Input High	V _{IH}	SDA, SCL, ADDR	3.0		V _{CC}	V
Clock Frequency	f _{SCL}	SCL		100		kHz
Input Rise Time	t _r	1.5V to 3V		1000		ns
Input Fall Time	t _f	1.5V to 3V		300		ns
Clock Low Period	t _{LOW}			4.7		μs
Clock High Period	t _{HIGH}			4.0		μs
Data Set-up Time	t _{SU, DAT}			300		ns
Data Hold Time	t _{HD, DAT}			0		ns
Set-up Time from Clock High to Stop	t _{SU, STO}			4		μs
Start Set-up Time Following a Stop	t _{BUF}			4.7		μs
Start Hold Time	t _{HD, STA}			4		μs
Start Set-up Time Following Clock Low to High	t _{SU, STA}			4.7		μs

REGISTER MAPS

I²C Slave Address of SGM6501: 0x06 (0000 0110)

The I²C address is 0x06 (0000 0110). When the ADDR pin goes high, it can be to offset to 0x86 (1000 0110).

W: Write only bit(s)

PORV: Power-On Reset Value

Output Control Register

Table 1. Output Control Register Maps

Address	Register Name	Bit7	Bit6	Bit5	Bit4 ⁽¹⁾	Bit3	Bit2	Bit1	Bit0
0x01	OUT1	Enable	Gain[1:0]		IN[4:0]				
0x02	OUT2	Enable	Gain[1:0]		IN[4:0]				
0x03	OUT3	Enable	Gain[1:0]		IN[4:0]				
0x04	OUT4	Enable	Gain[1:0]		IN[4:0]				
0x05	OUT5	Enable	Gain[1:0]		IN[4:0]				
0x06	OUT6	Enable	Gain[1:0]		IN[4:0]				
0x07	OUT7	Enable	Gain[1:0]		IN[4:0]				
0x08	OUT8	Enable	Gain[1:0]		IN[4:0]				
0x09	OUT9	Enable	Gain[1:0]		IN[4:0]				

NOTE:

1. IN[4] is provided for forward compatibility and should always be written as '0' in the SGM6501.

Table 2. Output Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7]	Enable	Channel Enable 0 = Power-Down ⁽¹⁾ 1 = Enable		0	W
D[6:5]	Gain[1:0]	Channel Gain 00 = 6dB 01 = 7dB 10 = 8dB 11 = 9dB		00	W
D[4:0]	IN[4:0]	Input Selected to Drive the Output 00000 = Off ⁽²⁾ 00001 = IN1 00010 = IN2 ... 01100 = IN12		00000	W

NOTES:

- Power-down places the output in a high-impedance state so multiple SGM6501 devices may be paralleled. Power-down also de-selects any input routed to the specified output.
- When all inputs are off, the amplifier input is tied to approximately 150mV and the output goes to approximately 300mV with the 6dB gain setting.

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REGISTER MAPS (continued)

Clamp Control Register

Table 3. Clamp Control Register Maps

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D	CLAMP1	Clmp8	Clmp7	Clmp6	Clmp5	Clmp4	Clmp3	Clmp2	Clmp1
0x1E	CLAMP2	Reserved	Reserved	Reserved	Reserved	Clmp12	Clmp11	Clmp10	Clmp9

Table 4. CLAMP1 Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7:0]	Clmp8	Clamp/Bias Selection (for Input 1 to Input 8) 0 = Bias 1 = Clamp		0	W
	Clmp7			0	W
	Clmp6			0	W
	Clmp5			0	W
	Clmp4			0	W
	Clmp3			0	W
	Clmp2			0	W
	Clmp1			0	W

Table 5. CLAMP2 Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7:4]	Reserved	Reserved.			
D[3:0]	Clmp12	Clamp/Bias Selection (for Input 9 to Input 12) 0 = Bias 1 = Clamp		0	W
	Clmp11			0	W
	Clmp10			0	W
	Clmp9			0	W

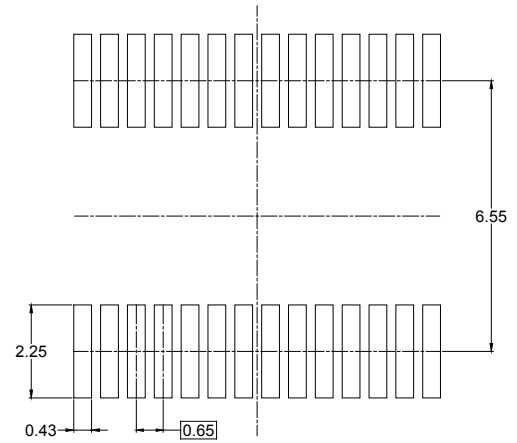
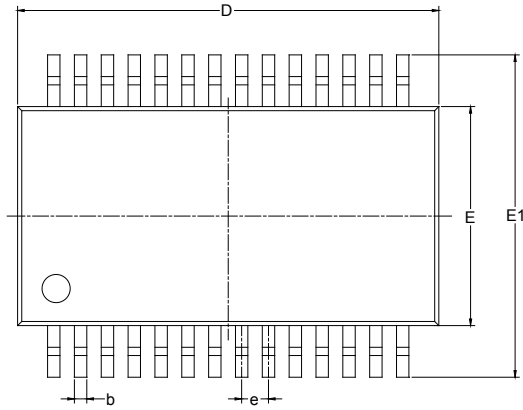
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

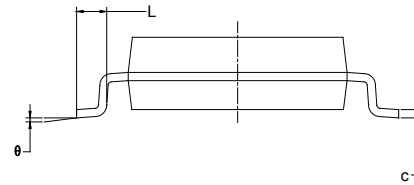
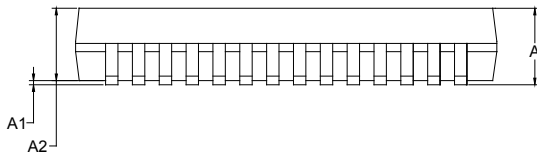
JANUARY 2013 – REV.A.3 to REV.A.4	Page
Added Recommended Land Pattern Information	13, 14
Added Tape and Reel Information.....	15, 16
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MAY 2011 – REV.A.2 to REV.A.3	Page
Updated Package Description	All
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MARCH 2011 – REV.A.1 to REV.A.2	Page
Updated Package Outline Dimensions section	13
Added Tape and Reel Information.....	10, 11
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JANUARY 2011 – REV.A to REV.A.1	Page
Updated Pin Configurations section	3
<hr/>	
Changes from Original (NOVEMBER 2010) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

SSOP-28



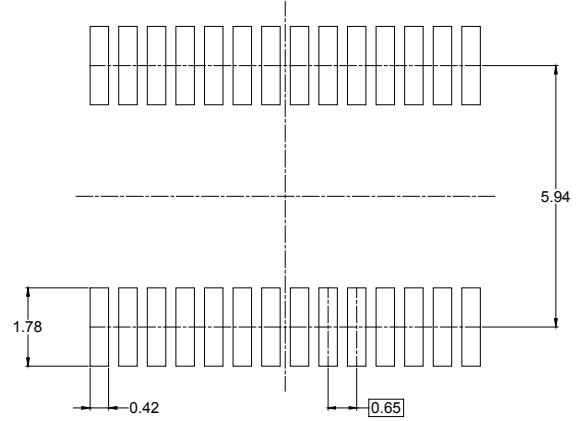
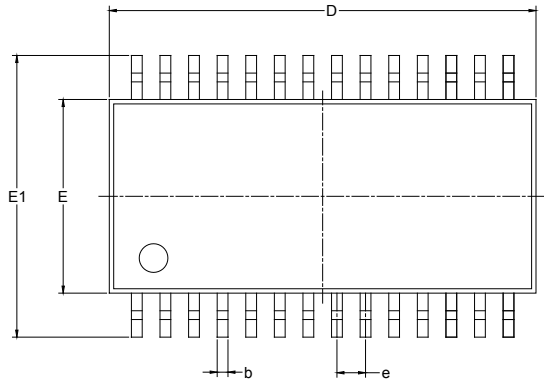
RECOMMENDED LAND PATTERN (Unit: mm)



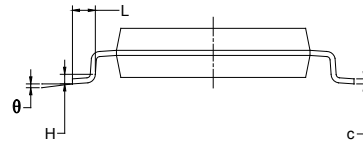
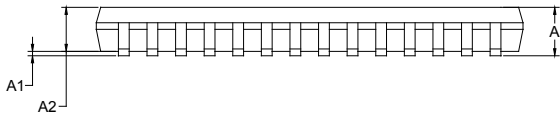
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		2.000		0.079
A1	0.050		0.002	
A2	1.650	1.850	0.065	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	9.900	10.500	0.390	0.413
E	5.000	5.600	0.197	0.220
E1	7.400	8.200	0.291	0.323
e	0.65 BSC		0.026 BSC	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

TSSOP-28



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.020	0.150	0.001	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SSOP-28	13"	16.4	8.20	10.50	0.30	4.0	12.0	2.0	16.0	Q1
TSSOP-28	13"	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002