

## DS34C87 CMOS Quad TRI-STATE<sup>®</sup> Differential Line Driver

### General Description

The DS34C87 is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

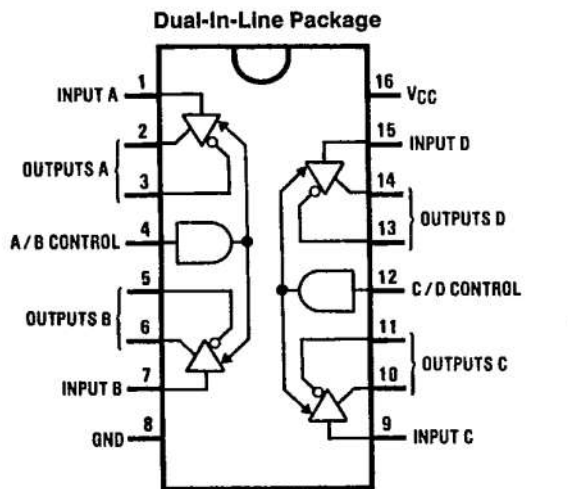
The DS34C87 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The DS34C87 also includes special power up and down circuitry which will TRI-STATE the outputs during power up or down, preventing spurious glitches on its outputs. This device has separate enable circuitry for each pair of the four drivers. The DS34C87 is pin compatible to the DS3487.

All inputs are protected against damage due to electrostatic discharge by diodes to  $V_{CC}$  and ground.

### Features

- TTL input compatible
- Typical propagation delays: 8 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when  $V_{CC} = 0V$
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current

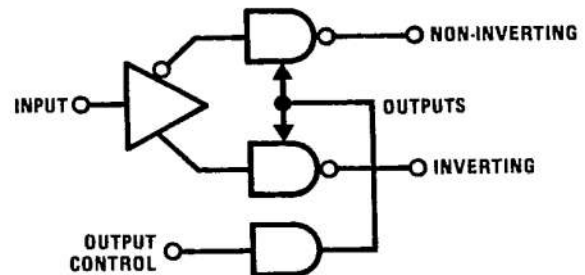
### Connection and Logic Diagrams



TL/F/8576-1

#### Top View

Order Number DS34C87J,  
DS34C87N or DS34C87M  
See NS Package Number  
J16A, M16A or N16A



TL/F/8576-2

### Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state

X = Irrelevant

H = High logic state

Z = TRI-STATE (high impedance)

For complete specifications  
see the Interface Databook.

## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to 7.0V
DC Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to 7V
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 150$ mA
DC $V_{CC}$ or GND Current ( $I_{CC}$ )	$\pm 150$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation (Note 3) ( $P_D$ )	500 mW
Lead Temperature ( $T_L$ ) (Soldering 4 sec)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.50	5.50	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	-40	+85	°C
Input Rise or Fall Times ( $t_r, t_f$ )		500	ns

## DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IH}$	High Level Input Voltage		2.0			V
$V_{IL}$	Low Level Input Voltage				0.8	V
$V_{OH}$	High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = -20$ mA	2.5			V
$V_{OL}$	Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = 48$ mA			0.5	V
$V_T$	Differential Output Voltage	$R_L = 100 \Omega$ (Note 5)	2.0			V
$ V_T  -  \bar{V}_T $	Difference In Differential Output	$R_L = 100 \Omega$ (Note 5)			0.4	V
$V_{OS}$	Common Mode Output Voltage	$R_L = 100 \Omega$ (Note 5)			3.0	V
$ V_{OS} - \bar{V}_{OS} $	Difference In Common Mode Output	$R_L = 100 \Omega$ (Note 5)			0.4	V
$I_{IN}$	Input Current	$V_{IN} = V_{CC}, GND, V_{IH},$ or $V_{IL}$			$\pm 1.0$	$\mu A$
$I_{CC}$	Quiescent Supply Current	$I_{OUT} = 0 \mu A$ , $V_{IN} = V_{CC}$ or GND $V_{IN} = 2.4V$ or $0.5V$ (Note 6)		200 0.8		$\mu A$ mA
$I_{OZ}$	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Control = $V_{IL}$		$\pm 0.5$	$\pm 5.0$	$\mu A$
$I_{SC}$	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND (Note 7)	-30		-150	mA
$I_{OFF}$	Output Leakage Current Power Off	$V_{CC} = 0V$ $V_{OUT} = 6V$ $V_{OUT} = -0.25V$			100 -100	$\mu A$ $\mu A$

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.

**Note 3:** Power Dissipation temperature derating—plastic "N" package: -12 mW/°C from 65°C to 85°C.

ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** Unless otherwise specified, min/max limits apply across the -40°C to 85°C temperature range. All typicals are given for  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

**Note 5:** See EIA Specification RS-422 for exact test conditions.

**Note 6:** Measured per input. All other inputs at  $V_{CC}$  or GND.

**Note 7:** Only one output at a time should be shorted.

## Switching Characteristics $V_{CC} = 5V \pm 10\%$ , $t_r = t_f = 6\text{ ns}$ (Figures 1, 2, 3, and 4) (Note 4)

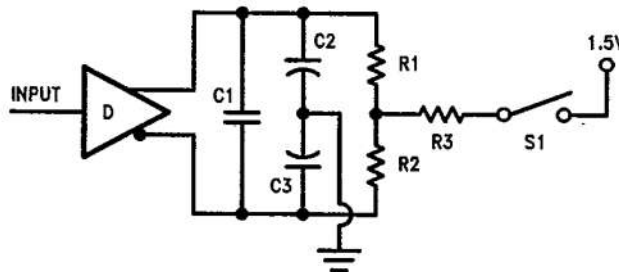
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Input to Output	S1 Open		8		ns
Skew	(Note 8)	S1 Open		0.5		ns
$t_{TLH}$ , $t_{THL}$	Differential Output Rise And Fall Times	S1 Open		8		ns
$t_{PZH}$	Output Enable Time	S1 Closed		13		ns
$t_{PZL}$	Output Enable Time	S1 Closed		15		ns
$t_{PHZ}$	Output Disable Time (Note 9)	S1 Closed		9		ns
$t_{PLZ}$	Output Disable Time (Note 9)	S1 Closed		10		ns
$C_{PD}$	Power Dissipation Capacitance (Note 10)			100		pF
$C_{IN}$	Input Capacitance			10		pF

**Note 8:** Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

**Note 9:** Output disable time is the delay from ENABLE or ENABLE being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

**Note 10:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## AC Test Circuit and Switching Time Waveforms



Note:  $C1 = C2 = C3 = 40\text{ pF}$ ,  $R1 = R2 = 50\Omega$ ,  $R3 = 500\Omega$

**FIGURE 1. AC Test Circuit**

## AC Test Circuit and Switching Time Waveforms (Continued)

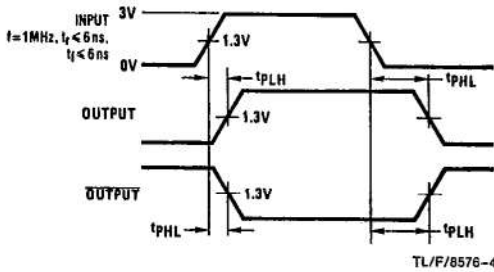


FIGURE 2. Propagation Delays

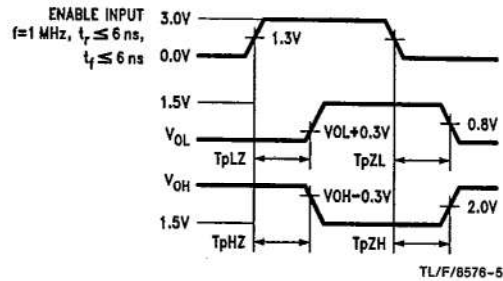


FIGURE 3. Enable and Disable Times

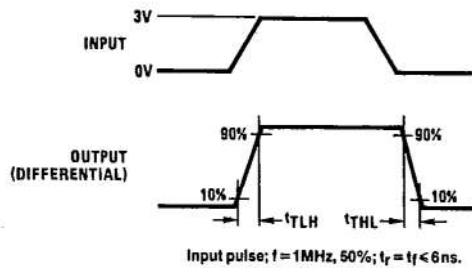
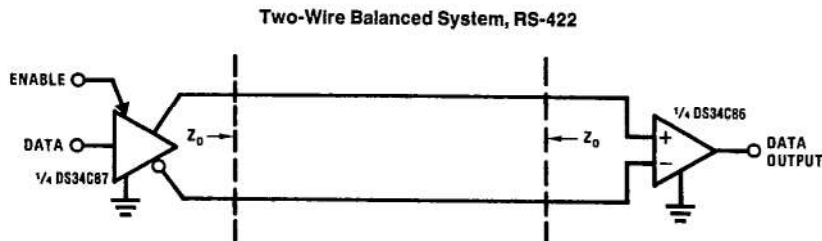


FIGURE 4. Differential Rise and Fall Times

## Typical Applications



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