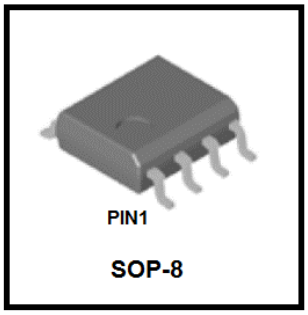
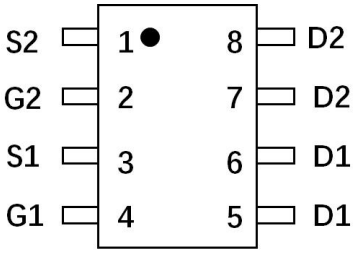
LDP4098T1G

Dual P-Channel MOSFET





Top View

1. FEATURES

- Low RDS(on) trench technology.
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.

2. ORDERING INFORMATION

Device	Marking	Shipping
LDP4098T1G	4098	4000/Tape&Reel

3. MAXIMUM RATINGS(Ta = 25ºC unless otherwise stated)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		VDSS	-30	V
Gate−to−Source Voltage		VGS	±20	V
Continuous Drain Current	TA =25°C	ID	-5.3	A
	TA =70°C		-4.2	
Pulsed Drain Current (Note 3)		IDM	-25	
Power Dissipation(Note 2)	TA =25°C	PD	2.5	W
	TA =70°C		1.9	
Operating Junction Temperature and Storage Temperature Range		TJ , TSTG	−55 ~+150	℃

1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

2. Repetitive rating, pulse width limited by junction temperature.

3.The RθJA is the sum of the thermal impedence from junction to lead RθJL and lead to ambient.

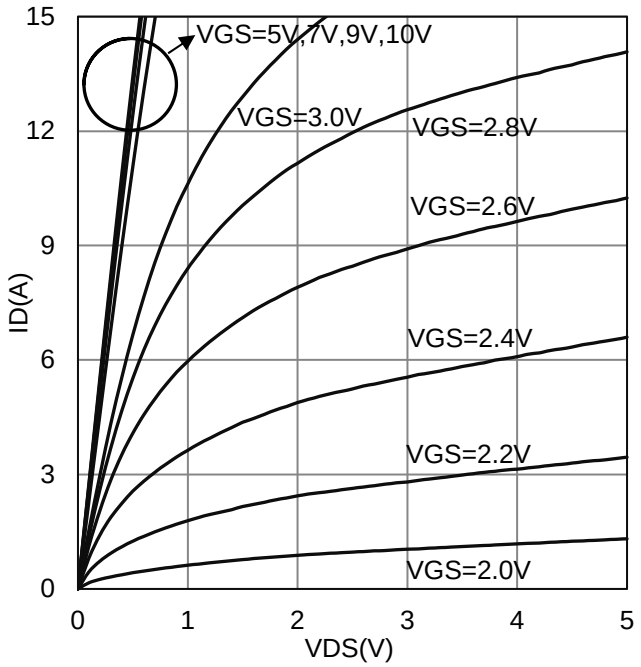
4. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Junction-to-Ambient(Note 1)	RθJA	50	℃/W

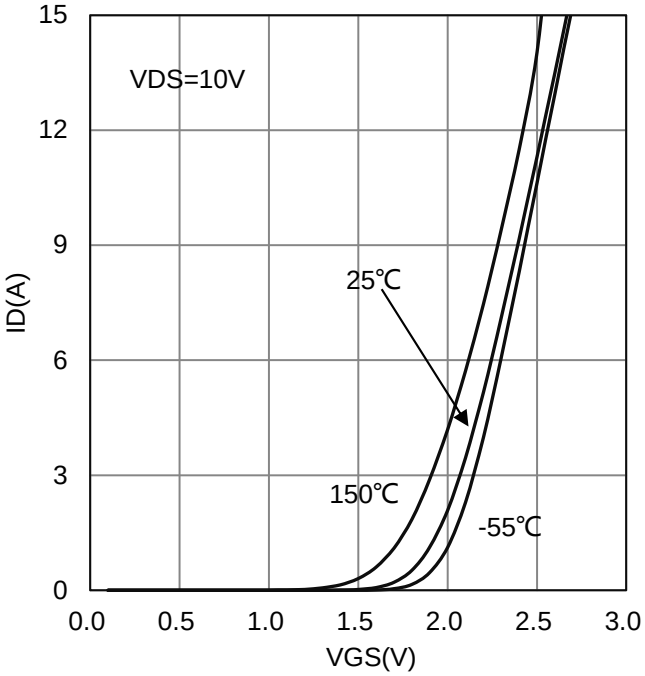
5. ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage (ID =-250μA, VGS =0V)		BVDSS	-30	-	-	V
Zero Gate Voltage Drain Current (VDS =-24V, VGS =0V) (VDS =-24V, VGS =0V,TJ = 55°C)		IDSS	- -	- -	-1 -5	μA
Gate-Body Leakage (VDS = 0 V, VGS = ±20 V)		IGSS	-	-	±100	nA
Gate-Source Threshold Voltage (VDS = VGS , ID = 250 uA)		VGS(th)	-1	-1.4	-2.5	V
Drain-Source On-Resistance (VGS =-10V, ID =-4.1A) (VGS =-4.5V, ID =-3A)		RDS(on)	- -	38 45	50 70	mΩ
Diode Forward Voltage (IS =-1A,VGS =0V)		VSD	-	-0.77	-1	V
Dynamic						
Input Capacitance	(VGS =0V, VDS =-15V, f=1MHz)	Ciss	-	662	-	pF
Output Capacitance		Coss	-	80	-	
Reverse Transfer Capacitance		Crss	-	75	-	
Gate resistance (VGS =0V, VDS =0V, f=1MHz)		Rg	-	6	-	Ω
Total Gate Charge(10V)	(VGS =-10V, VDS =-15V, ID =-4A)	Qg	-	13	-	nC
Total Gate Charge(4.5V)		Qg	-	6.6	-	
Gate-Source Charge		Qgs	-	1.1	-	
Gate-Drain Charge		Qgd	-	3.3	-	
Turn-On Delay Time	(VGS =-10V, VDS =-15V, RL =3.6 Ω,RGEN =3Ω)	td(on)	-	39	-	ns
Rise Time		tr	-	21	-	
Turn-Off Delay Time		td(off)	-	48	-	
Fall Time		tf	-	7	-	

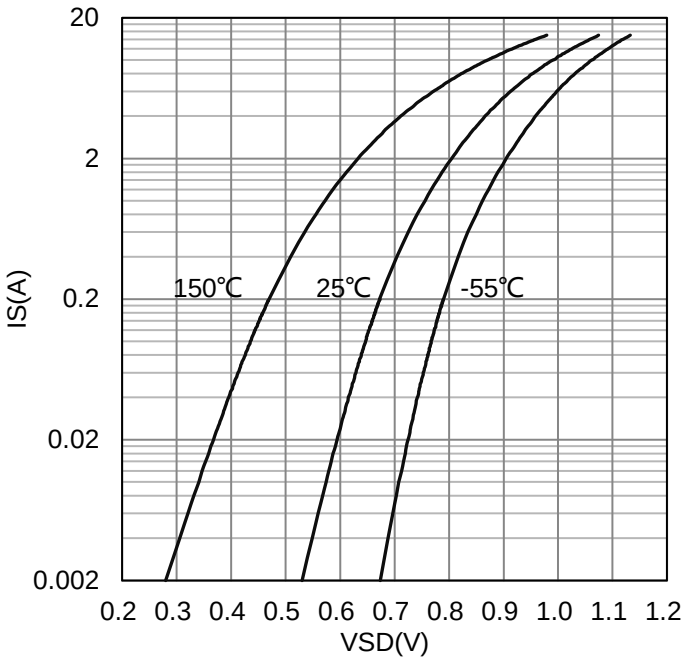
6. ELECTRICAL CHARACTERISTICS CURVES



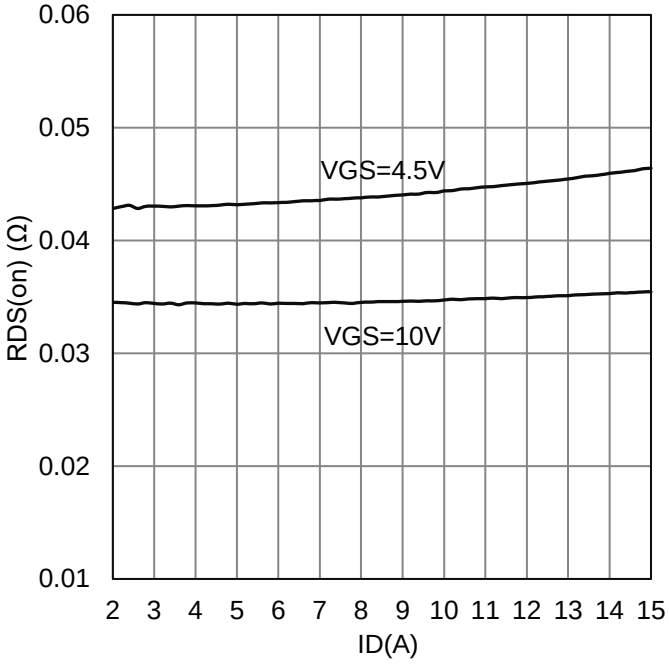
ID vs. VDS



ID vs. VGS

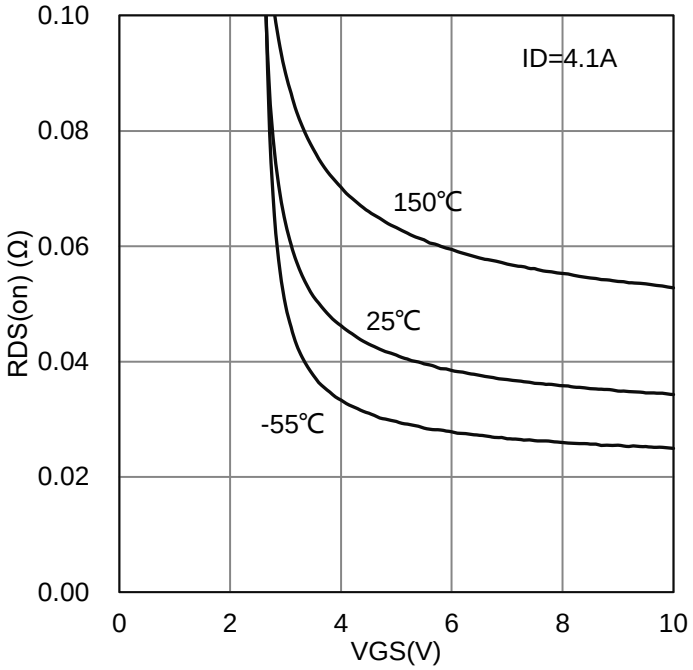


IS vs. VSD

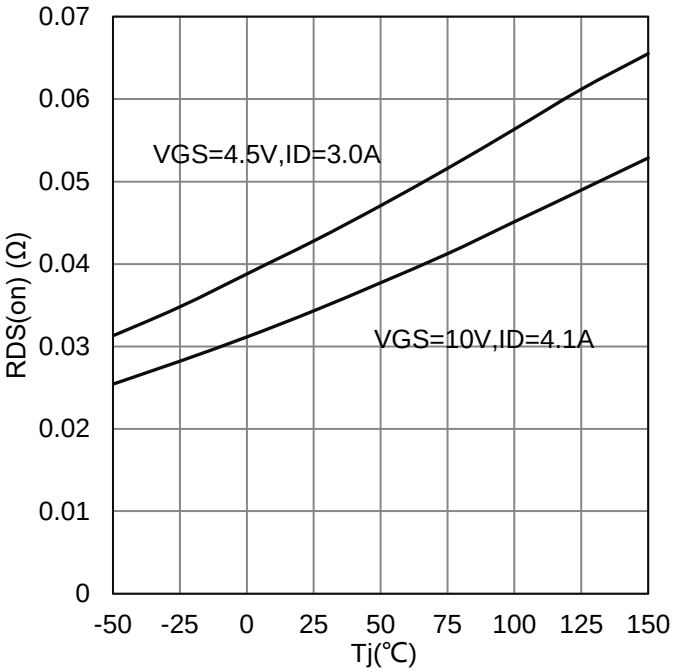


RDS(on) vs. ID

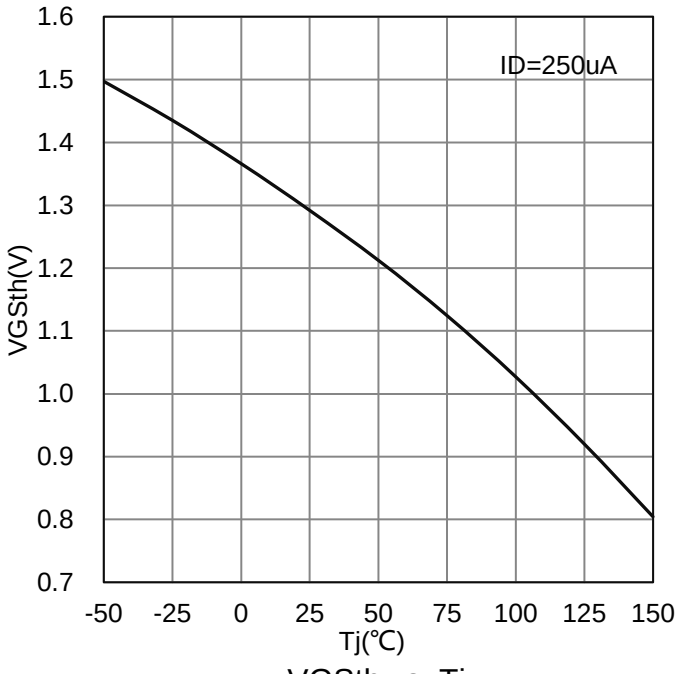
6. ELECTRICAL CHARACTERISTICS CURVES(Con.)



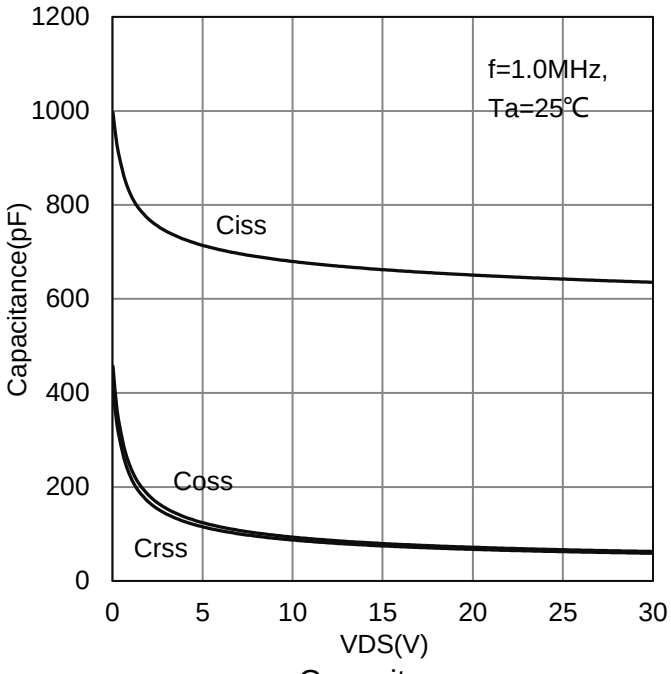
RDS(on) vs. VGS



RDS(on) vs. Tj



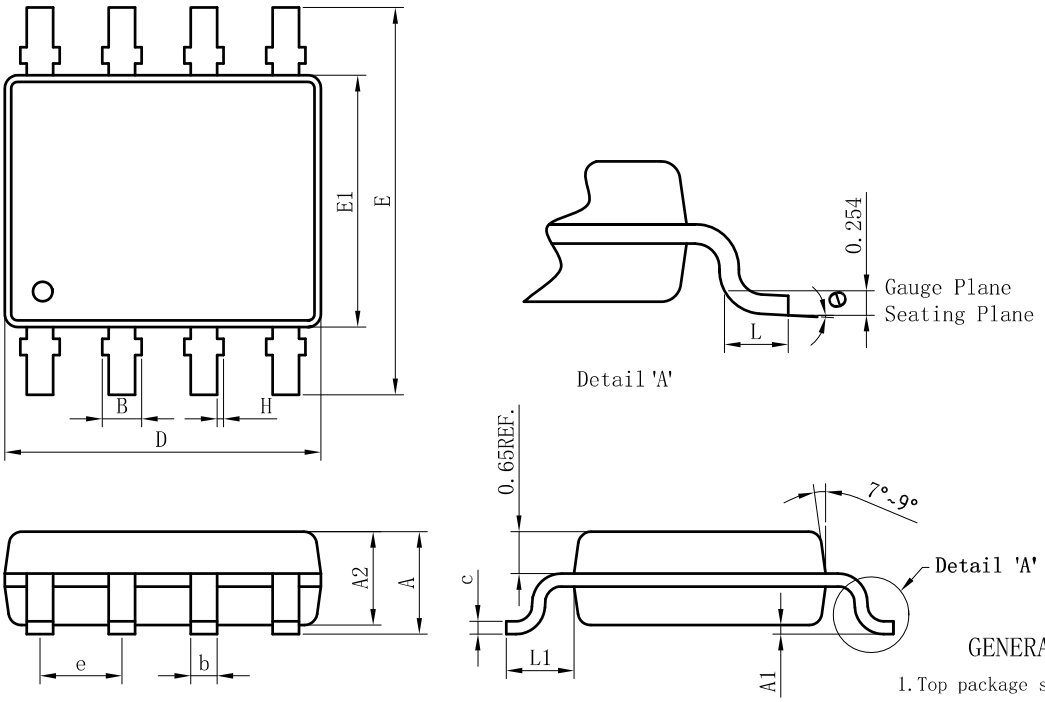
VGSth vs. Tj



Capacitance

7.OUTLINE AND DIMENSIONS

SOP8

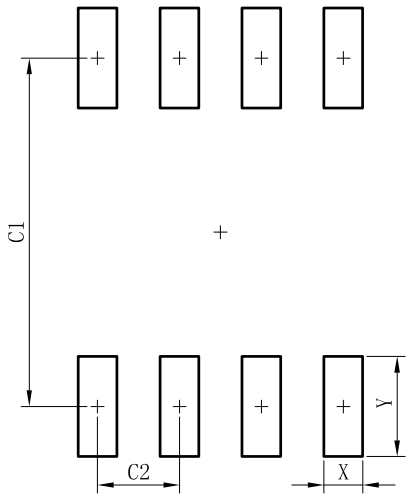


SOP8			
DIM	MIN	NOR	MAX
A	—	—	1.75
A1	0.10	0.15	0.20
A2	1.35	1.45	1.55
b	0.33	0.42	0.51
c	0.15	0.22	0.29
D	4.77	4.90	5.03
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.46	0.66	0.86
L1	0.85	1.05	1.25
θ	0°	5°	8°
B	—	—	0.55
H	0	0.05	0.10
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
5. Dimension "b" Does Not Include Dambar Protrusion.

8.SOLDERING FOOTPRINT



SOP8	
DIM	(mm)
X	0.60
Y	1.55
C1	5.40
C2	1.27

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