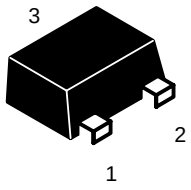
Bias Resistor Transistors

NPN Silicon Surface Mount Transistors With Monolithic Bias Resistor Network

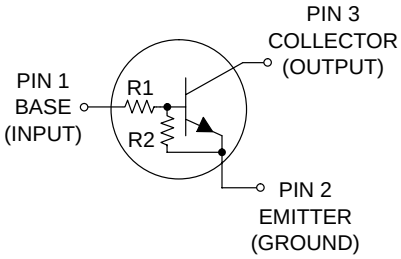
LDTC114EM3T5G Series
S-LDTC114EM3T5G Series

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT-723 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SOT-723 Package can be Soldered using Wave or Reflow.
- Available in 4 mm, 8000 Unit Tape & Reel
- These are Pb-Free Devices.
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



SOT-723



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

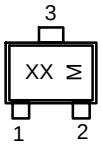
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	260 (Note 1) 600 (Note 2) 2.0 (Note 1) 4.8 (Note 2)	mW mW/°C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	480 (Note 1) 205 (Note 2)	°C/W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

1. FR–4 @ Minimum Pad
2. FR–4 @ 1.0 x 1.0 inch Pad

MARKING DIAGRAM



xx = Specific Device Code
M = Date Code

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

DEVICE MARKING AND RESISTOR VALUES

Device		Marking	R1 (K)	R2 (K)	Package	Shipping
LDTC114EM3T5G	S-LDTC114EM3T5G	8A	10	10	SOT−723	8000/Tape & Reel
LDTC124EM3T5G	S-LDTC124EM3T5G	8B	22	22		
LDTC144EM3T5G	S-LDTC144EM3T5G	8C	47	47		
LDTC114YM3T5G	S-LDTC114YM3T5G	8D	10	47		
LDTC114TM3T5G	S-LDTC114TM3T5G	94	10	∞		
LDTC143TM3T5G	S-LDTC143TM3T5G	8F	4.7	∞		
LDTC123EM3T5G	S-LDTC123EM3T5G	8H	2.2	2.2		
LDTC143EM3T5G	S-LDTC143EM3T5G	8J	4.7	4.7		
LDTC143ZM3T5G	S-LDTC143ZM3T5G	8K	4.7	47		
LDTC124XM3T5G	S-LDTC124XM3T5G	8L	22	47		
LDTC123JM3T5G	S-LDTC123JM3T5G	8M	2.2	47		
LDTC115EM3T5G	S-LDTC115EM3T5G	8N	100	100		
LDTC144WM3T5G	S-LDTC144WM3T5G	8P	47	22		
LDTC144TM3T5G	S-LDTC144TM3T5G	8T	47	∞		

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current	LDTC114EM3T5G	I_{EBO}	−	−	0.5	mAdc
(V_{EB} = 6.0 V, I_C = 0)	LDTC124EM3T5G		−	−	0.2	
	LDTC144EM3T5G		−	−	0.1	
	LDTC114YM3T5G		−	−	0.2	
	LDTC114TM3T5G		−	−	0.9	
	LDTC143TM3T5G		−	−	1.9	
	LDTC123EM3T5G		−	−	2.3	
	LDTC143EM3T5G		−	−	1.5	
	LDTC143ZM3T5G		−	−	0.18	
	LDTC124XM3T5G		−	−	0.13	
	LDTC123JM3T5G		−	−	0.2	
	LDTC115EM3T5G		−	−	0.05	
	LDTC144WM3T5G		−	−	0.13	
	LDTC144TM3T5G		−	−	0.2	
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc
ON CHARACTERISTICS (Note 3)						
DC Current Gain	LDTC114EM3T5G	h_{FE}	35	60	−	
(V_{CE} = 10 V, I_C = 5.0 mA)	LDTC124EM3T5G		60	100	−	
	LDTC144EM3T5G		80	140	−	
	LDTC114YM3T5G		80	140	−	
	LDTC114TM3T5G		160	350	−	
	LDTC143TM3T5G		160	350	−	
	LDTC123EM3T5G		8.0	15	−	
	LDTC143EM3T5G		15	30	−	
	LDTC143ZM3T5G		80	200	−	
	LDTC124XM3T5G		80	150	−	
	LDTC123JM3T5G		80	140	−	
	LDTC115EM3T5G		80	150	−	
	LDTC144WM3T5G		80	140	−	
	LDTC144TM3T5G		160	350	−	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)		$V_{CE(sat)}$	−	−	0.25	Vdc
(I_C = 10 mA, I_B = 5 mA)	LDTC123EM3T5G					
(I_C = 10 mA, I_B = 1 mA)	LDTC143TM3T5G/LDTC114TM3T5G/ LDTC143EM3T5G/LDTC143ZM3T5G/ LDTC124XM3T5G/LDTC144TM3T5G					
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	LDTC114EM3T5G		−	−	0.2	
	LDTC124EM3T5G		−	−	0.2	
	LDTC114YM3T5G		−	−	0.2	
	LDTC114TM3T5G		−	−	0.2	
	LDTC143TM3T5G		−	−	0.2	
	LDTC123EM3T5G		−	−	0.2	
	LDTC143EM3T5G		−	−	0.2	
	LDTC143ZM3T5G		−	−	0.2	
	LDTC124XM3T5G		−	−	0.2	
	LDTC123JM3T5G		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	LDTC144EM3T5G		−	−	0.2	
	LDTC144TM3T5G		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 5.5 V, R_L = 1.0 kΩ)	LDTC115EM3T5G		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)	LDTC144WM3T5G		−	−	0.2	

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)					
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ) LDTC143TM3T5G LDTC143ZM3T5G LDTC114TM3T5G LDTC144TM3T5G	V_{OH}	4.9	–	–	Vdc
Input Resistor LDTC114EM3T5G	R1	7.0	10	13	kΩ
LDTC124EM3T5G		15.4	22	28.6	
LDTC144EM3T5G		32.9	47	61.1	
LDTC114YM3T5G		7.0	10	13	
LDTC114TM3T5G		7.0	10	13	
LDTC143TM3T5G		3.3	4.7	6.1	
LDTC123EM3T5G		1.5	2.2	2.9	
LDTC143EM3T5G		3.3	4.7	6.1	
LDTC143ZM3T5G		3.3	4.7	6.1	
LDTC124XM3T5G		15.4	22	28.6	
LDTC123JM3T5G		1.54	2.2	2.86	
LDTC115EM3T5G		70	100	130	
LDTC144WM3T5G		32.9	47	61.1	
LDTC144TM3T5G		32.9	47	61.1	
Resistor Ratio	R_1/R_2				
LDTC114EM3T5G/LDTC124EM3T5G/ LDTC144EM3T5G/LDTC115EM3T5G		0.8	1.0	1.2	
LDTC114YM3T5G		0.17	0.21	0.25	
LDTC143TM3T5G/LDTC114TM3T5G/LDTC144TM3T5G		–	–	–	
LDTC123EM3T5G/LDTC143EM3T5G		0.8	1.0	1.2	
LDTC143ZM3T5G		0.055	0.1	0.185	
LDTC124XM3T5G		0.38	0.47	0.56	
LDTC123JM3T5G		0.038	0.047	0.056	
LDTC144WM3T5G		1.7	2.1	2.6	
Input voltage (V_{CC} = 5.0 V, I_O= 100μA) LDTC123JM3T5G	$V_{I(off)}$	–	–	0.5	V
Input voltage (V_O = 0.3 V, I_O = 5 mA) LDTC123JM3T5G	$V_{I(on)}$	1.1	–	–	V

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

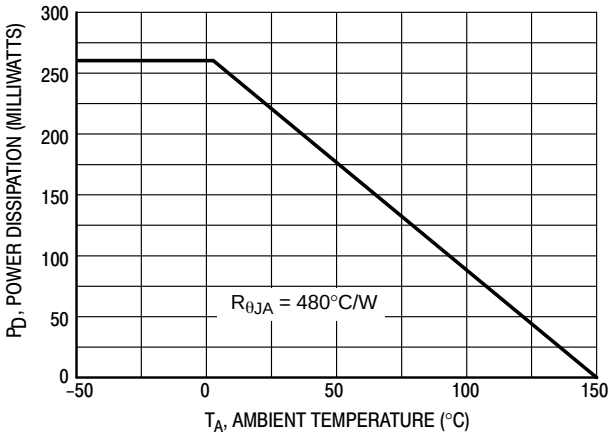


Figure 1. Derating Curve

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC114EM3T5G

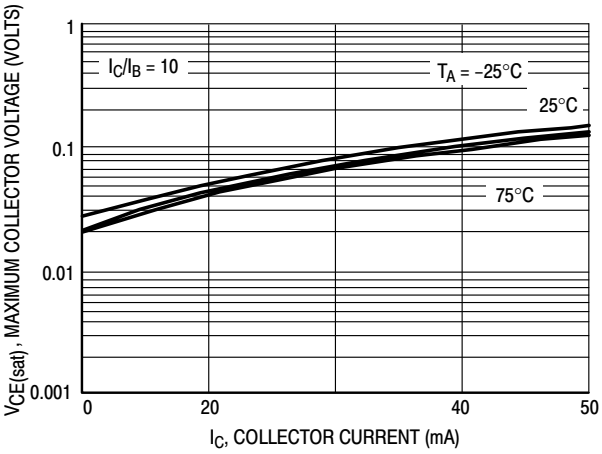


Figure 2. $V_{CE(sat)}$ versus I_C

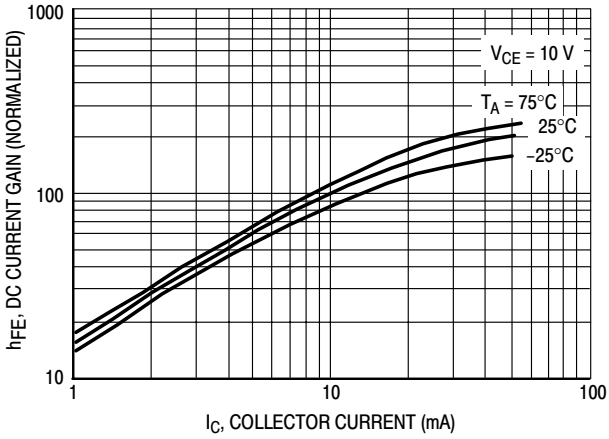


Figure 3. DC Current Gain

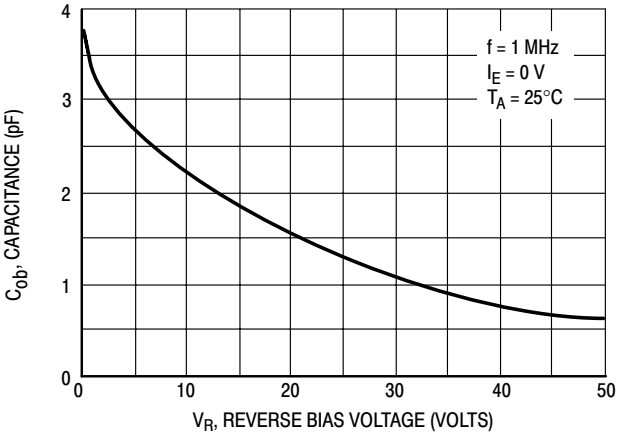


Figure 4. Output Capacitance

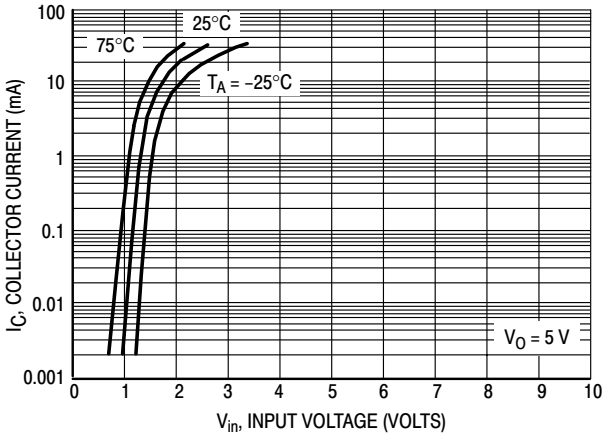


Figure 5. Output Current versus Input Voltage

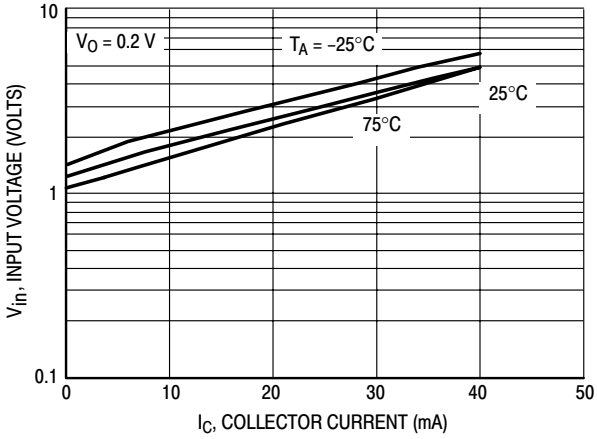


Figure 6. Input Voltage versus Output Current

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC124EM3T5G

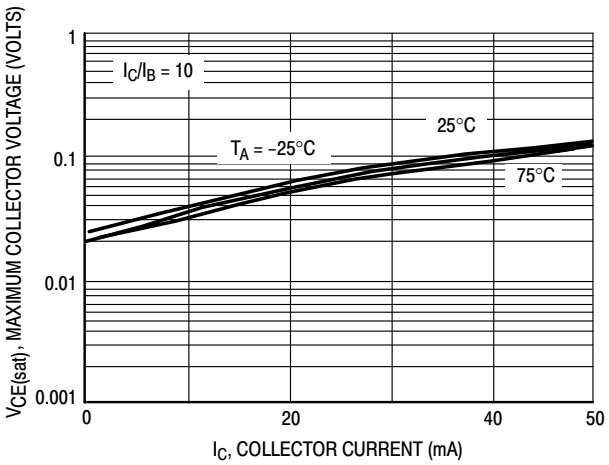


Figure 7. $V_{CE(sat)}$ versus I_C

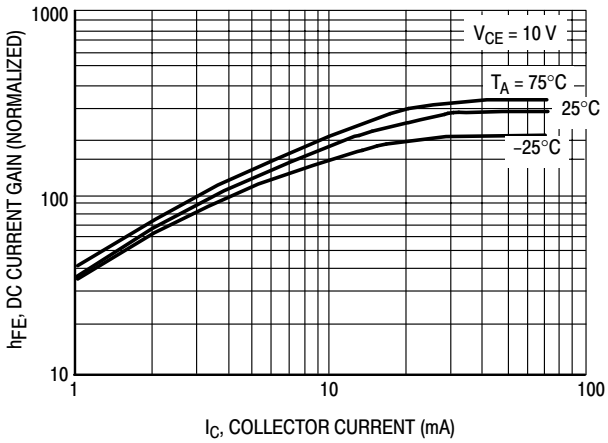


Figure 8. DC Current Gain

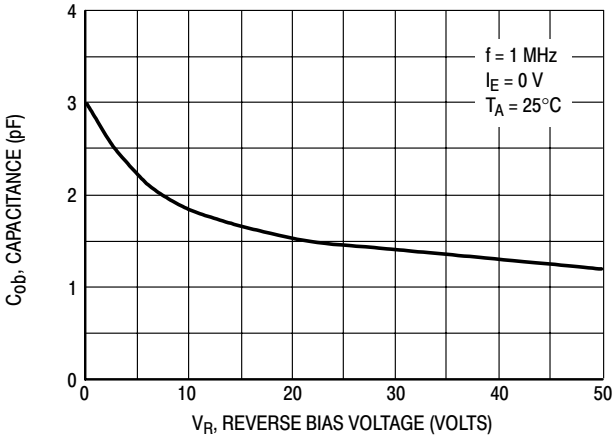


Figure 9. Output Capacitance

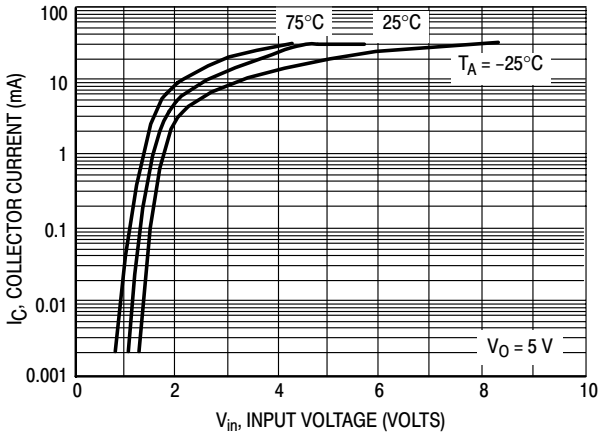


Figure 10. Output Current versus Input Voltage

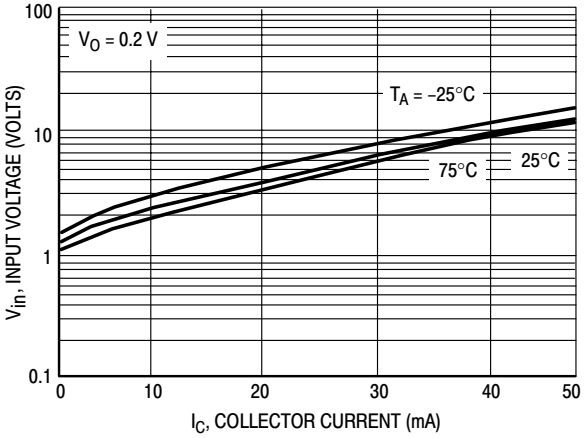


Figure 11. Input Voltage versus Output Current

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC144EM3T5G

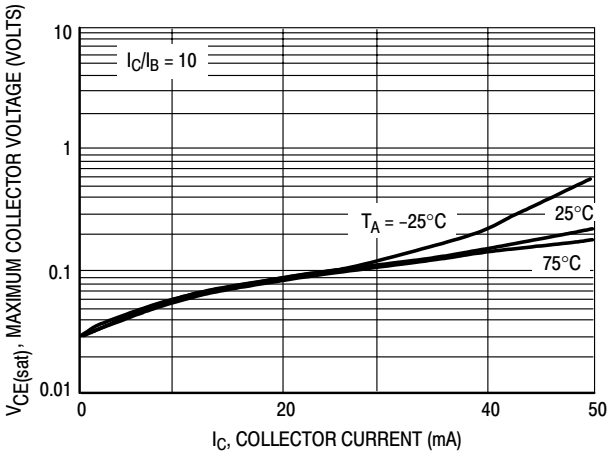


Figure 12. $V_{CE(sat)}$ versus I_C

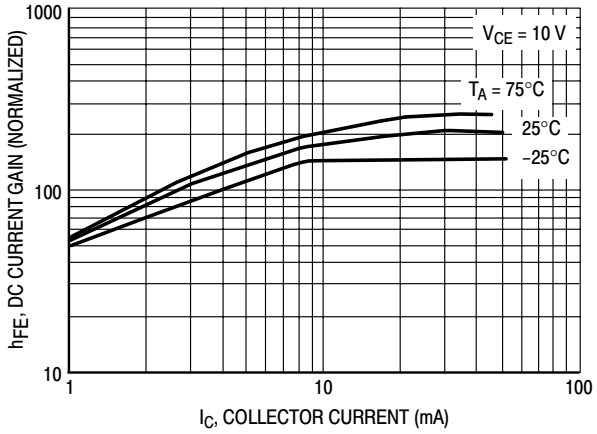


Figure 13. DC Current Gain

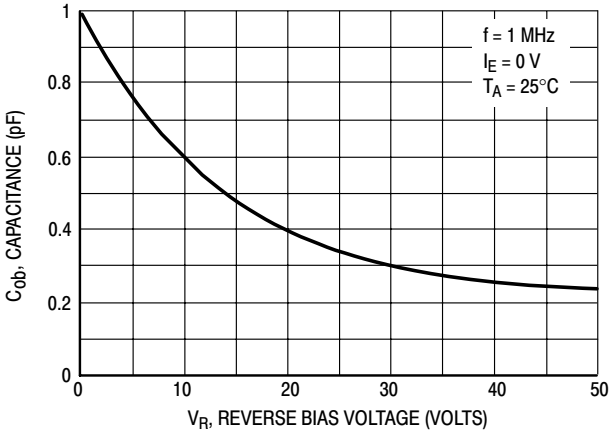


Figure 14. Output Capacitance

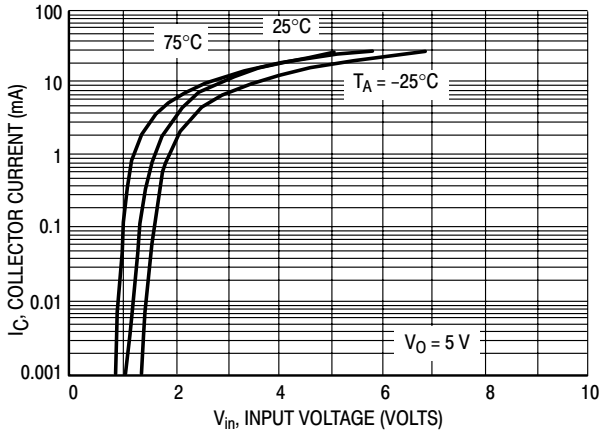


Figure 15. Output Current versus Input Voltage

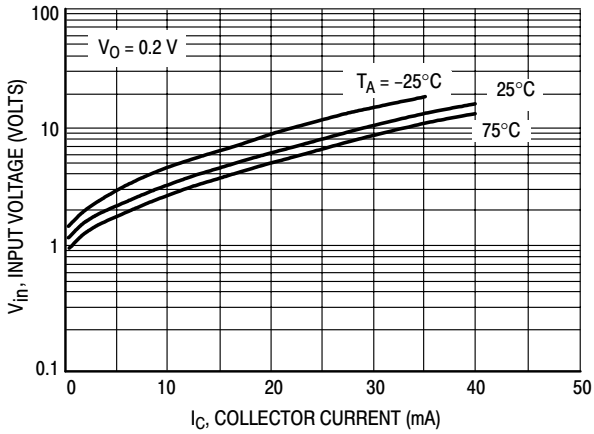


Figure 16. Input Voltage versus Output Current

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC114YM3T5G

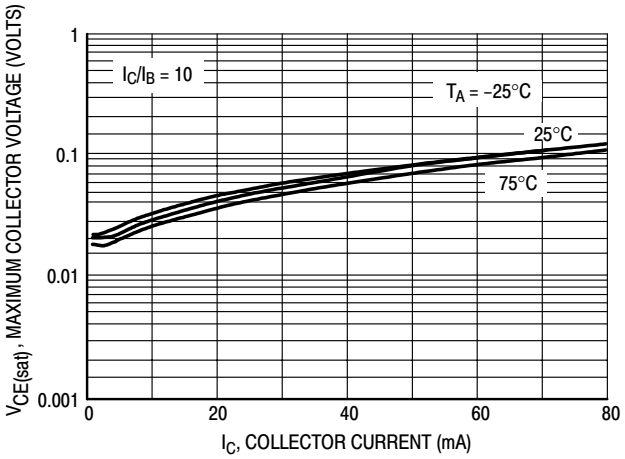


Figure 17. $V_{CE(sat)}$ versus I_C

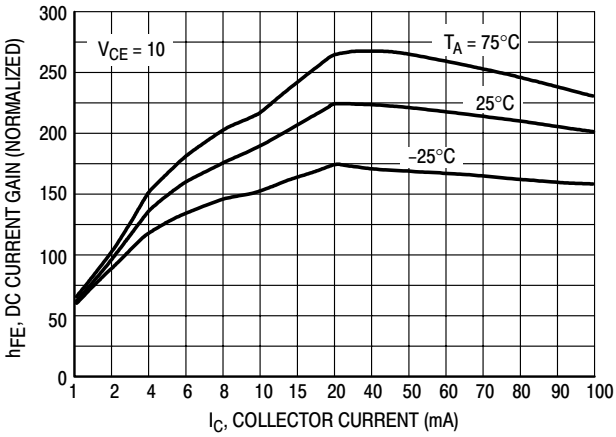


Figure 18. DC Current Gain

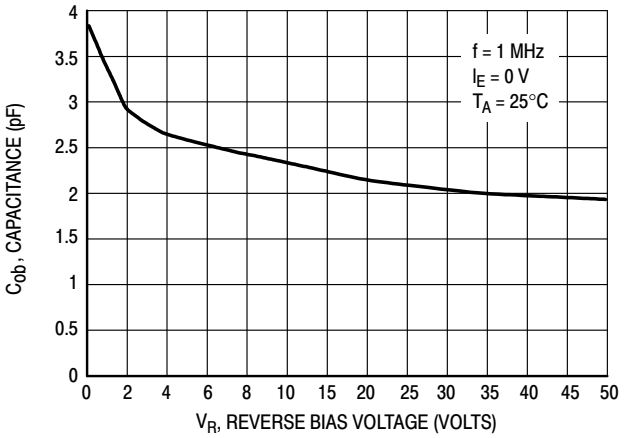


Figure 19. Output Capacitance

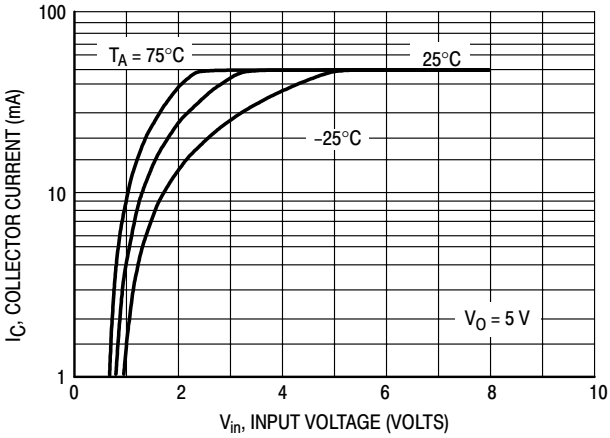


Figure 20. Output Current versus Input Voltage

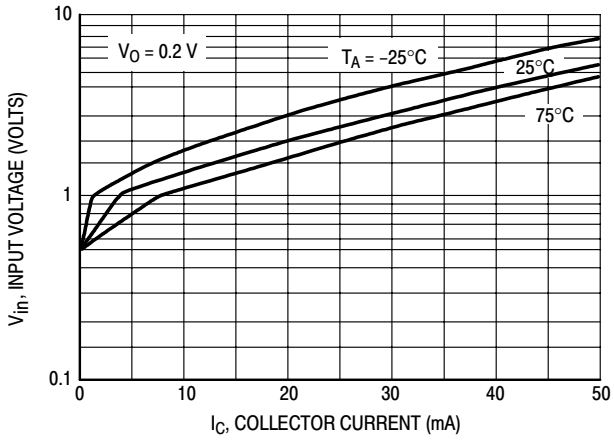


Figure 21. Input Voltage versus Output Current

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC143ZM3T5G

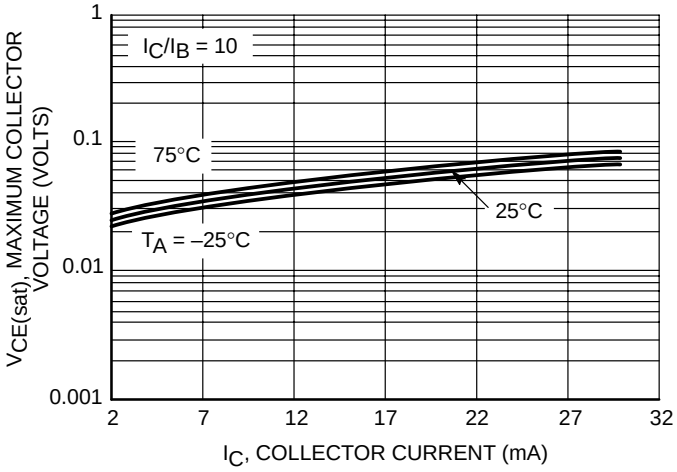


Figure 27. $V_{CE(sat)}$ vs. I_C

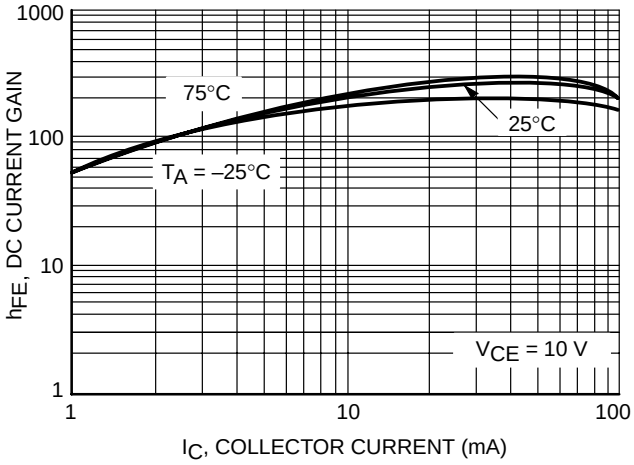


Figure 28. DC Current Gain

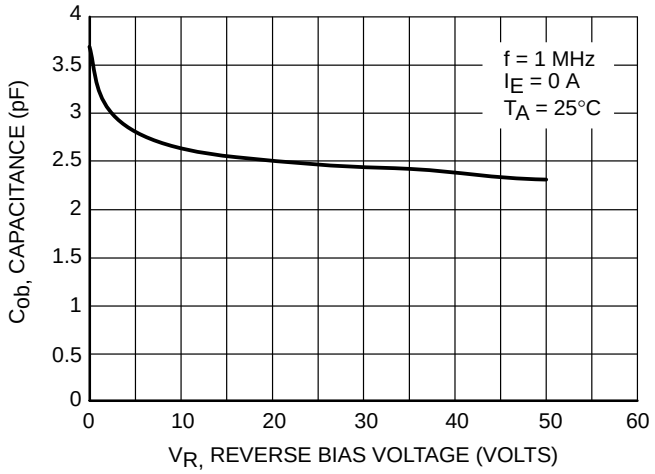


Figure 29. Output Capacitance

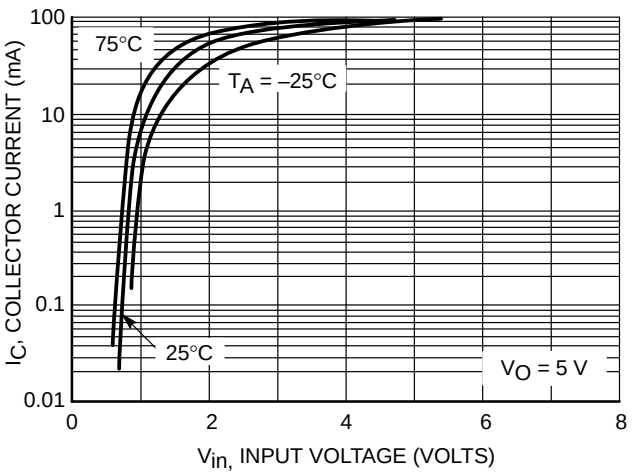


Figure 30. Output Current vs. Input Voltage

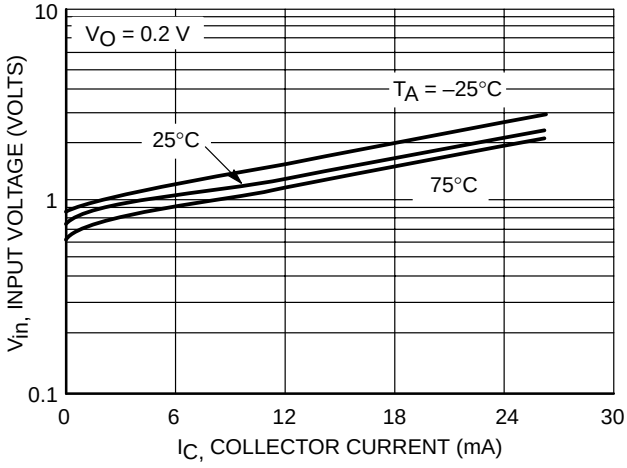


Figure 31. Input Voltage vs. Output Current

TYPICAL APPLICATIONS FOR NPN BRTs

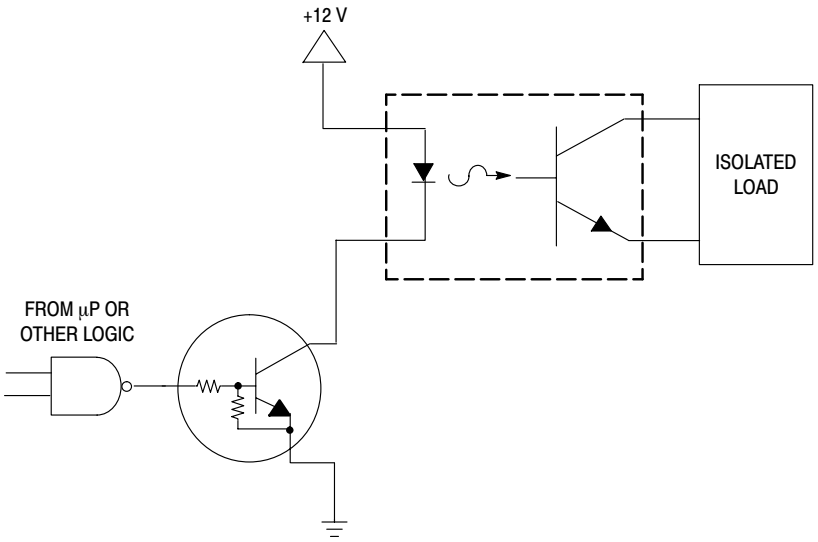


Figure 22. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

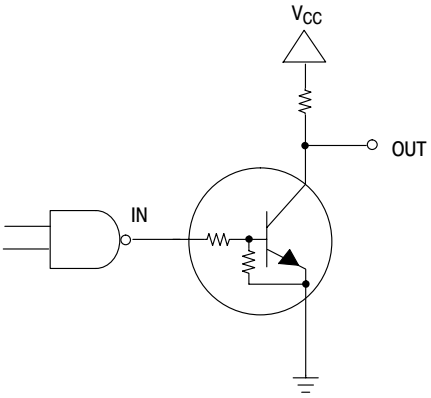


Figure 23. Open Collector Inverter: Inverts the Input Signal

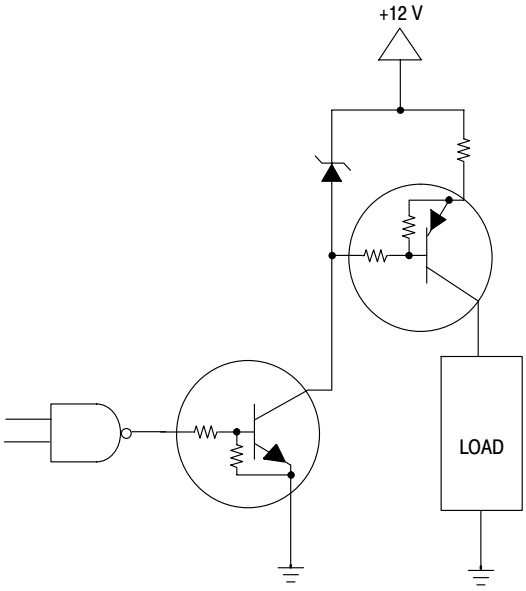
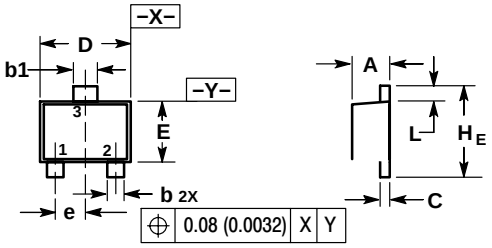


Figure 24. Inexpensive, Unregulated Current Source

LDTC114EM3T5G SERIES,S-LDTC114EM3T5G SERIES

PACKAGE DIMENSIONS

SOT−723

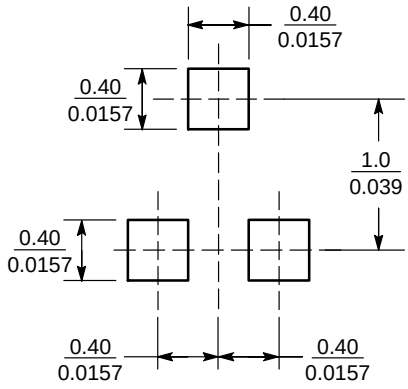


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PIN 1. BASE
2. EMITTER
3. COLLECTOR

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
b	0.15	0.20	0.27	0.0059	0.0079	0.0106
b1	0.25	0.3	0.35	0.010	0.012	0.014
C	0.07	0.12	0.17	0.0028	0.0047	0.0067
D	1.15	1.20	1.25	0.045	0.047	0.049
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.40 BSC			0.016 BSC		
H E	1.15	1.20	1.25	0.045	0.047	0.049
L	0.15	0.20	0.25	0.0059	0.0079	0.0098

SOLDERING FOOTPRINT



(mm / inches)

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