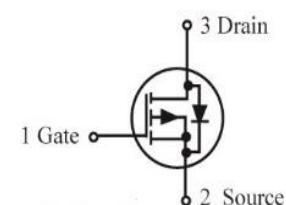
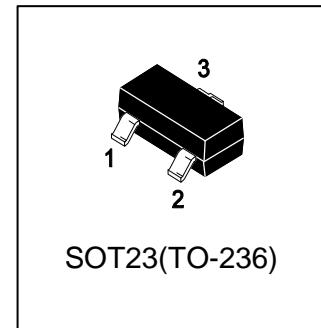


S-LP3407LT1G

30V P-Channel Enhancement-Mode MOSFET

1. FEATURES

- VDS = -30V
- ID=-4.1A @ VGS = -10V
- RDS(ON) ≤ 70mΩ(VGS = -10V)
- RDS(ON) ≤ 100mΩ(VGS = -4.5V)
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



2. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
S-LP3407LT1G	A07	3000/Tape&Reel
S-LP3407LT3G	A07	10000/Tape&Reel

3. MAXIMUM RATINGS($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	VDSS	-30	V
Gate-to-Source Voltage	VGS	±20	V
Continuous Drain Current Ta=25°C	ID	-3.5	A
Ta=70°C	ID	-2.5	
Pulsed Drain Current (Note 3)	IDM	-15	
Power Dissipation (Note 2) Ta=25°C	PD	1.1	W
Ta=70°C	PD	0.6	
Junction and Storage Temperature Range	Tj,Tstg	-55~+150	°C

4. THERMAL CHARACTERISTICS

Parameter	Symbol	Typ.	Max	Unit
Thermal Resistance, Junction-to-Ambient (Note 1)	R _{θJA}	70	90	°C/W
Steady State	R _{θJA}	100	125	
Maximum Junction-to-Lead	R _{θJL}	63	80	

1.The value of R_{θJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

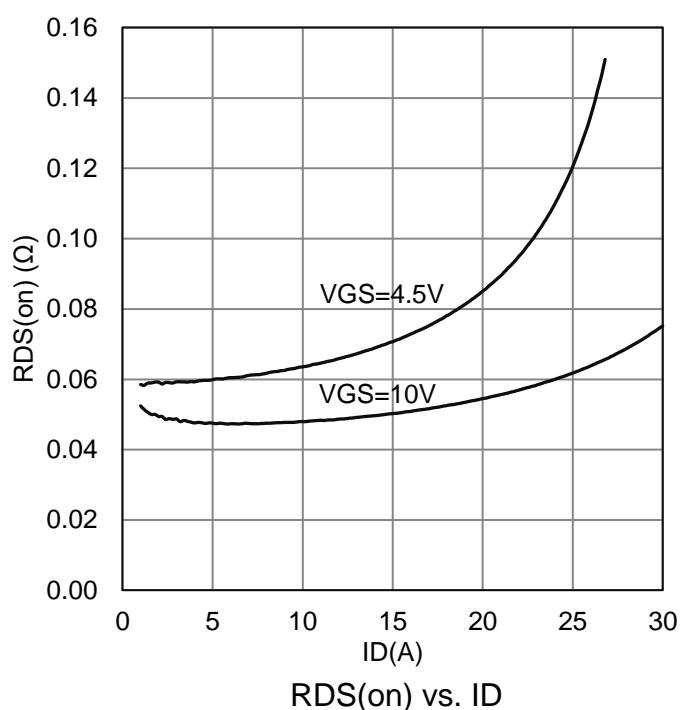
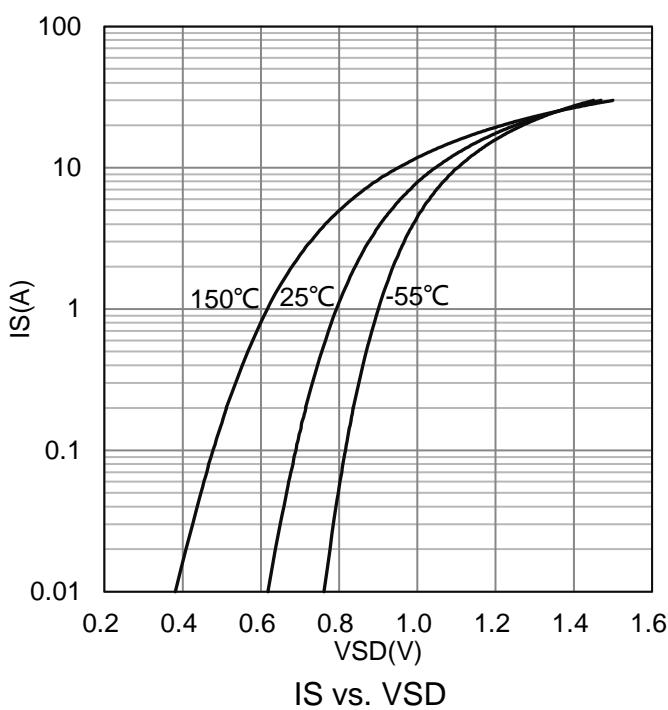
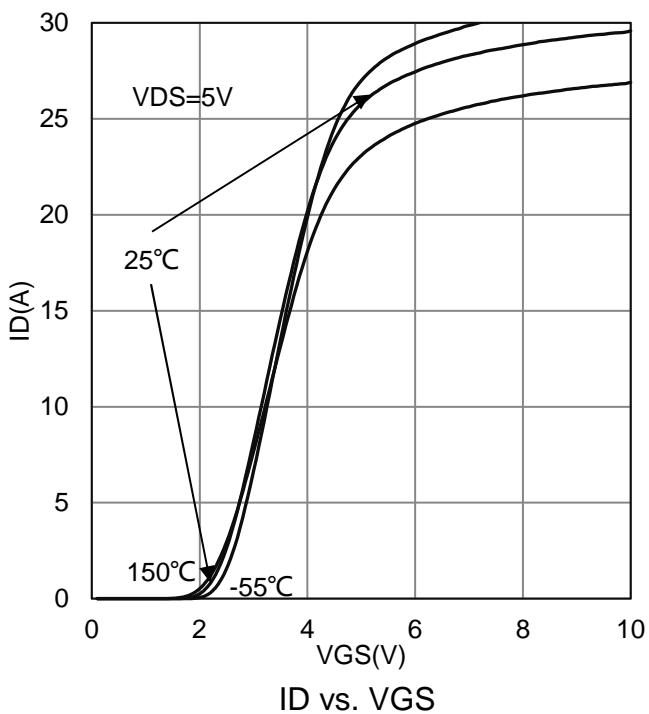
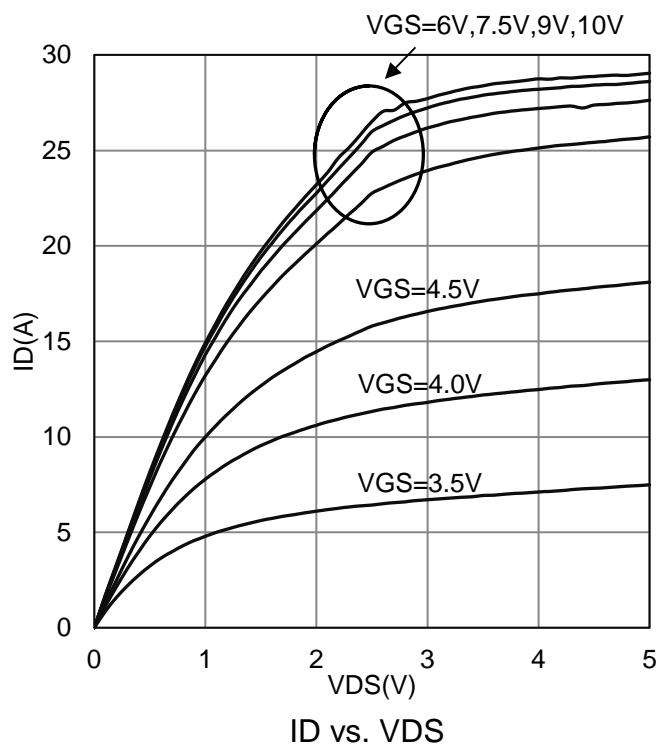
2.Repetitive rating, pulse width limited by junction temperature.

3.The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

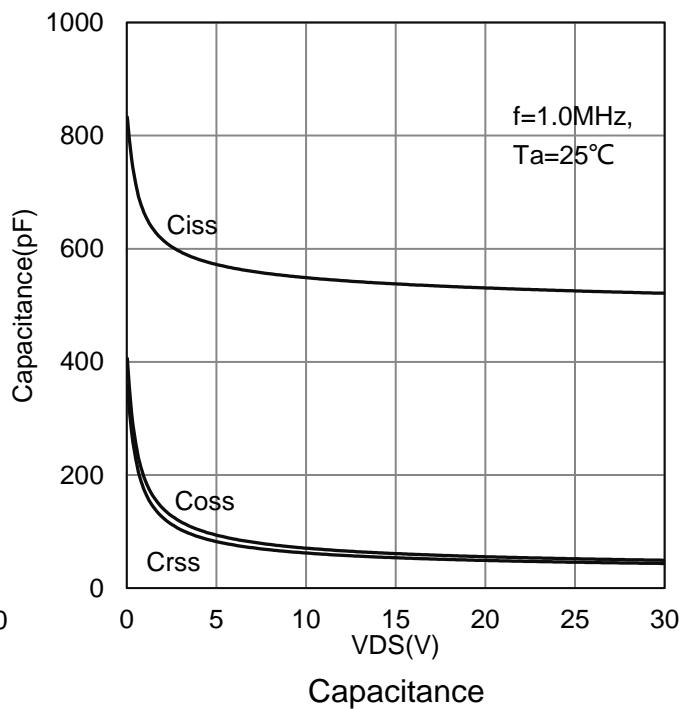
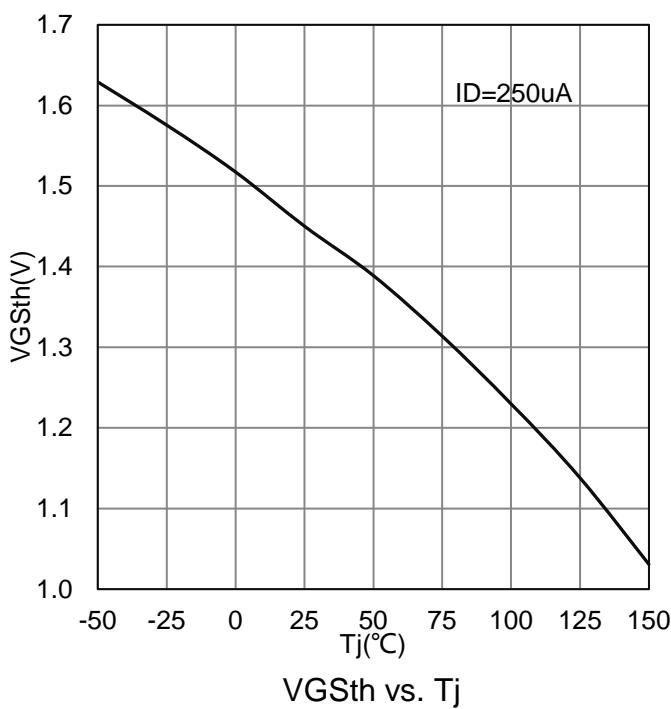
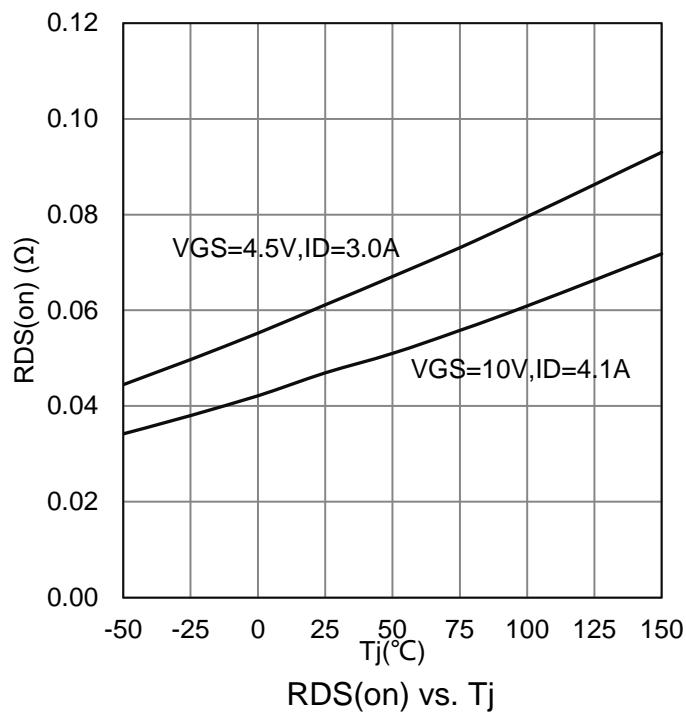
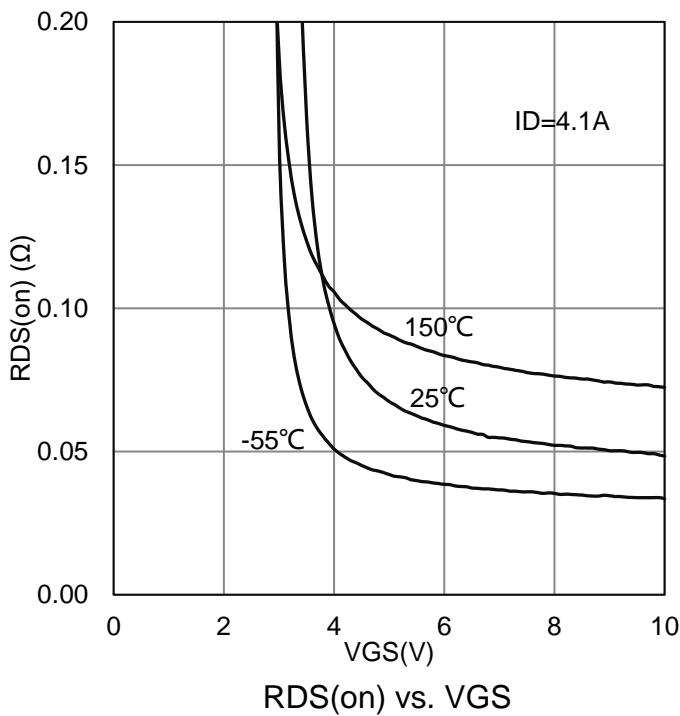
5. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Static					
Drain–Source Breakdown Voltage (VGS = 0, ID = -250µA)	VBRDSS	-30	-	-	V
Zero Gate Voltage Drain Current (VGS = 0, VDS = -24 V) (VGS = 0, VDS = -24 V, TJ =55°C)	IDSS	-	-	-1 -5	µA
Gate Leakage Current (VDS =0V, VGS =±20V)	IGSS	-	-	±100	nA
Gate Threshold Voltage (VDS = VGS, ID = -250µA)	VGS(th)	-1	-1.4	-2.1	V
Static Drain–Source On–State Resistance (VGS =-10V, ID =-4.1A) (VGS =-10V, ID =-4.1A, TJ =125°C) (VGS =-4.5V, ID =-3A)	RDS(on)	-	52 65 70	70 95 100	mΩ
Forward Voltage (VGS = 0 V, IS = -1A)	VSD	-	-0.7	-1	V
Dynamic					
Input Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -15 V)	Ciss	-	521	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -15 V)	Coss	-	61	-	
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -15 V)	Crss	-	54	-	
Gate resistance (VGS =0V, VDS =0V, f=1MHz)	Rg	-	10	-	Ω
Total Gate Charge	(VDS =-15V, ID =-4A)	Qg(10V)	-	11	nC
Total Gate Charge		Qg(4.5V)	-	5.7	
Gate-Source Charge		Qgs	-	1.24	
Gate-Drain Charge		Qgd	-	2.5	
Turn-On Delay Time	(VDS = -15V, RL= 3.6 Ω,VGS = -10V,RG = 3.1Ω)	td(on)	-	3.6	ns
Rise Time		tr	-	9.8	
Turn-Off Delay Time		td(off)	-	19.2	
Fall Time		tf	-	6.7	
Body Diode Reverse Recovery Time (IF =-4A, dI/dt=100A/µs)	trr	-	11	-	
Body Diode Reverse Recovery Charge (IF =-4A, dI/dt=100A/µs)	Qrr	-	5.3	-	nC

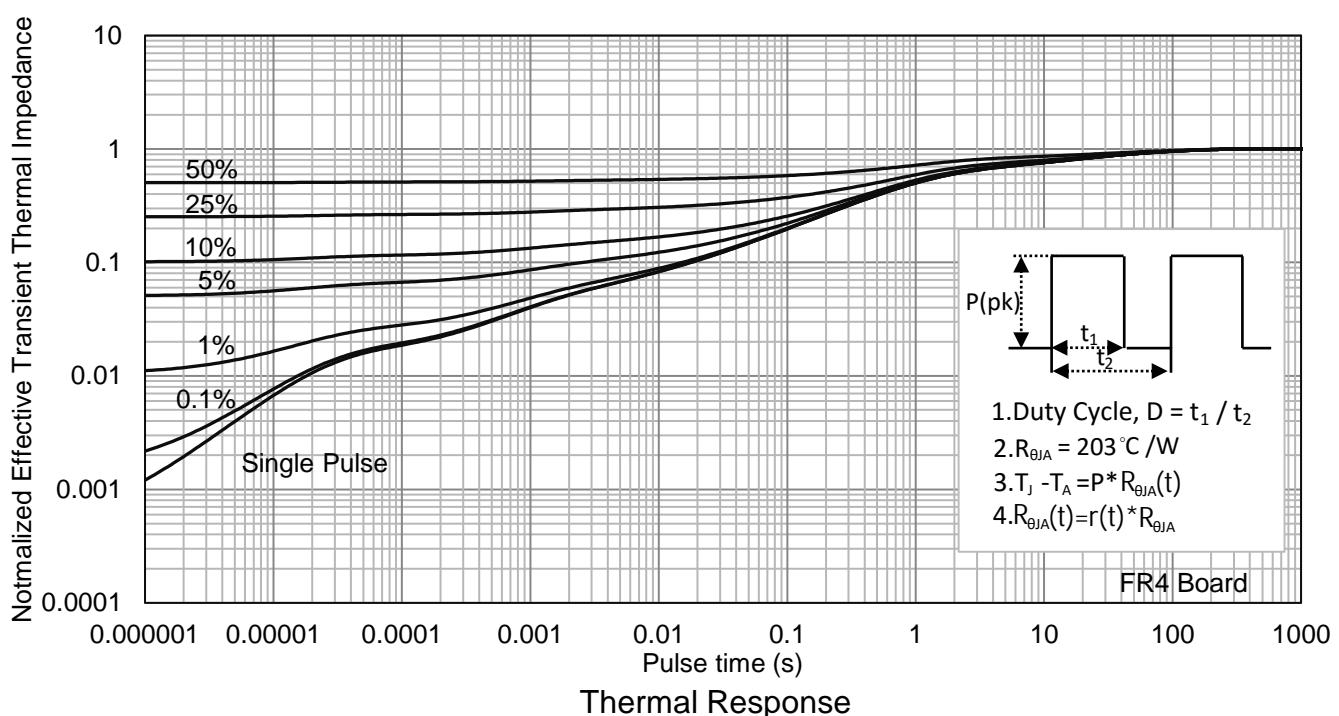
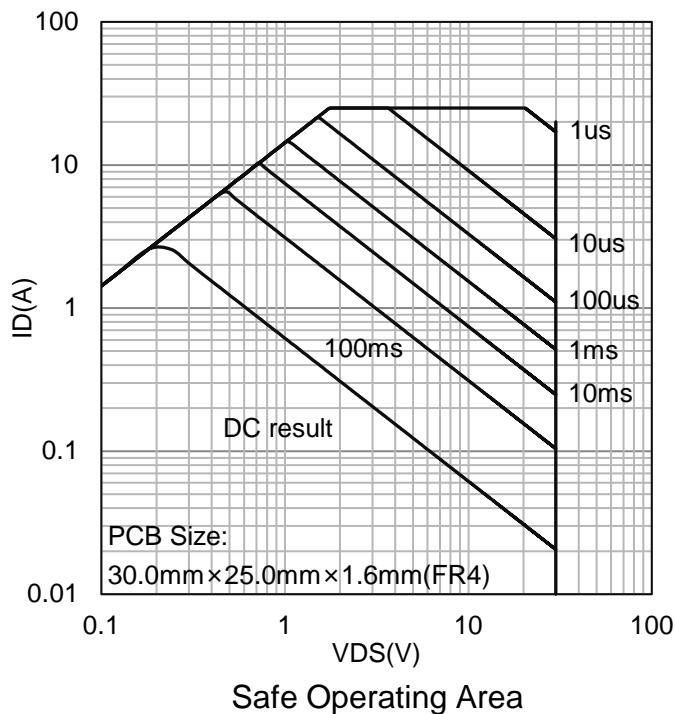
6. ELECTRICAL CHARACTERISTICS CURVES



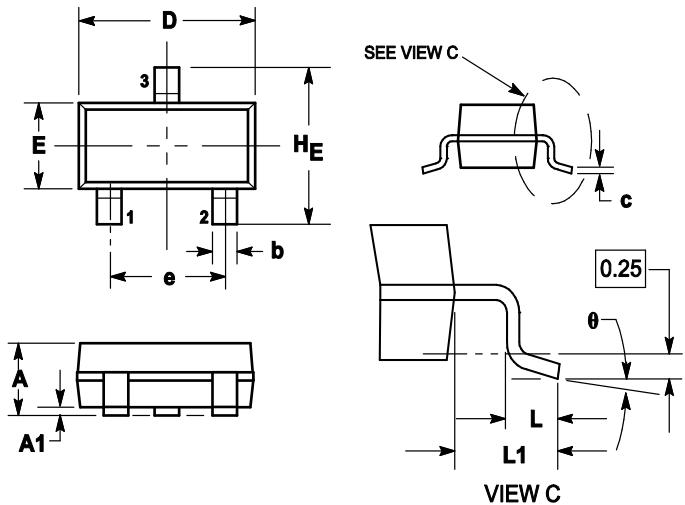
6. ELECTRICAL CHARACTERISTICS CURVES(Con.)



6.ELECTRICAL CHARACTERISTICS CURVES(Con.)



7. OUTLINE AND DIMENSIONS

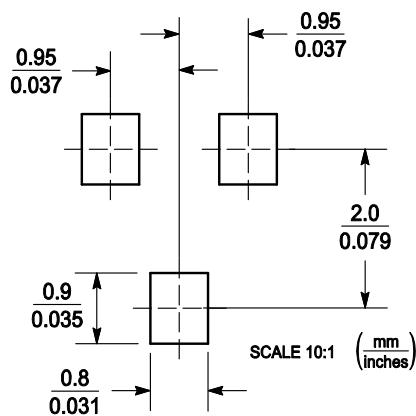


Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

8. SOLDERING FOOTPRINT





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