

- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

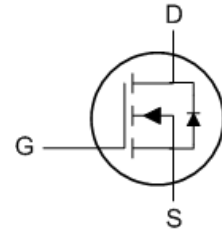
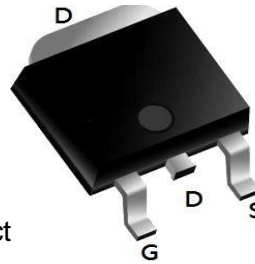
Product Summary

BVDSS	RDSON	ID
100V	85 mΩ	15A

Description

The IRLR120NTRPBF is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The IRLR120NTRPBF meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	15	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	7.7	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	3	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	2.4	A
I _{DM}	Pulsed Drain Current ²	24	A
EAS	Single Pulse Avalanche Energy ³	6.1	mJ
I _{AS}	Avalanche Current	11	A
P _D @T _C =25°C	Total Power Dissipation ³	34.7	W
P _D @T _A =25°C	Total Power Dissipation ³	2	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	3.6	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.098	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =10A	---	85	112	mΩ
		V _{GS} =4.5V, I _D =8A	---	105	120	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	---	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4.57	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =80V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =80V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =10A	---	13	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2	---	Ω
Q _g	Total Gate Charge (10V)	V _{DS} =80V, V _{GS} =10V, I _D =10A	---	26.2	---	nC
Q _{gs}	Gate-Source Charge		---	4.6	---	
Q _{gd}	Gate-Drain Charge		---	5.1	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =50V, V _{GS} =10V, R _G =3.3Ω I _D =10A	---	4.2	---	ns
T _r	Rise Time		---	8.2	---	
T _{d(off)}	Turn-Off Delay Time		---	35.6	---	
T _f	Fall Time		---	9.6	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1535	---	pF
C _{oss}	Output Capacitance		---	60	---	
C _{rss}	Reverse Transfer Capacitance		---	37	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	15	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	24	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =10A, dI/dt=100A/μs, T _J =25°C	---	37	---	nS
Q _{rr}	Reverse Recovery Charge		---	27.3	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=11A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

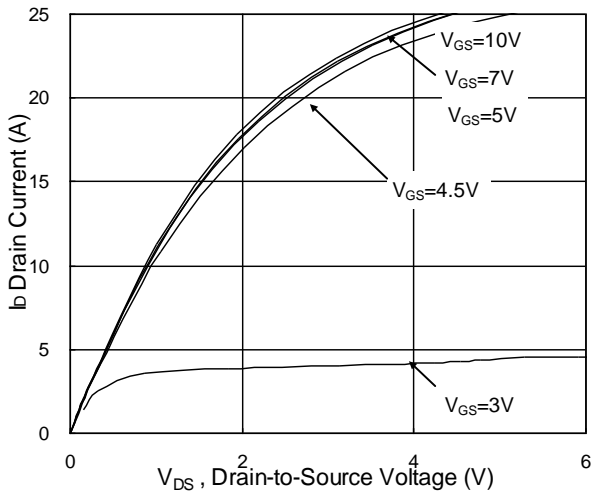


Fig.1 Typical Output Characteristics

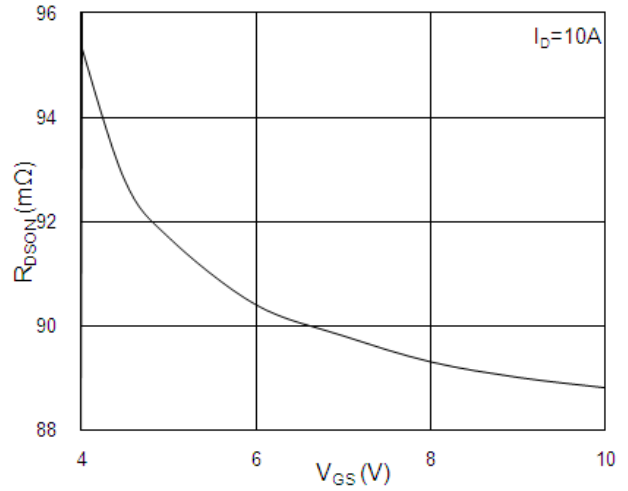


Fig.2 On-Resistance vs. Gate-Source

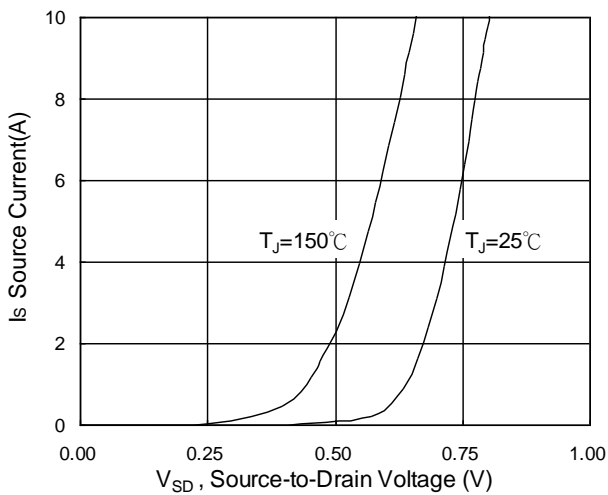


Fig.3 Forward Characteristics Of Reverse

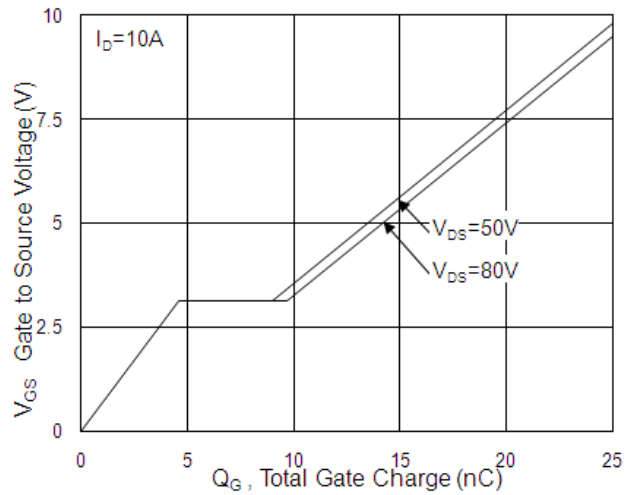


Fig.4 Gate-Charge Characteristics

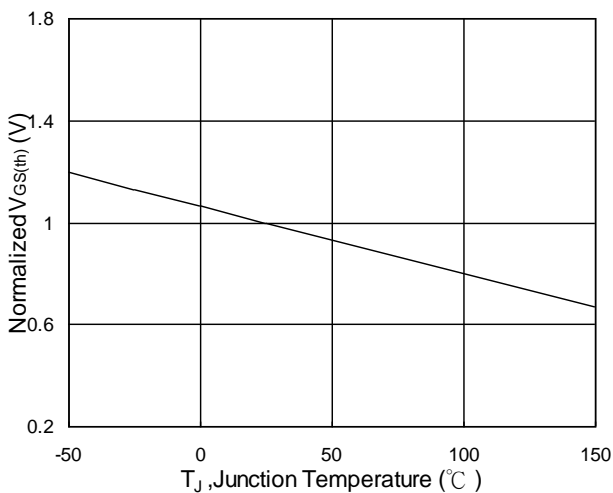


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

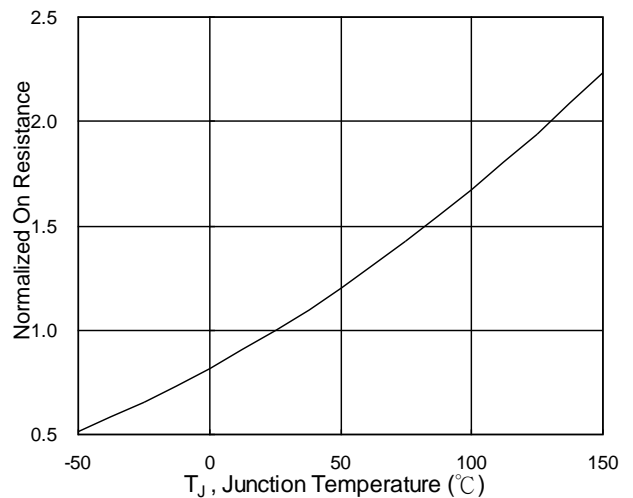


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

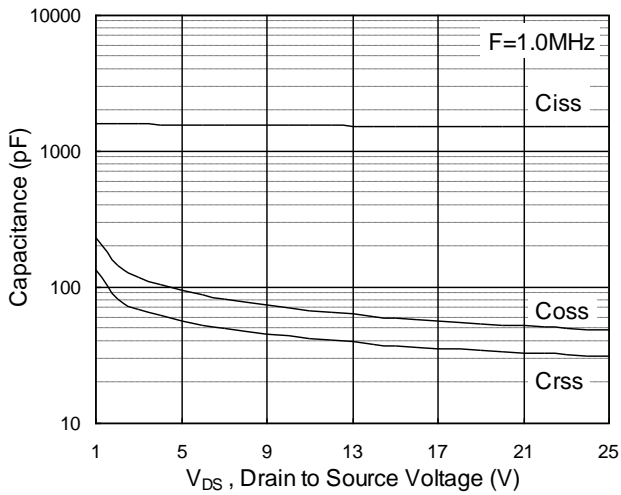


Fig.7 Capacitance

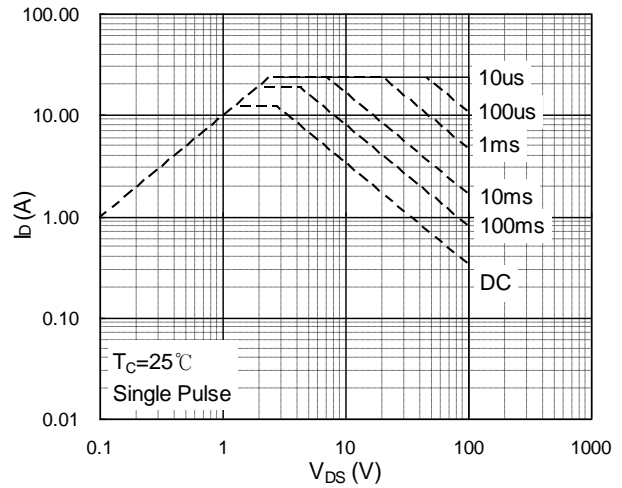


Fig.8 Safe Operating Area

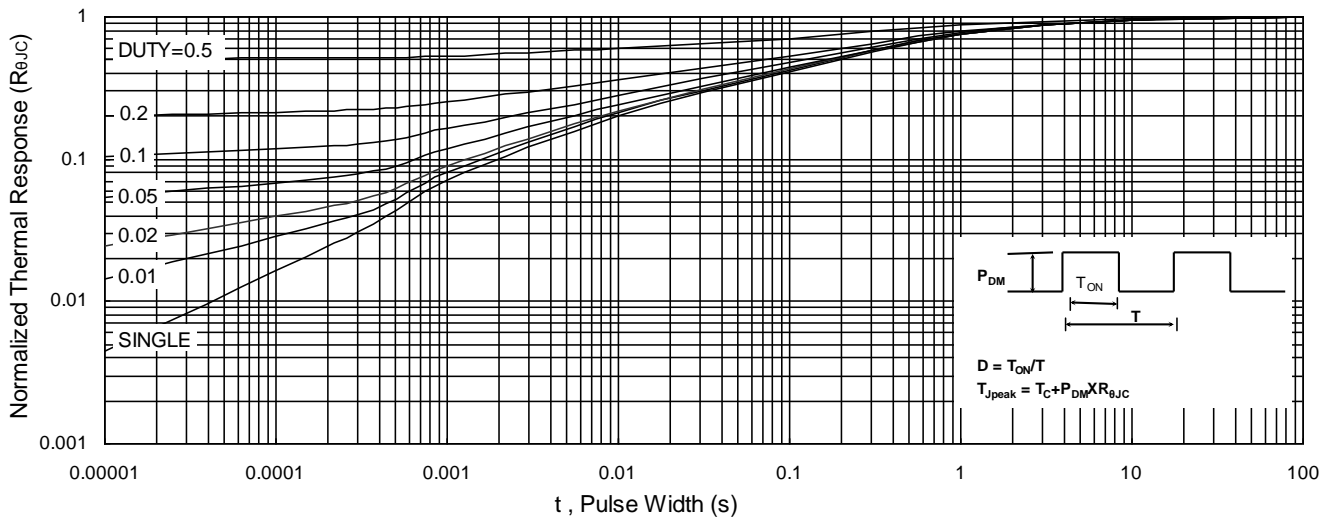


Fig.9 Normalized Maximum Transient Thermal Impedance

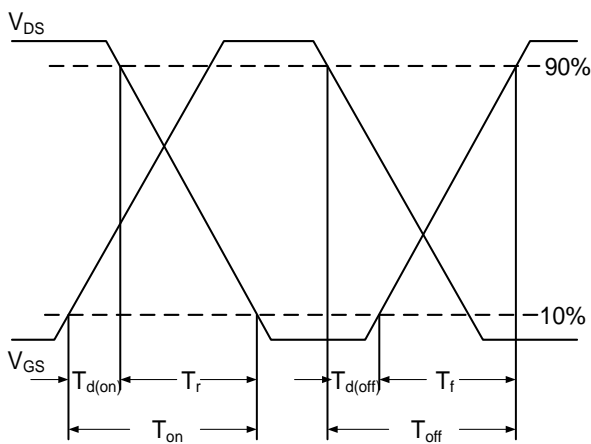


Fig.10 Switching Time Waveform

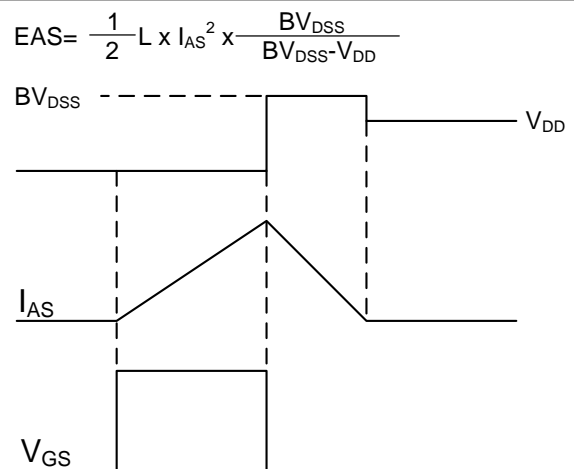


Fig.11 Unclamped Inductive Switching Waveform