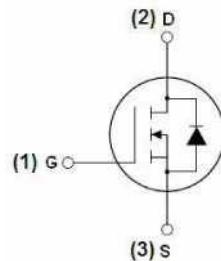




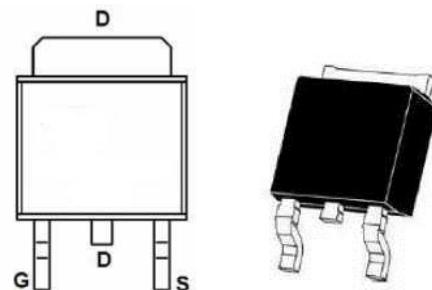
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60V (V_{DS}) / 25A (I_D) N-Channel Enhancement-Mode MOSFET



Schematic diagram



TO-252

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous $T_c = 100^\circ\text{C}$	I_D	25	A
		14	
Drain Current -Pulsed ^a	I_{DM}	60	A
Power Dissipation	P_D	45	W
Derating factor		0.3	W/ °C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C
Single pulse avalanche energy (Note 5)	EAS	72	mJ
Thermal Resistance, Junction-to-Ambient ¹ (Note2)	$R_{\theta JA}$	3.3	°C/W



Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	60	—	—	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	—	—	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	—	—	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.2	1.6	2.5	V
Static Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =10V, I _D =4.5 A	—	27	32	mΩ
Forward Transconductance	g _{fS}	V _{DS} =5V, I _D =5A	11	—	—	S
Diode Forward Voltage (Note3)	V _{SD}	V _{GS} =0V,I _S =20A	—	—	1.2	V
Continuous Source Current (Note2)	I _S		—	—	20	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, IF =20A di/dt = 100A/μs(Note3)	—	35	—	nS
Reverse Recovery Charge	Q _{rr}		—	53	—	nC
Input Capacitance	C _{iss}	V _{GS} =0V,V _{DS} =30V, f=1.0MHz	—	1500	—	pF
Output Capacitance	C _{oss}		—	60	—	
Reverse Transfer Capacitance	C _{rss}		—	25	—	
Total Gate Charge	Q _g	V _{GS} =10V,V _{DS} =30V, I _D =4.5A	—	47	—	nC
Gate-Source Charge	Q _{gs}		—	6	—	
Gate-Drain Charge	Q _{gd}		—	14	—	
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, R _L =6.7Ω R _G =3Ω, V _{GS} =10V	—	5	—	ns
Turn-on Rise Time	t _r		—	2.6	—	
Turn-off Delay Time	t _{d(off)}		—	16.1	—	
Turn-off Fall Time	t _f		—	2.3	—	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

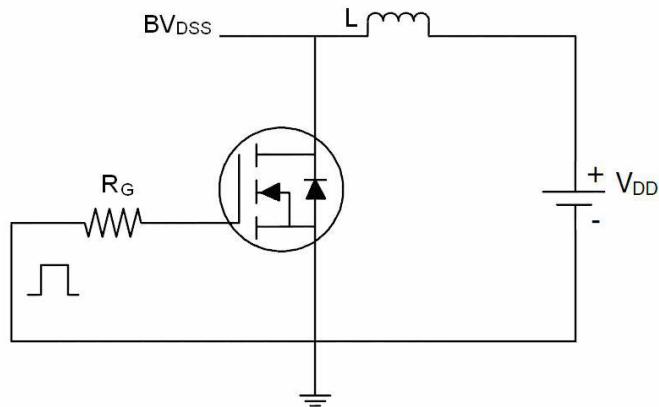
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Pulse Test: Pulse Width ≤ 300μ ≤ 10 sec .
3. Surface Mounted on FR4 Board,s,t Duty Cycle ≤ 2%.
- 4.Guaranteed by design, not subject to production
5. EAS condition:Tj=25 ,VDD=30V,VG=10V,L=0.5mH,Rg=25Ω

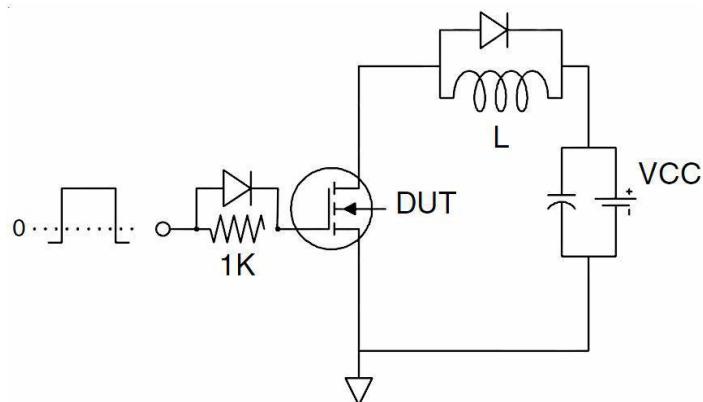


Test Circuit

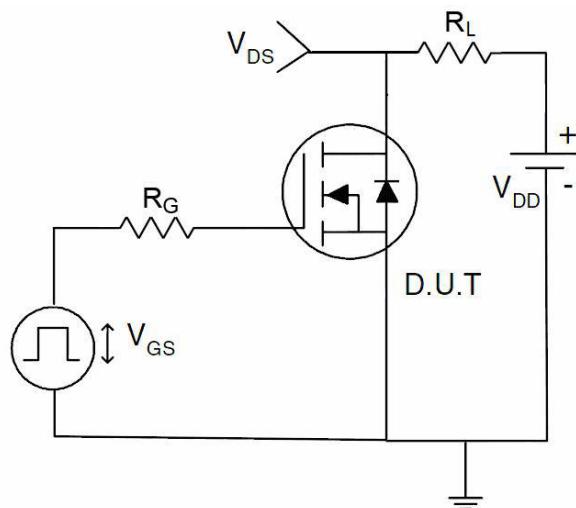
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit

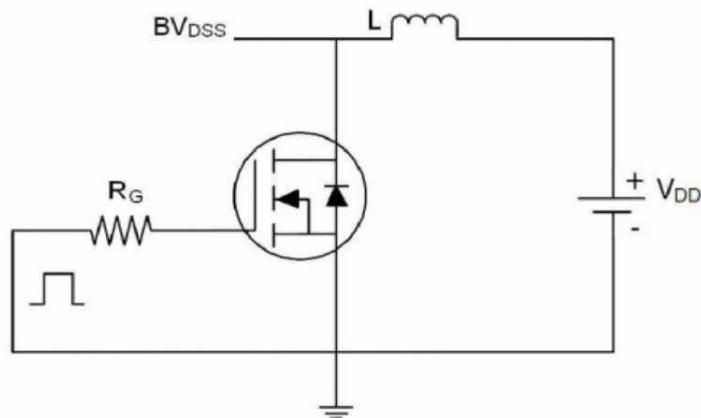




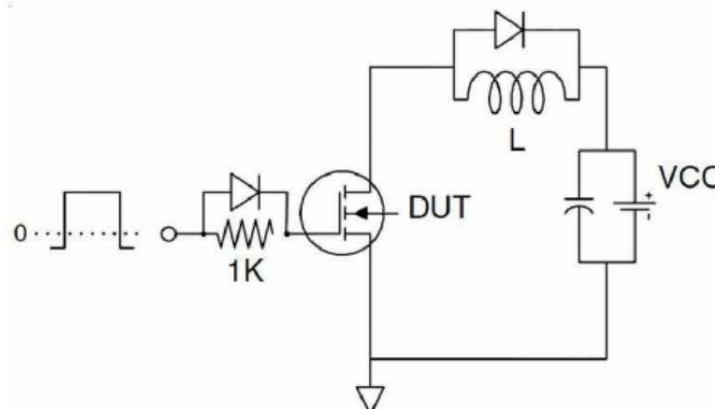
Typical Electrical and Thermal Characteristics (Curves)

Test Circuit

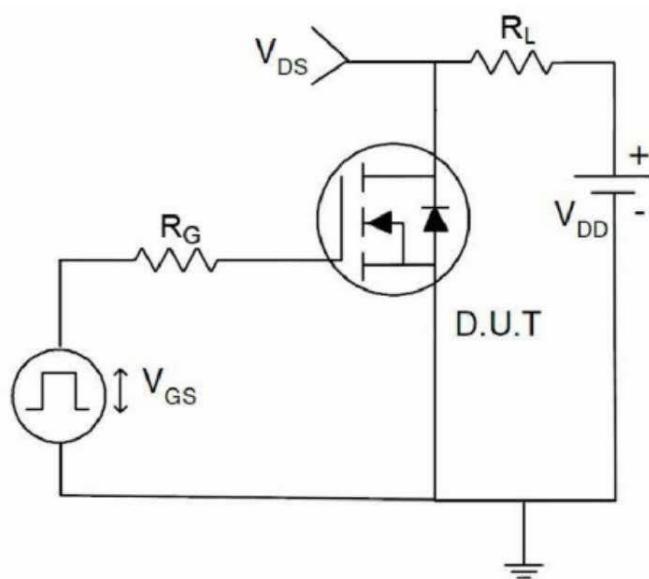
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit





60V (V_{DS}) / 30A (I_D) N-Channel Enhancement-Mode MOSFET

Typical Electrical and Thermal Characteristics (Curves)

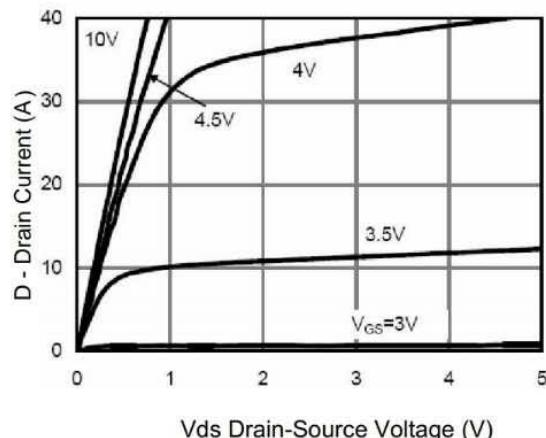


Figure 1 Output Characteristics

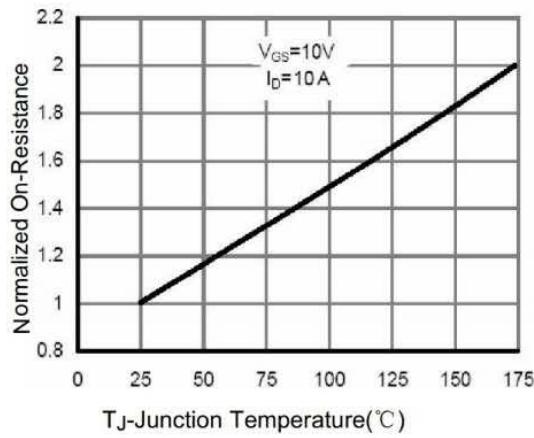


Figure 4 Rdson-Junction Temperature

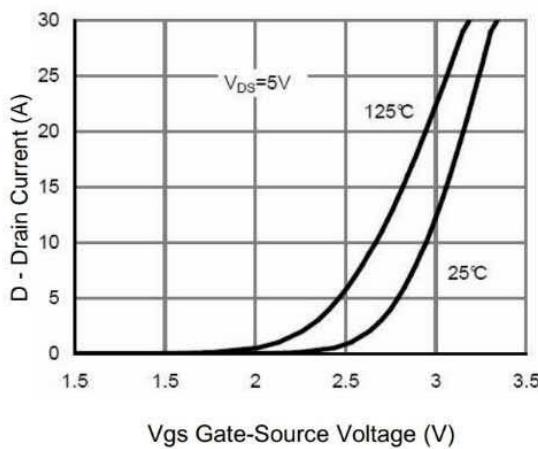


Figure 2 Transfer Characteristics

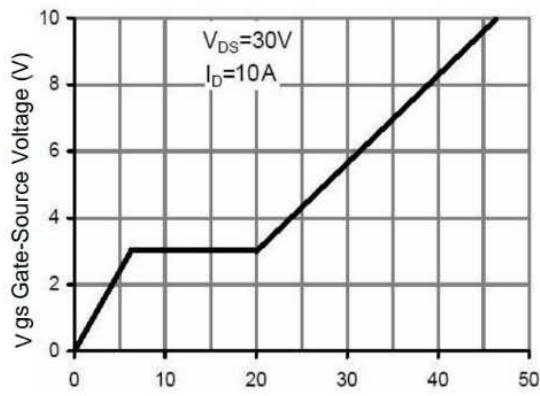


Figure 5 Gate Charge

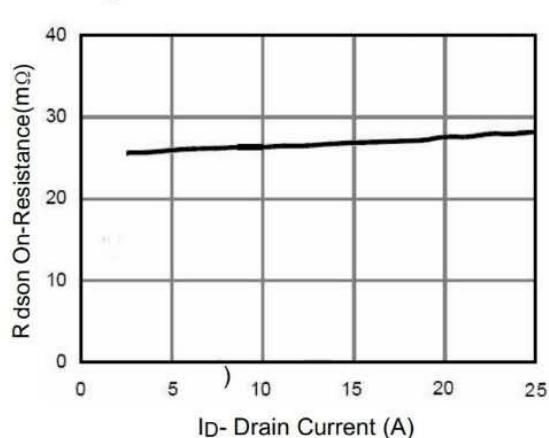


Figure 3 Rdson- Drain Current

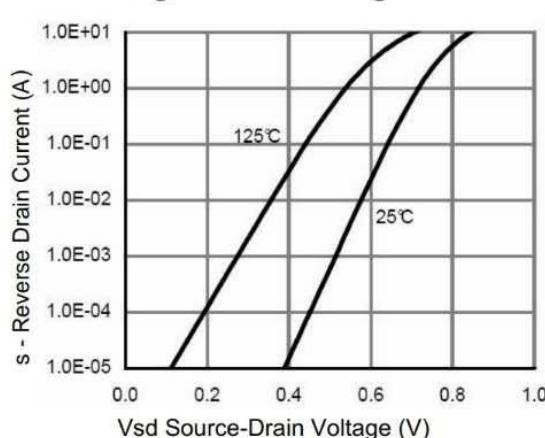


Figure 6 Source- Drain Diode Forward



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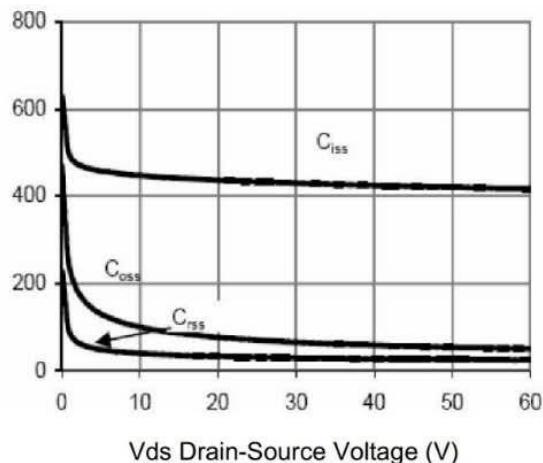


Figure 7 Capacitance vs V_{DS}

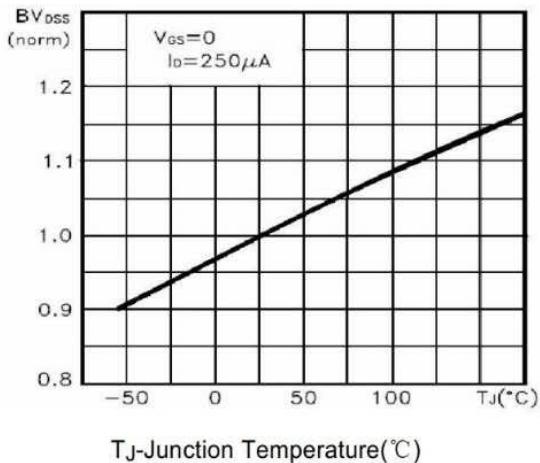


Figure 9 BV_{DSS} vs Junction Temperature

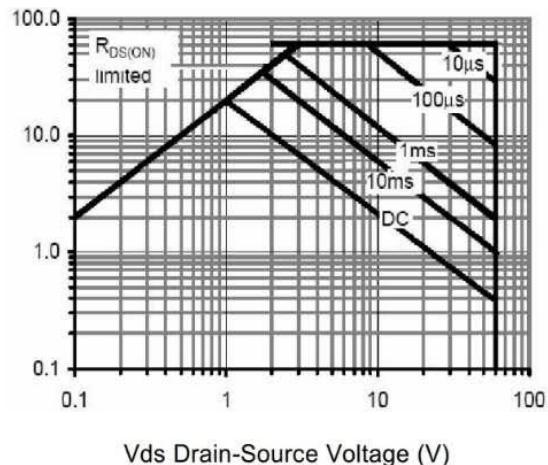


Figure 8 Safe Operation Area

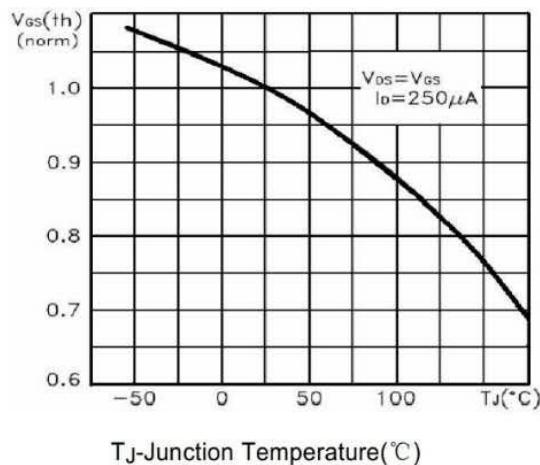


Figure 10 $V_{GS(th)}$ vs Junction Temperature

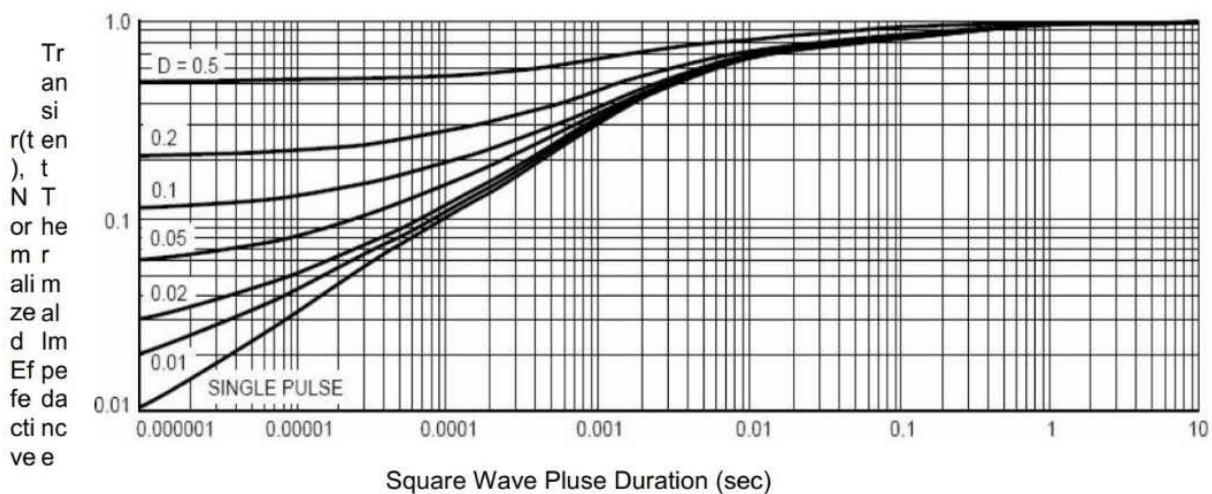


Figure 11 Normalized Maximum Transient Thermal Impedance

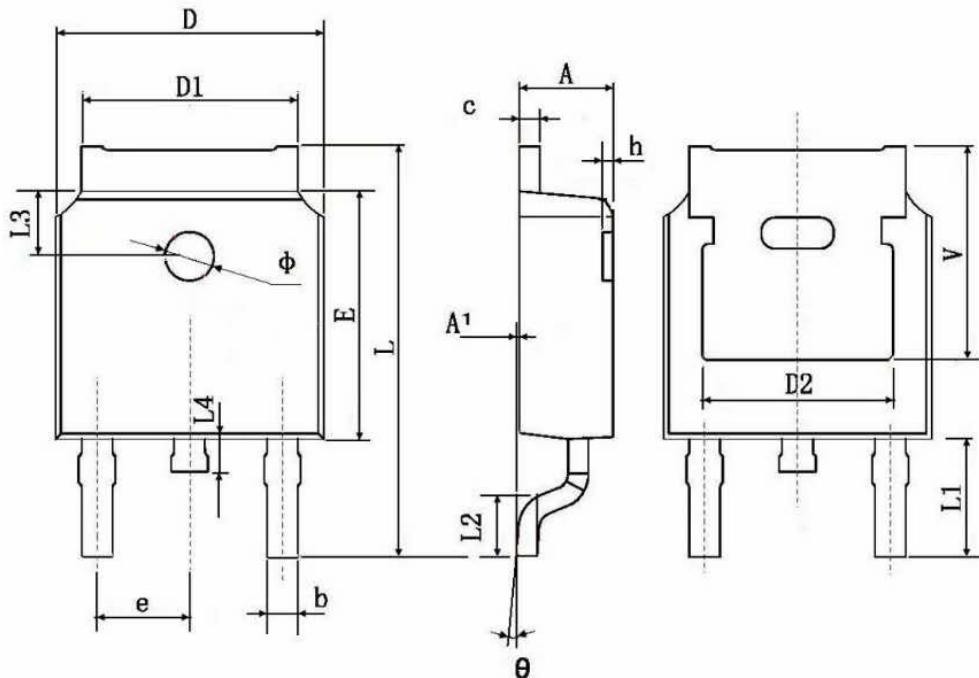


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TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	