YTY UNiCORE

Memory Module Data Sheet

DDR4-2666(CL19) 288-Pin U-DIMM 16GB Based on 8Gb ChangXin M-Die (2048M x 64-bit)

Version 1-0

Revision History

Version	Changes	Page	Date
V1-0	Formal release	-	2021/02/03

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General Description：

GD4UD26N16C4C000 is DDR4-2666(CL19)-19-19 SDRAM memory module. The SPD is programmed to JEDEC standard latency 2666Mbps timing of 19-19-19 at 1.2V. The module is composed of 8Gb CMOS DDR4 SDRAMs in FBGA package and one 4Kbit EEPROM in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features：

- Power supply (Normal)
  VDD & VDDQ = 1.2V +5% / -5%
  VPP = 2.5V +10% / -5%
  VDDSPD = 2.5V (2.25V to 3.6V)
- Burst Length (BL):8 and 4 with Burst Chop(BC)
- Bi-directional, differential data strobe (DQS and /DQS)
- Differential clock input operation
- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture; two data transfers per clock cycle
- 16 internal banks; 4 groups of 4 banks each
- Internal self calibration through ZQ pin (RZQ:240 ohm±1%)
- Low-power auto refresh (LPASR)
- Tc of 0°C to 95°C
  - 64ms, 8192-cycle refresh at 0°C to 85°C
  - 32ms, 8192-cycle refresh at 85°C to 95°C
- 8-bit pre-fetch architecture
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals.
- Data bus inversion for data bus(DBI)
- Data bus Write CRC
- Lead-free and Halogen-free products are RoHS Compliant

Pin Assignment：

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	12V	41	NC	81	BA0	121	DM6,DBI6	161	DQ9	201	CB3	241	VSS	281	VSS
2	VSS	42	VSS	82	RAS_n/A16	122	NC	162	VSS	202	VSS	242	DQ33	282	DQ59
3	DQ4	43	DQ30	83	VDD	123	VSS	163	DQS1_C	203	CKE1	243	VSS	283	VSS
4	VSS	44	VSS	84	CS0_n	124	DQ54	164	DQS1_T	204	VDD	244	DQS4_C	284	VDDSPD
5	DQ0	45	DQ26	85	VDD	125	VSS	165	VSS	205	RFU	245	DQS4_T	285	SDA
6	VSS	46	VSS	86	CAS_n/A15	126	DQ50	166	DQ15	206	VDD	246	VSS	286	VPP
7	DM0,DBI0	47	CB4	87	ODT0	127	VSS	167	VSS	207	BG1	247	DQ39	287	VPP
8	NC	48	VSS	88	VDD	128	DQ60	168	DQ11	208	ALERT_n	248	VSS	288	VPP
9	VSS	49	CB0	89	CS1_n	129	VSS	169	VSS	209	VDD	249	DQ35		
10	QD6	50	VSS	90	VDD	130	DQ56	170	DQ21	210	A11	250	VSS		
11	VSS	51	DM8,DBI8	91	ODT1	131	VSS	171	VSS	211	A7	251	DQ45		
12	DQ2	52	NC	92	VDD	132	DM7,DBI7	172	DQ17	212	VDD	252	VSS		
13	VSS	53	VSS	93	NC	133	NC	173	VSS	213	A5	253	DQ41		
14	DQ12	54	CB6	94	VSS	134	VSS	174	DQS2_C	214	A4	254	VSS		
15	VSS	55	VSS	95	DQ36	135	DQ62	175	DQS2_T	215	VDD	255	DQS5_C		
16	DQ8	56	CB2	96	VSS	136	VSS	176	VSS	216	A2	256	DQS5_T		
17	VSS	57	VSS	97	DQ32	137	DQ58	177	DQ23	217	VDD	257	VSS		
18	DM1,DBI1	58	RESET_n	98	VSS	138	VSS	178	VSS	218	CK1_T	258	DQ47		
19	NC	59	VDD	99	DM4,DBI4	139	SA0	179	DQ19	219	CK1_C	259	VSS		
20	VSS	60	CKE0	100	NC	140	SA1	180	VSS	220	VDD	260	DQ43		
21	DQ14	61	VDD	101	VSS	141	SCL	181	DQ29	221	VTT	261	VSS		
22	VSS	62	ACT_n	102	DQ38	142	VPP	182	VSS	222	PARITY	262	DQ53		
23	DQ10	63	BG0	103	VSS	143	VPP	183	DQ25	223	VDD	263	VSS		
24	VSS	64	VDD	104	DQ34	144	RFU	184	VSS	224	BA1	264	DQ49		
25	DQ20	65	A12/BC_n	105	VSS	145	12V	185	DQS3_C	225	A10/AP	265	VSS		
26	VSS	66	A9	106	DQ44	146	VREFCA	186	DQS3_T	226	VDD	266	DQS6_C		
27	DQ16	67	VDD	107	VSS	147	VSS	187	VSS	227	RFU	267	DQS6_T		
28	VSS	68	A8	108	DQ40	148	DQ5	188	DQ31	228	WE_n/A14	268	VSS		
29	DM2,DBI2	69	A6	109	VSS	149	VSS	189	VSS	229	VDD	269	DQ55		
30	NC	70	VDD	110	DM5,DBI5	150	DQ1	190	DQ27	230	NC	270	VSS		
31	VSS	71	A3	111	NC	151	VSS	191	VSS	231	VDD	271	DQ51		
32	DQ22	72	A1	112	VSS	152	DQS0_C	192	CB5	232	A13	272	VSS		
33	VSS	73	VDD	113	DQ46	153	DQS0_T	193	VSS	233	VDD	273	DQ61		
34	DQ18	74	CK0_t	114	VSS	154	VSS	194	CB1	234	NC	274	VSS		
35	VSS	75	CK0_c	115	DQ42	155	DQ7	195	VSS	235	NC	275	DQ57		
36	DQ28	76	VDD	116	VSS	156	VSS	196	DQS8_C	236	VDD	276	VSS		
37	VSS	77	VTT	117	DQ52	157	DQ3	197	DQS8_T	237	NC	277	DQS7_C		
38	DQ24	78	EVENT_n	118	VSS	158	VSS	198	VSS	238	SA2	278	DQS7_T		
39	VSS	79	A0	119	DQ48	159	DQ13	199	CB7	239	VSS	279	VSS		
40	DM3,DBI3	80	VDD	120	VSS	160	VSS	200	VSS	240	DQ37	280	DQ63		

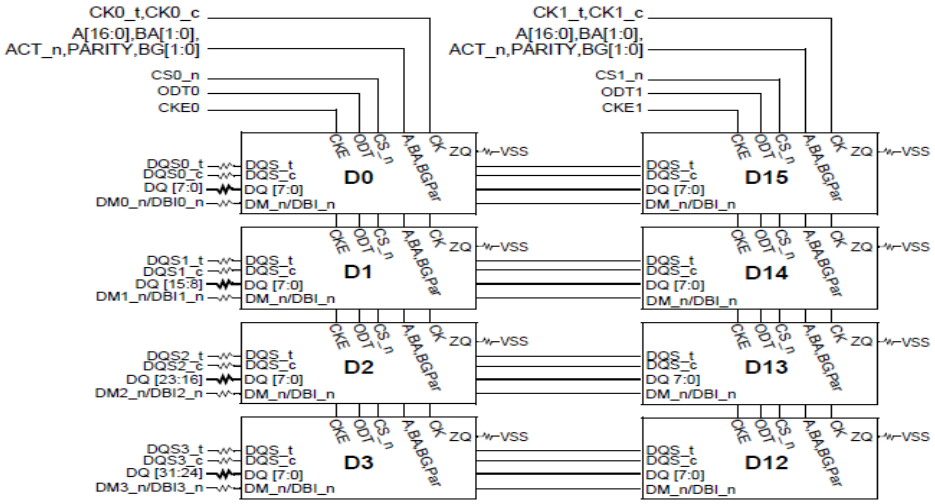
Pin Description：

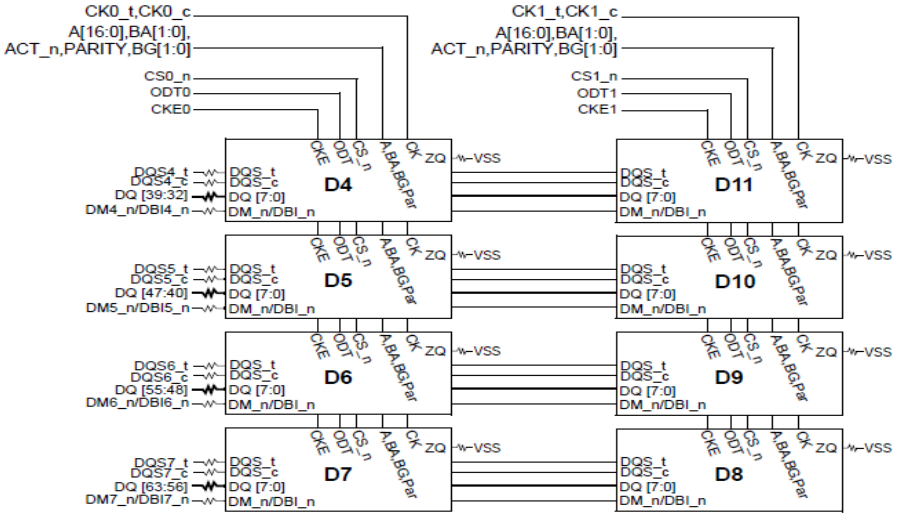
Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address bus	SCL	I2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD-TSE
RAS_n[2]	SDRAM row address strobe	PAR	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE_n[4]	SDRAM write enable	12V	Optional power Supply on socket but not used on UDIMM`
CS0_n,CS1_n	DIMM Rank Select Lines	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	SDRAM clock enable lines	VSS	Power supply return (ground)
ODT0, ODT1	SDRAM on-die termination control lines	VDDSPD	Serial SPD/TSE positive power supply
ACT_n	SDRAM activate	ALERT_n	SDRAM ALERT_n
DQ0–DQ63	DIMM memory data bus	RESET_n	Set DRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS8_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS8_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)		
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)		
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

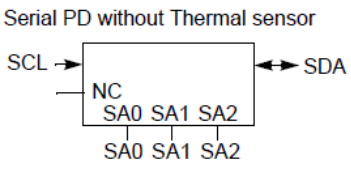
1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

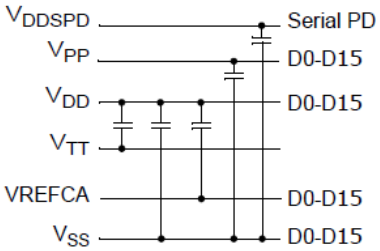
Block Diagram：

[16GB – 2Rank, 1024Mx8 DDR4 SDRAMs]









Absolute Maximum Ratings：

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	VDD	-0.3 ~ 1.5	V
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~1.5	V
Voltage on VPP pin relative to Vss	VPP	-0.3 ~3.0	V
Voltage on any pin relative to Vss	VIN, Vout	-0.3 ~ 1.5	V
Storage temperature	TSTG	-55 ~ +100	℃

Note: DDR4 SDRAM component specification.

Operation Temperature Condition

Parameter	Symbol	Value	Unit	Note
Normal Operating Temperature Range	TC	0~+85	℃	
Extended Temperature Range (Optional)	TC	+85~+95	℃	1

Note: (1) Refresh commands must be doubled in frequency, reducing the refresh interval tREFI to 3.9 μs

DC Operating Condition：

Voltage referenced to Vss = 0V, VDD&VDDQ=1.14V~1.26V, Tc = 0 to 85 ℃

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	1.14	1.2	1.26	V	1,2,3
	VDDSPD	2.25	2.5	3.6	V	
Supply Voltage for Output	VDDQ	1.14	1.2	1.26	V	1,2,3
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3
Reference Voltage for CMD/ADD	VREFCA, (DC)	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	4
Termination Voltage	VTT	0.49 x VDDQ-20mV	0.5 x VDD	0.51 x VDDQ+20mV	V	

Note: (1) Under all conditions VDDQ must be less than or equal to VDD.

(2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

(3) The DC bandwidth is limited to 20MHz.

(4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

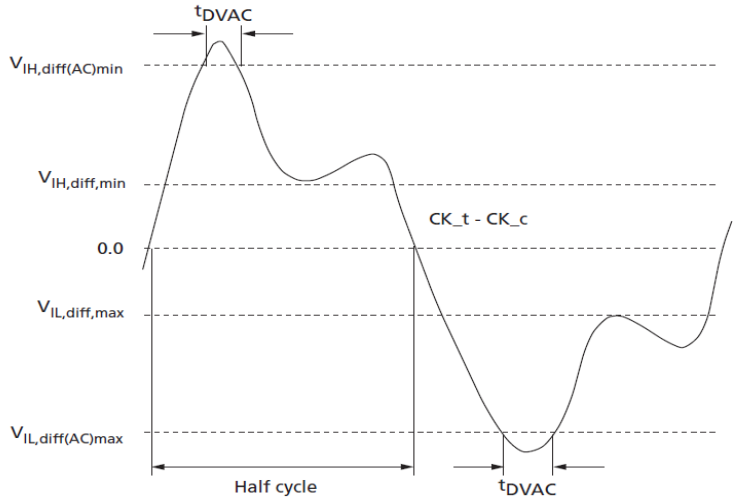
Input DC & AC Logic Level for single-ended signals：

Parameter	Symbol	Min	Max	Unit	Note
DC Input logic high voltage	VIH.CA (DC65)	VREFCA+65	VDD	mV	
DC Input logic low voltage	VIL.CA (DC65)	VSS	VREFCA-65	mV	
AC input logic high	VIH.CA(AC90)	VREF+90	Note 2	mV	1
AC input logic low	VIL.CA(AC90)	Note 2	VREF–90	mV	1

Note: 1. See “Overshoot and Undershoot Specifications” on section.

2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)

Input AC &DC Logic Level for Differential signals：



Parameter	Symbol	DDR4 -1600 / 1866 / 2133		DDR4 -2400 / 2666		Unit	Note
		Min	Max	Min	Max		
Differential input high	VIHdiff	+0.150	Note 3	+0.135	Note 3	V	1
Differential input low	VILdiff	Note 3	TBD	Note 3	-0.135	V	1
Differential input high AC	VIHdiff(AC)	2 (VIH(ac)-Vref)	Note 3	2 (VIH(ac)-Vref)	Note 3	V	2
Differential input low AC	VILdiff (AC)	Note 3	2 x (VIL(ac)- Vref)	Note 3	2 x (VIL(ac)- Vref)	V	2

Notes: 1. Used to define a differential signal slew-rate.

2. For CK_t – CK_c use VIH/VIL(ac) of ADD/CMD and VREFCA

3. These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot on Component Datasheet.

IDD Specification：

VDDQ = VDD = 1.2V(1.14V~1.26V)

Symbol	Condition	16GB	Unit
IDD0[1]	One bank ACTIVATE-PRECHARGE current	368	mA
IPP0[1]	One bank ACTIVATE-PRECHARGE,wordline boost,IPP current	56	mA
IDD1[1]	One Bank Active-Read-Precharge Current	400	mA
IDD2N[2]	Precharge Standby Current	288	mA
IDD2NT[1]	Precharge standby ODT current	336	mA
IDD2P[2]	Precharge Power-Down Current	176	mA
IDD2Q[2]	Precharge Quiet Standby Current	272	mA
IDD3N[2]	Active standby current	432	mA
IPP3N[2]	Active standby IPP current	64	mA
IDD3P[2]	Active Power-Down Current	304	mA
IDD4R[1]	Burst Read Current	936	mA
IDD4W[1]	Burst write current	880	mA
IDD5B[1]	Burst refresh current (1x REF)	1624	mA
IPP5B[1]	Burst refresh IPP current (1x REF)	168	mA
IDD6N[2]	Self refresh current: Normal temperature range (0–85°C)	336	mA
IDD6E[2]	Self refresh current: Extended temperature range (0–95°C)	544	mA
IDD7[1]	Bank interleave read current	1320	mA
IPP7[1]	Bank interleave read IPP current	112	mA
IDD8[2]	Maximum power-down current	160	mA

Note:

1. One module rank in the active IDD/PP, the other rank in IDD2N/PP2N.

2. All ranks in this IDD/PP condition.

3.IDD current measure method and detail patterns are described on DDR4 component datasheet. Only for reference.

Timings used for IDD, IPP and IDDQ Measurement：

Symbol		DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Units
Bin(CL-tRCD-tRP)		13-13-13	15-15-15	17-17-17	19-19-19	
Parameter		Min	Min	Min	Min	
tCK		1.071	0.937	0.833	0.75	ns
CL		13	15	17	19	nCK
CWL		12	14	16	18	nCK
nRCD		13	15	17	19	nCK
nRC		45	51	56	62	nCK
nRAS		32	36	39	43	nCK
nRP		13	15	17	19	nCK
nFAW	X4	16	16	16	16	nCK
	X8	22	23	26	28	nCK
	X16	28	32	36	40	nCK
nRRDS	X4	4	4	4	4	nCK
	X8	4	4	4	4	nCK
	X16	5	6	7	8	nCK
nRRDL	X4	5	6	6	7	nCK
	X8	5	6	6	7	nCK
	X16	6	7	8	9	nCK
tCCD_S		4	4	4	4	nCK
tCCD_L		5	6	6	7	nCK
tWTR_S		3	3	3	4	nCK
tWTR_L		7	8	9	10	nCK
nRFC 2Gb		150	171	193	214	nCK
nRFC 4Gb		243	278	313	347	nCK
nRFC 8Gb		327	374	421	467	nCK
nRFC 16Gb		TBD	TBD	TBD	734	nCK

Timing Parameters:

Parameter		Symbol	DDR4-2666		DDR4-2933		Reserved		Reserved		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing												
Clock period average: DLL disable mode		^{t}CK (DLL_OFF)	8	–	8	–					ns	
Clock period average: DLL enable mode		^{t}CK (AVG), (DLL_ON)	0.75	1.6	0.682	1.6					ns	14
High pulse width average		^{t}CH (AVG)	0.48	0.52	0.48	0.52					CK	
Low pulse width average		^{t}CL (AVG)	0.48	0.52	0.48	0.52					CK	
Clock period jitter	Total	$^{t}JIT_{PER\_TOT}$	–38	38	–34	34					ps	
	Deterministic	$^{t}JIT_{PER\_DJ}$	–19	19	–17	17					ps	
	DLL locking	$^{t}JIT_{PER,\ LCK}$	–30	30	–27	27					ps	
Clock absolute period		^{t}CK(ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITPER_TOT MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITPER_TOT MAX								ps	
Clock absolute high pulse width		^{t}CH (ABS)	0.45	–	0.45	–					^{t}CK (AVG)	
Clock absolute low pulse width		^{t}CL (ABS)	0.45	–	0.45	–					^{t}CK (AVG)	
Cycle-to-cycle jitter	Total	$^{t}JIT_{CC\_TOT}$	75		–68						ps	
	Deterministic	$^{t}JIT_{CC\_DJK}$	38		–34						ps	
	DLL locking	$^{t}JIT_{CC,\ LCK}$	60		–68						ps	
Cumulative error across	2 cycles	$^{t}ERR_{2PER}$	–55	55	–50	50					ps	
	3 cycles	$^{t}ERR_{3PER}$	–66	66	–59	59					ps	
	4 cycles	$^{t}ERR_{4PER}$	–73	73	–66	66					ps	
	5 cycles	$^{t}ERR_{5PER}$	–79	79	–71	71					ps	
	6 cycles	$^{t}ERR_{6PER}$	–83	83	–75	75					ps	
	7 cycles	$^{t}ERR_{7PER}$	–87	87	–79	79					ps	
	8 cycles	$^{t}ERR_{8PER}$	–91	91	–82	82					ps	
	9 cycles	$^{t}ERR_{9PER}$	–94	94	–85	85					ps	
	10 cycles	$^{t}ERR_{10PER}$	–96	96	–87	87					ps	
	11 cycles	$^{t}ERR_{11PER}$	–99	99	–89	89					ps	
	12 cycles	$^{t}ERR_{12PER}$	–101	101	–91	91					ps	
	n = 13, 14 . . . 49, 50 cycles	$^{t}ERR_{nPER}$	$^{t}ERR_{nPER}$ MIN = (1 + 0.68ln[*n*]) × $^{t}JIT_{PER}$ MIN $^{t}ERR_{nPER}$ MAX = (1 + 0.68ln[*n*]) × $^{t}JIT_{PER}$ MAX								ps	

Parameter		Symbol	DDR4-2666		DDR4-2933		Reserved		Reserved		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQ Input Timing												
Data setup time to DQS, DQS#	Base (calibrated V_{REF})	^{t}DS	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.35^{t}CK)								–	
	Non-calibrated V_{REF}	^{t}PDA_S	minimum of 0.5ui								UI	
Data hold time from DQS, DQS#	Base (calibrated V_{REF})	^{t}DH	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.35^{t}CK)								–	
	Non-calibrated V_{REF}	^{t}PDA_H	minimum of 0.5ui								UI	
DQ and DM minimum data pulse width		^{t}DIPW	0.58	–	0.58	–					UI_d	
DQ Output Timing (DLL enabled)												
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	0.18	–	0.18					UI_d	
DQ output hold time from DQS, DQS#		^{t}QH	0.74	–	0.74	–					UI_d	
Data valid window per device: ^{t}QH - ^{t}DQSQ for a device		$^{t}DVW_d$	0.63	–	0.63	–					UI_d	
Data valid window per device per pin: ^{t}QH - ^{t}DQSQ per pin for a device		$^{t}DVW_p$	0.72	–	0.72	–					UI_d	
DQ Low-Z time from CK, CK#		^{t}LZ (DQ)	–340	140	–330	135					ps	
DQ High-Z time from CK, CK#		^{t}HZ (DQ)	–	140	–	135					ps	
DQ Strobe Input Timing												
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1^{t}CKpreamble		$^{t}DQSS_{1ck}$	–0.27	0.27	–0.27	0.27					CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2^{t}CKpreamble		$^{t}DQSS_{2ck}$	–0.5	0.5	–0.5	0.5					CK	
DQS, DQS# differential input low pulse width		^{t}DQSL	0.46	0.54	0.46	0.54					CK	
DQS, DQS# differential input high pulse width		^{t}DQSH	0.46	0.54	0.46	0.54					CK	
DQS, DQS# falling setup to CK, CK# rising		^{t}DSS	0.18	–	0.18	–					CK	
DQS, DQS# falling hold from CK, CK# rising		^{t}DSH	0.18	–	0.18	–					CK	
DQS, DQS# differential WRITE preamble		^{t}WPRE	0.9	–	0.9	–					CK	
DQS, DQS# differential WRITE postamble		^{t}WPST	0.33	–	0.33	–					CK	

Parameter		Symbol	DDR4-2666		DDR4-2933		Reserved		Reserved		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQ Strobe Output Timing (DLL enabled)												
DQS, DQS# rising to/from rising CK, CK#		^{t}DQSCK	-170	170	-165	165					ps	
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		^{t}DQSCKi	-	270	-	265					ns	
DQS, DQS# differential output high time		^{t}QSH	0.40	-	0.40	-					CK	
DQS, DQS# differential output low time		^{t}QSL	0.40	-	0.40	-					CK	
DQS, DQS# Low-Z time (RL - 1)		^{t}LZ (DQS)	-340	140	-330	130					ps	
DQS, DQS# High-Z time (RL + BL/2)		^{t}HZ (DQS)	-	140	-	135					ps	
DQS, DQS# differential READ preamble		^{t}RPRE	0.9	-	0.9	-					CK	
DQS, DQS# differential READ postamble		^{t}RPST	0.33	-	0.33	-					CK	
Command and Address Timing												
DLL locking time		^{t}DLLK	854	-	940	-					CK	2, 3
CMD, ADDR setup time to CK_t, CK_c referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$ levels	Base	^{t}IS	55	-	48	-					ps	
	V_{REFCA}	$^{t}IS_{REF}$	145	-	138	-					ps	
CMD, ADDR hold time to CK_t, CK_c referenced to $V_{IH(DC)}$ and $V_{IL(DC)}$ levels	Base	^{t}IH	80	-	73	-					ps	
	V_{REFCA}	$^{t}IH_{REF}$	145	-	138	-					ps	
Minimum CTRL, CMD, ADDR pulse width		^{t}IPW	385	-	365	-					ps	
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD								ns	
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP								ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS								ns	13
ACTIVATE-to-ACTIVATE command period		^{t}RC	See Speed Bin Tables for ^{t}RC								ns	13
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size		^{t}RRD_S (1/2KB)	MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 3.0ns						CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size		^{t}RRD_S (1KB)	MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 3.0ns						CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size		^{t}RRD_S (2KB)	MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns						CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size		^{t}RRD_L (1/2KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns						CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size		^{t}RRD_L (1KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns						CK	1

Parameter	Symbol	DDR4-2666		DDR4-2933		Reserved		Reserved		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size	^{t}RRD_L (2KB)	MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns						CK	1
Four ACTIVATE windows for 1/2KB page size	^{t}FAW (1/2KB)	MIN = greater of 16CK or 12ns		MIN = greater of 16CK or 12ns						CK	1
Four ACTIVATE windows for 1KB page size	^{t}FAW (1KB)	MIN = greater of 20CK or 21ns		MIN = greater of 20CK or 21ns						ns	
Four ACTIVATE windows for 2KB page size	^{t}FAW (2KB)	MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns						ns	
Write recovery time	^{t}WR	MIN = 15ns								ns	5, 10, 1
	$^{t}WR_2$	MIN = 1CK + ^{t}WR								CK	5, 11, 1
Write recovery time when CRC and DM are both enabled	^{t}WR_CRC_DM	MIN = ^{t}WR + greater of (5CK or 3.75ns)								ns	6, 10, 1
	$^{t}WR_{CRC}DM_2$	MIN = 1CK + ^{t}WR_CRC_DM								CK	6, 11, 1
Delay from start of internal WRITE transaction to internal READ command	^{t}WTR_L	MIN = greater of 4CK or 7.5ns								CK	5, 10, 1
	$^{t}WTR_L_2$	MIN = 1CK + ^{t}WTR_L								CK	5, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	^{t}WTR_L_CRC_DM	MIN = ^{t}WR + greater of (5CK or 3.75ns)								CK	6, 10, 1
	$^{t}WTR_{L}CRC_{DM_2}$	MIN = 1CK + ^{t}WTR_L_CRC_DM								CK	6, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group	^{t}WTR_S	MIN = greater of (2CK or 2.5ns)								CK	5, 7, 8, 10, 1
	$^{t}WTR_S_2$	MIN = 1CK + ^{t}WTR_S								CK	5, 7, 8, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	^{t}WTR_S_CRC_DM	MIN = ^{t}WR + greater of (5CK or 3.75ns)								CK	6, 7, 8, 10, 1
	$^{t}WTR_{S}CRC_{DM_2}$	MIN = 1CK + ^{t}WTR_S_CRC_DM								CK	6, 7, 8, 11, 1
READ-to-PRECHARGE time	^{t}RTP	MIN = greater of 4CK or 7.5n								CK	1
CAS#-to-CAS# command delay to different bank group	^{t}CCD_S	4	–	4	–					CK	
CAS#-to-CAS# command delay to same bank group	^{t}CCD_L	MIN = greater of 4CK or 5n	–	MIN = greater of 4CK or 5n	–					CK	15
Auto precharge write recovery + precharge time	^{t}DAL(MIN)	MIN = WR + ROUNDUP(^{t}RP/^{t}CK (AVG); MAX = n/a								CK	
MRS Command Timing											

Parameter	Symbol	DDR4-2666		DDR4-2933		Reserved		Reserved		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
MRS command cycle time	tMRD	9	–	10	–					CK	
MRS command cycle time in PDA mode	tMRD_PDA	MIN = greater of (16nCK; 10ns)								CK	1
MRS command cycle time in CAL mode	tMRD_CAL	MIN = tMOD + tCAL								CK	
MRS command update delay	tMOD	MIN = greater of (24nCK; 15ns)								CK	1
MRS command update delay in PDA mode	tMOD_PDA	MIN = tMOD								CK	
MRS command update delay in CAL mode	tMOD_CAL	MIN = tMOD + tCAL								CK	
MRS command to DQS drive in preamble training	tSDO	MIN = tMOD + 9ns									
MPR Command Timing											
Multipurpose register recovery time	tMPRR	MIN = 1nCK								CK	
Multipurpose register write recovery time	tWR_MPRR	MIN = tMOD + AL + PL								CK	
CRC Error Reporting Timing											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13					ns	
CRC ALERT_n pulse width	tCRC_ALERT_P_W	6	10	6	10					CK	
CA Parity Timing											
Parity latency	PL	6	–	8	–					CK	
Commands uncertain to be executed during this time	tPAR_UNKNOWN	–	PL							CK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	–	PL + 6ns							CK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	80	160	88	176					CK	
Time from alert asserted until DES commands required in persistent CA parity mode	tPAR_ALERT_RSP	–	71	–	78					CK	
CAL Timing											
CS_n to command address latency	tCAL	5	–	6	–					CK	
CS_n to command address latency	tCALg	6	–	8	–					CK	
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	MIN = tMOD (MIN) + tCPDED (MIN)								CK	1
Valid clock requirement after MPSM entry	tCKMPE	MIN = tMOD (MIN) + tCPDED (MIN)								CK	1
Valid clock requirement before MPSM exit	tCKMPX	MIN = tCK - tSRX (MIN)								CK	1
Exit MPSM to commands not requiring a locked DLL	tXMP	tSX (MIN)								CK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	MIN = tXMP (MIN) + tXSDLL (MIN)								CK	1

Parameter		Symbol	DDR4-2666		DDR4-2933		Reserved		Reserved		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
CS setup time to CKE		tMPX_S	MIN = tIS (MIN) + tIH (MIN)								ns	
CS_n HIGH hold time to CKE rising edge		tMPX_HH	MIN = tXP								ns	
CS_n LOW hold time to CKE rising edge		tMPX_LH	12	tXMP-10ns	12	tXMP-10ns					ns	
Connectivity Test Timing												
TEN pin HIGH to CS_n LOW – Enter CT mode		tCT_Enable	200	–	200	–					ns	
CS_n LOW and valid input to valid output		tCT_Valid	–	200	–	200					ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH		tCTEXT_Valid	10	–	10	–					ns	
Calibration and V_{REFDQ} Train Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQ_{INIT}	1024	–	1024	–					CK	
	Normal operation	tZQ_{OPER}	512	–	512	–					CK	
ZQCS command: Short calibration time		tZQ_{CS}	128	–	128	–					CK	
The V_{REF} increment/decrement step time		tZV_{REF_time}	MIN = 150ns									
Enter V_{REFDQ} training mode to the first write or V_{REFDQ} MRS command delay		tZV_{REFDQE}	MIN = 150ns								ns	1
Exit V_{REFDQ} training mode to the first WRITE command delay		tZV_{REFDQX}	MIN = 150ns								ns	1
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		tXPR	MIN = greater of 5CK or tRFC + 10ns								CK	1
RESET_L pulse low after power stable		tPW_REST_S	0.1	–	0.1	–					µs	
RESET_L pulse low after power-up		tPW_REST_L	200	–	200	–					µs	
Begin power supply ramp to power supplies stable		tV_{DDPR}	MIN = N/A; MAX = 200								ms	
RESET# LOW to power supplies stable		tRPS	MIN = 0; MAX = 0								ms	
RESET# LOW to I/O and R_{TT} High-Z		tIOz	MIN = N/A; MAX = undefined								ns	

Parameter		Symbol	DDR4-2666 Min	DDR4-2666 Max	DDR4-2933 Min	DDR4-2933 Max	Reserved Min	Reserved Max	Reserved Min	Reserved Max	Units	Notes
Refresh Timing												
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)	4Gb	^{t}RFC1	MIN = 260								ns	1, 11
		^{t}RFC2	MIN = 160								ns	1, 11
		^{t}RFC4	MIN = 110								ns	1, 11
	8Gb	^{t}RFC1	MIN = 350								ns	1, 11
		^{t}RFC2	MIN = 260								ns	1, 11
		^{t}RFC4	MIN = 160								ns	1, 11
	16Gb	^{t}RFC1	MIN = 550								ns	1, 11
		^{t}RFC2	MIN = 405								ns	1, 11
		^{t}RFC4	MIN = 250								ns	1, 11
Average periodic refresh interval	0° ≤ T_C ≤ 85°C	^{t}REFI	MIN = N/A; MAX = 7.8								µs	
	0° ≤ T_C ≤ 95°C		MIN = N/A; MAX = 3.9								µs	
Self Refresh Timing												
Exit self refresh to commands not requiring a locked DLL SRX to commands not requiring a locked DLL in self refresh abort		^{t}XS	MIN = ^{t}RFC + 10ns								ns	1
		^{t}XS_ABORT	MIN = ^{t}RFC4 + 10ns								ns	1
Exit self refresh to ZQCL, ZQCR, and MRS (CL, CWL, WR, RTP, and gear-down)		^{t}XS_FAST	MIN = ^{t}RFC4 + 10ns								ns	1
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN)								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + 1*n*CK								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled		^{t}CKESR_par	MIN = ^{t}CKE (MIN) + 1*n*CK + PL								CK	1
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns								CK	1
Valid clocks after self refresh entry or power-down entry when CA parity is enabled		^{t}CKSRE_par	MIN = greater of 5CK or 10ns + PL								CK	1
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns								CK	1
Power-Down Timing												
Exit power-down with DLL on to any value command		^{t}XP	MIN = greater of 4CK or 6ns								CK	1

Parameter		Symbol	DDR4-2666 Min	DDR4-2666 Max	DDR4-2933 Min	DDR4-2933 Max	Reserved Min	Reserved Max	Reserved Min	Reserved Max	Units	Notes
Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled		^{t}XP_PAR	MIN = (greater of 4CK or 6ns) + PL								CK	1
CKE MIN pulse width		^{t}CKE (MIN)	MIN = greater of 3CK or 5ns								CK	1
Command pass disable delay		^{t}CPDED	5	–	5	–					CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 x ^{t}REFI								CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK								CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time								CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XSDLL								CK	
Power-Down Entry Minimum Timing												
ACTIVATE command to power-down entry		^{t}ACTPDEN	2	–	2	2		–			CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	2	–	2	2		–			CK	
REFRESH command to power-down entry		^{t}REFPDEN	2	–	2	2		–			CK	1
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)								CK	1
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1								CK	1
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)								CK	1
	BC4MRS	^{t}WRPBC4DEN	MIN = WL + 2 + ^{t}WR/^{t}CK (AVG) CK								CK	1
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAPDEN	MIN = WL + 4 + WR + 1								CK	1
	BC4MRS	^{t}WRAPBC4DEN	MIN = WL + 2 + WR + 1								CK	1
ODT Timing												
Direct ODT turn-on latency		DODTL on	WL - 2 = CWL + AL - 2CK								CK	
Direct ODT turn-off latency		DODTL off	WL - 2 = CWL + AL - 2CK								CK	

Parameter	Symbol	DDR4-2666		DDR4-2933		Reserved		Reserved		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
R_{TT} dynamic change skew	tADC	0.3	0.7	0.3	0.7					CK	
Asynchronous $R_{TT(NOM)}$ turn-on delay (with DLL off)	tAONAS	1	9	1	9					ns	
Asynchronous $R_{TT(NOM)}$ turn-off delay (with DLL off)	tAOFAS	1	9	1	9					ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1tCK	6	–	6	–					CK	
	ODTH8 2tCK	7	–	7	–					CK	
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4 1tCK	4	–	4	–					CK	
	ODTH4 2tCK	5	–	5	–					CK	
Write Leveling Timing											
First DQS, DQS# rising edge	tWLMRD	40	–	40	–					CK	
DQS, DQS# delay	tWLDQSEN	25	–	25	–					CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	0.13	–	0.13	–					CK	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	0.13	–	0.13	–					CK	
Write leveling output delay	tWLO	0	9.5	0	9.5					ns	
Write leveling output error	tWLOE	0	2	0	2					ns	
Gear-Down Timing											
Exit reset from CKE HIGH to a valid MRS gear-down	tXPR_GEAR	tXPR		tXPR						CK	
CKE HIGH assert to gear-down enable time)	tXS_GEAR	tXS		tXS						CK	
MRS command to sync pulse time	tSYNC_GEAR	tMOD + 4CK		tMOD + 4CK						CK	
Sync pulse to first valid command	tCMD_GEAR	tMOD		tMOD						CK	
Gear-down setup time	tGEAR_setup	2CK	–	2CK	–					CK	
Gear-down hold time	tGEAR_hold	2CK	–	2CK	–					CK	

NOTE :

1. Start of internal write transaction is defined as follows :

   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.

   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.

   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled

3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.

5. WR in clock cycles as programmed in MR0.

6. tREFI depends on TOPER.

7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied

9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

12. The max values are system dependent.

13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in Device Operation.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400 speed grade.

44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Device Operation. to Data Strobe Relationship".

Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in See Device Operation Preamble".

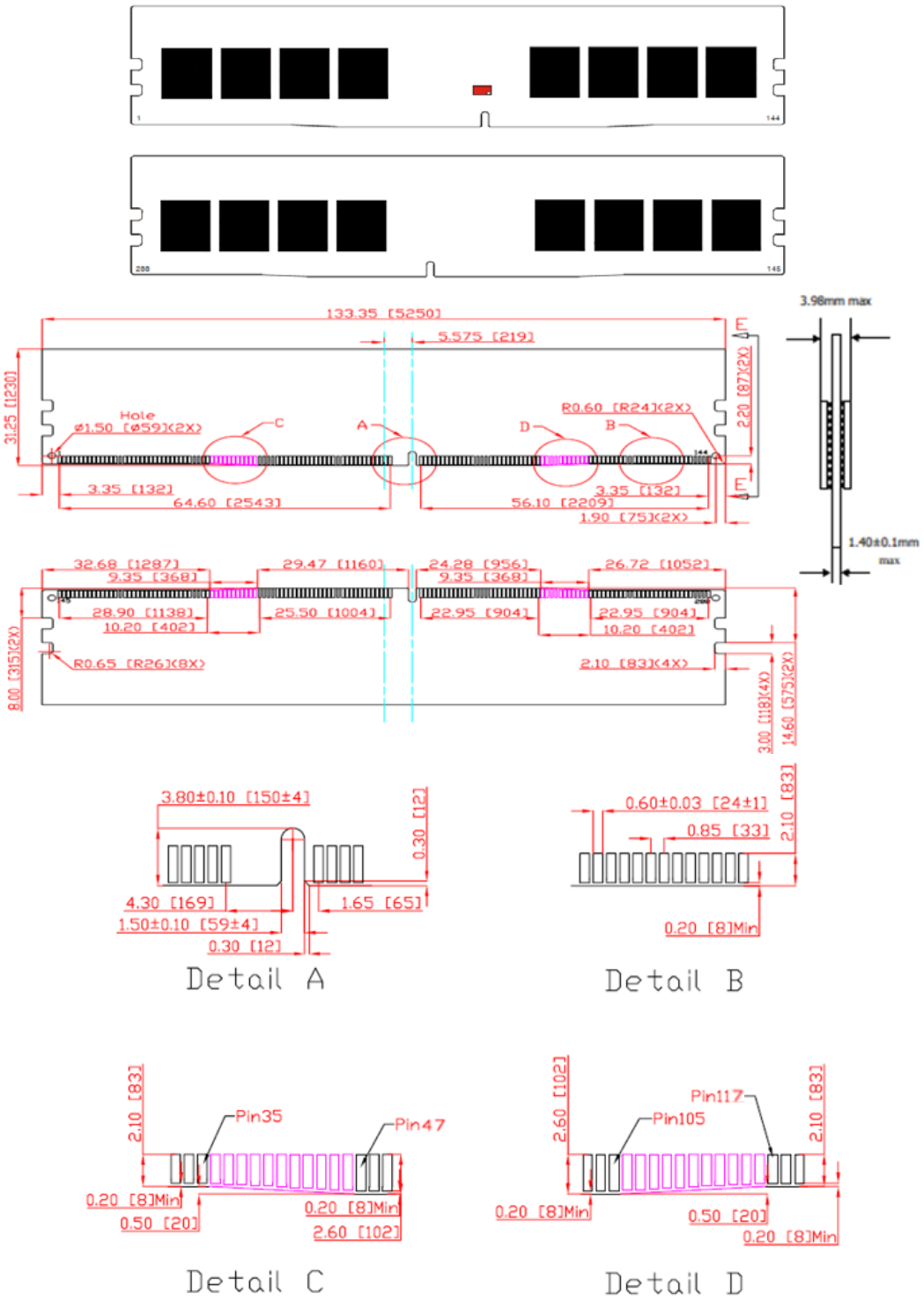
45.DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point

46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High

47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

Package Dimensions：

[16GB – 2Rank, 1024Mx8 DDR4 SDRAMs]



Note: All dimensions are in millimeters(mils) and should be kept within a tolerance of ± 0.15(5.91),unless otherwise specified.