

N-Channel and P-Channel Enhancement Mode Power MOSFET

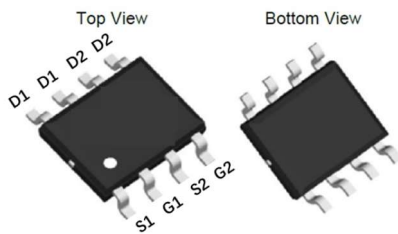
Features

- N-Channel: 40V, 8A
 $R_{DS(ON)} < 14 \text{ m}\Omega @ V_{GS} = 10\text{V}$
 $R_{DS(ON)} < 19 \text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- P-Channel: -40V, -7A
 $R_{DS(ON)} < 29 \text{ m}\Omega @ V_{GS} = -10\text{V}$
 $R_{DS(ON)} < 34 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$

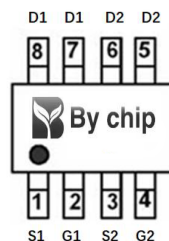
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

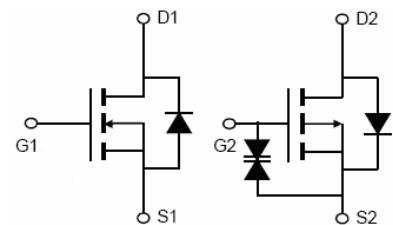
100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8 Dual



Pin Assignment



Schematic diagram

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_D	8	-7	A
	$T_A=70^\circ\text{C}$		6	-5.5	
Pulsed Drain Current (Note 1)		I_{DM}	40	-30	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.0	2.0	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 To 150	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note2)	$R_{\theta JA}$	N-Ch	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Note2)	$R_{\theta JA}$	P-Ch	62.5	$^\circ\text{C/W}$

N-CH Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =8A	-		14	mΩ
		V _{GS} =4.5V, I _D =4A	-		19	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =8A	33	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, F=1.0MHz	-	1110	-	PF
Output Capacitance	C _{oss}		-	114	-	PF
Reverse Transfer Capacitance	C _{rss}		-	109	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, R _L =2.5Ω V _{GS} =10V, R _{GEN} =3Ω	-	5.5	-	nS
Turn-on Rise Time	t _r		-	14	-	nS
Turn-Off Delay Time	t _{d(off)}		-	24	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =20V, I _D =8A, V _{GS} =10V	-	30	-	nC
Gate-Source Charge	Q _{gs}		-	5	-	nC
Gate-Drain Charge	Q _{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =8A	-	0.8	1.2	V

P-CH Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-7A	-		29	mΩ
		V _{GS} =-4.5V, I _D =-4A	-		34	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-7A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V, F=1.0MHz	-	1139	-	PF
Output Capacitance	C _{oss}		-	114	-	PF
Reverse Transfer Capacitance	C _{rss}		-	103	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V, R _L =2.9Ω V _{GS} =-10V, R _{GEN} =6Ω	-	7.5	-	nS
Turn-on Rise Time	t _r		-	5.5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	19	-	nS
Turn-Off Fall Time	t _f		-	7	-	nS
Total Gate Charge	Q _g	V _{DS} =-20V, I _D =-7A V _{GS} =-10V	-	22.5	-	nC
Gate-Source Charge	Q _{gs}		-	2.4	-	nC
Gate-Drain Charge	Q _{gd}		-	5.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-7A	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

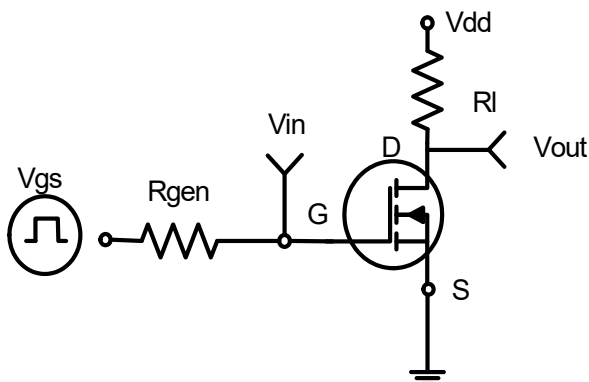


Figure 1: Switching Test Circuit

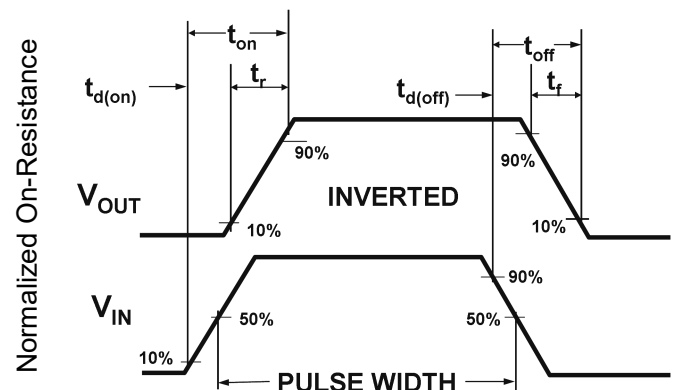


Figure 2: Switching Waveforms

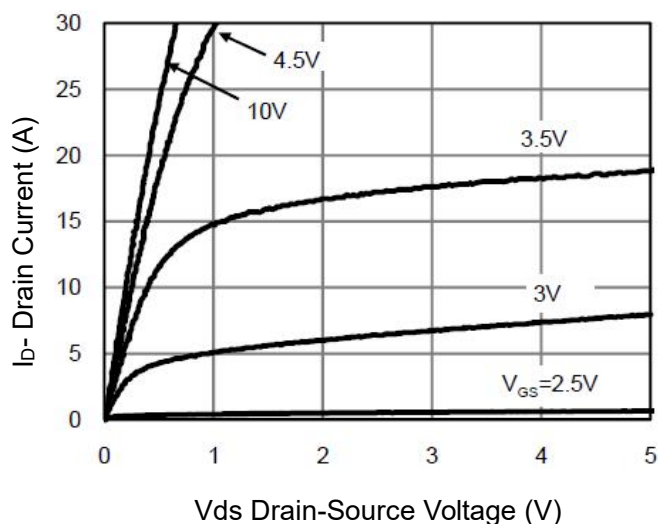


Figure 3 Output Characteristics

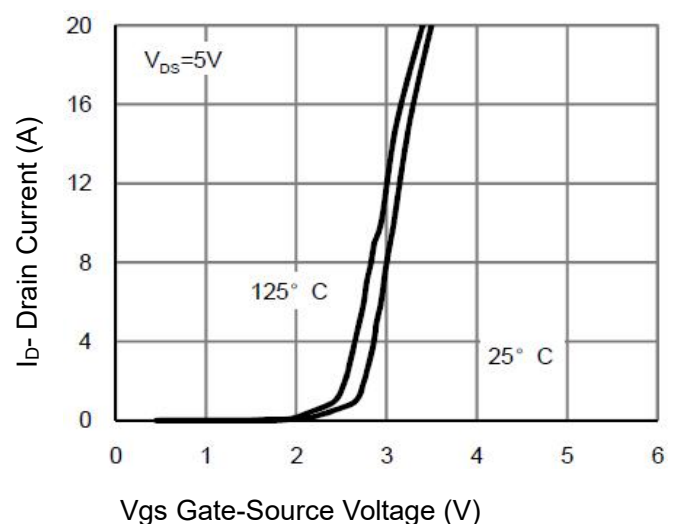


Figure 4 Transfer Characteristics

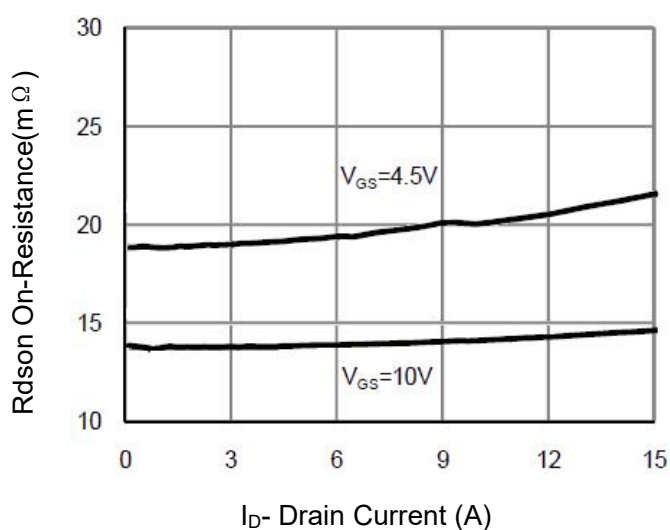


Figure 5 Drain-Source On-Resistance

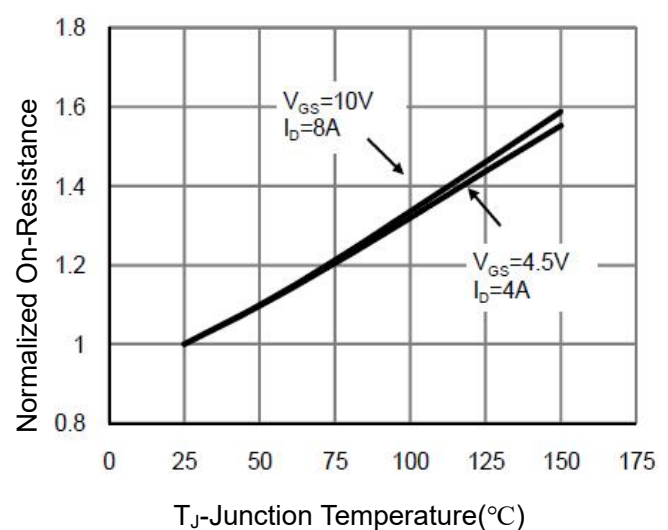


Figure 6 Drain-Source On-Resistance

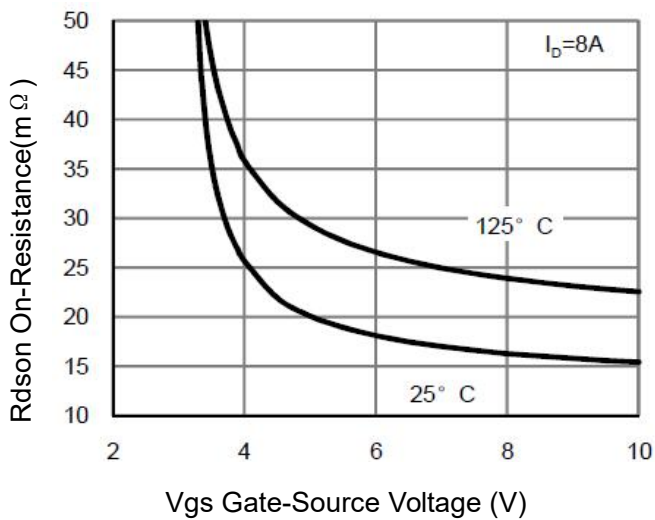


Figure7 Rdson vs Vgs

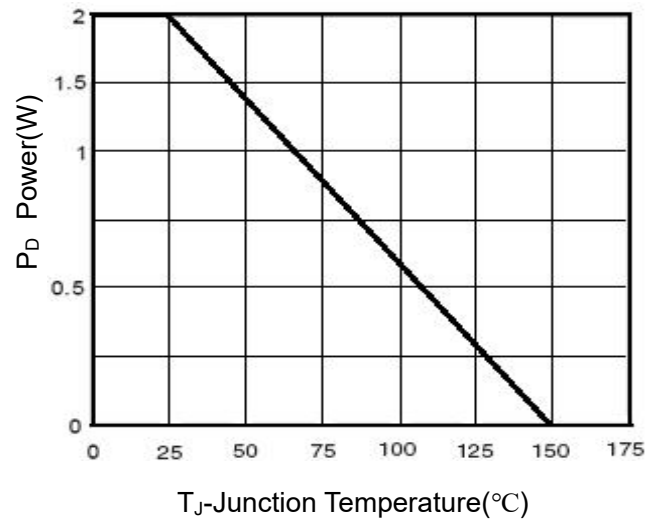


Figure 8 Power Dissipation

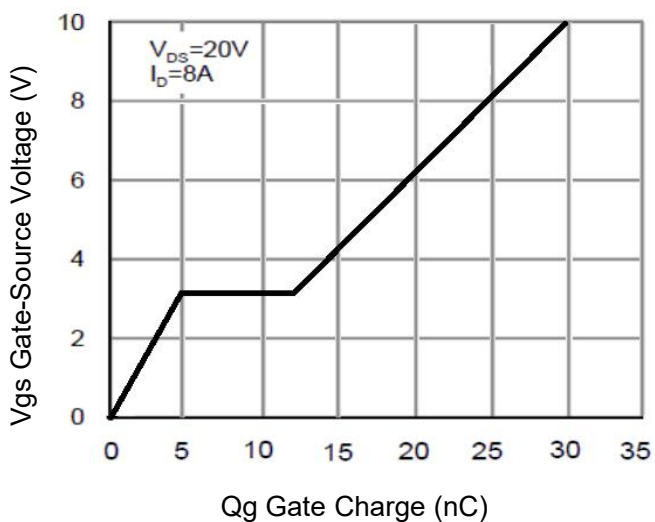


Figure 9 Gate Charge

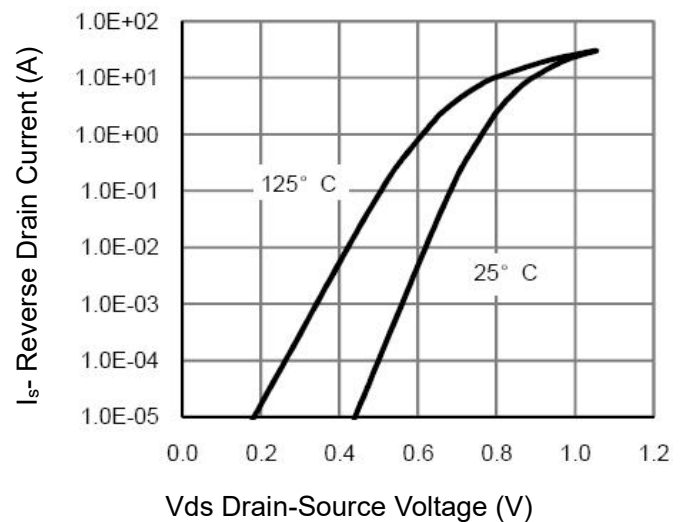


Figure 10 Source- Drain Diode Forward

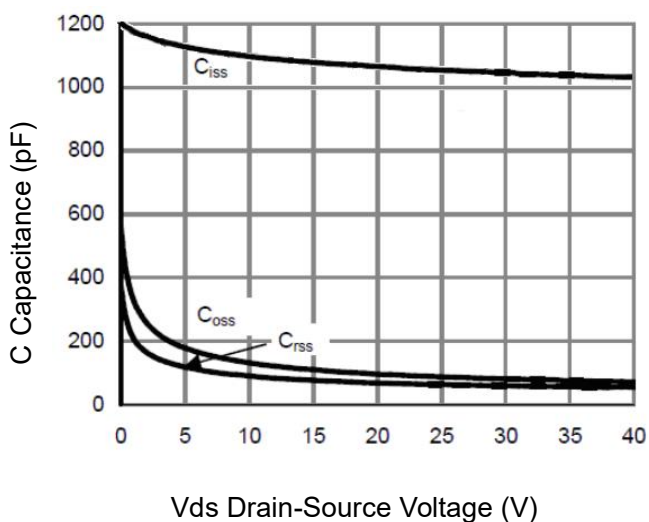


Figure 11 Capacitance vs Vds

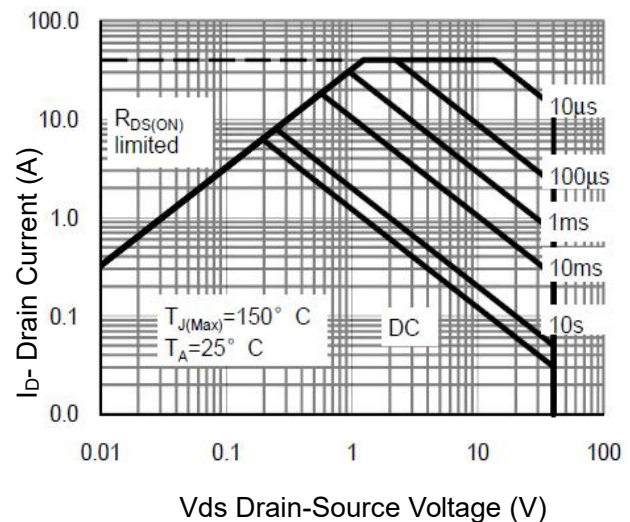


Figure 12 Safe Operation Area

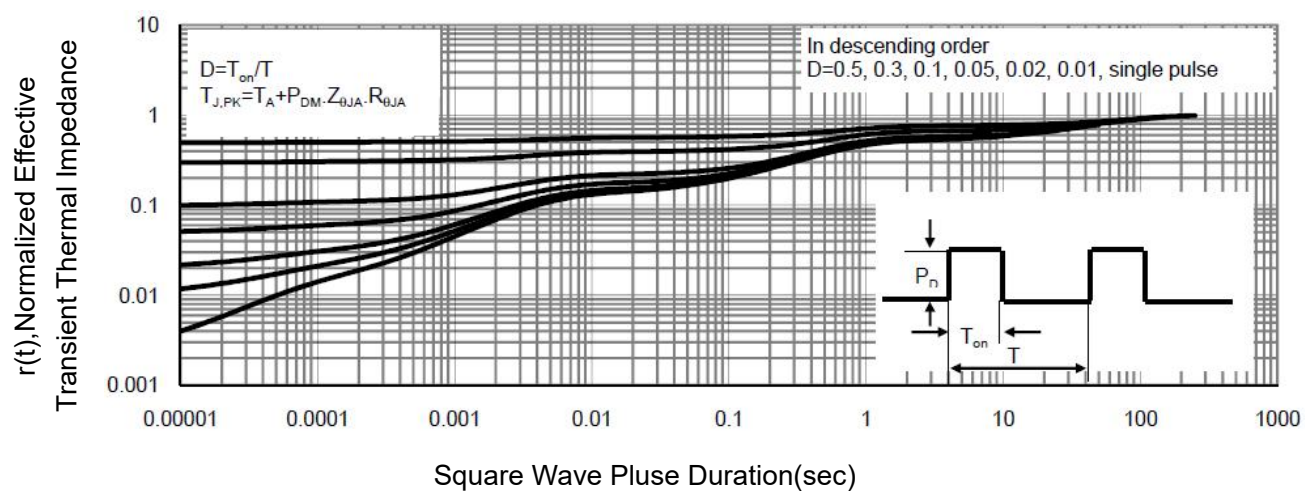


Figure 13 Normalized Maximum Transient Thermal Impedance

P- Channel Typical Electrical and Thermal Characteristics (Curves)

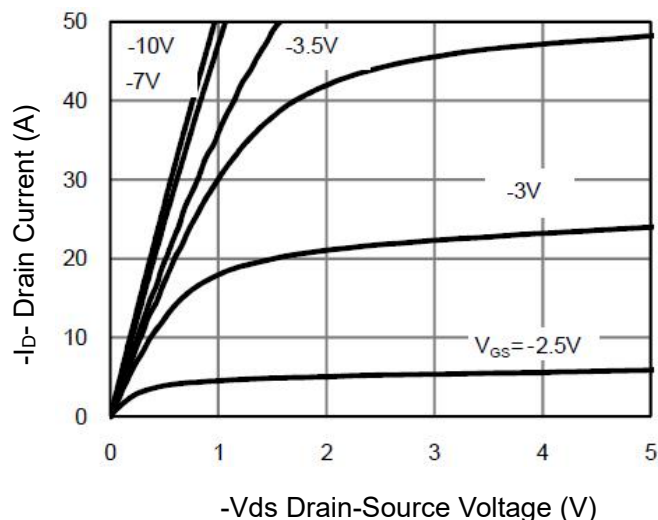


Figure 1 Output Characteristics

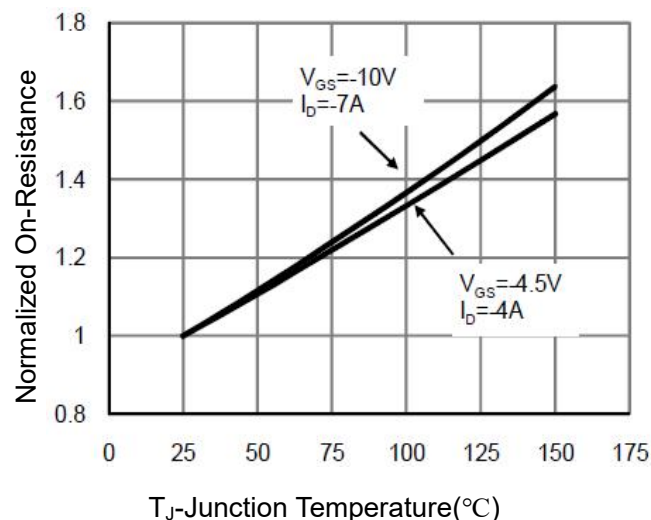


Figure 4 $R_{DS(on)}$ -Junction Temperature

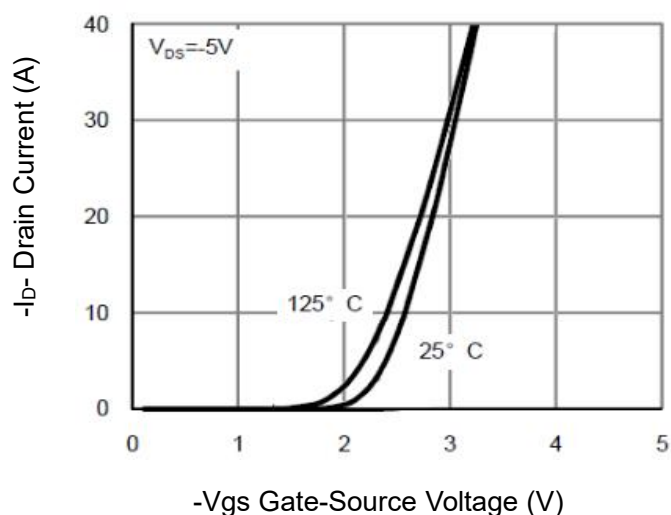


Figure 2 Transfer Characteristics

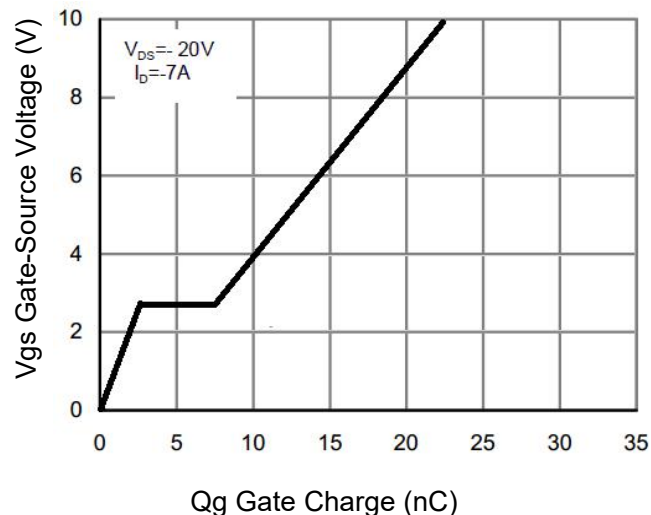


Figure 5 Gate Charge

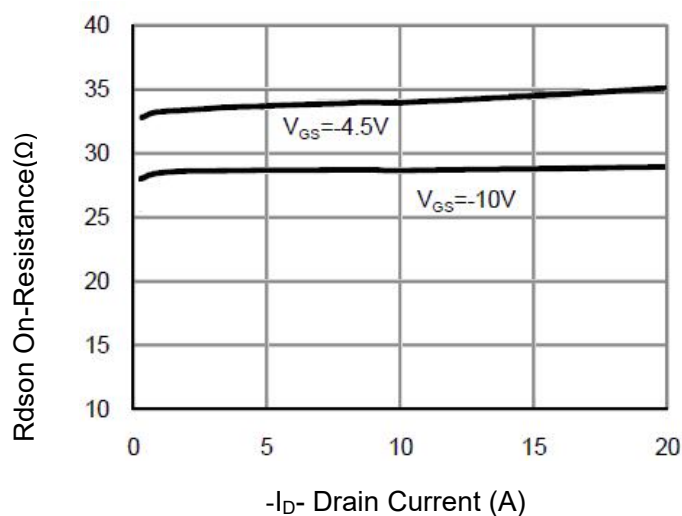


Figure 3 $R_{DS(on)}$ - Drain Current

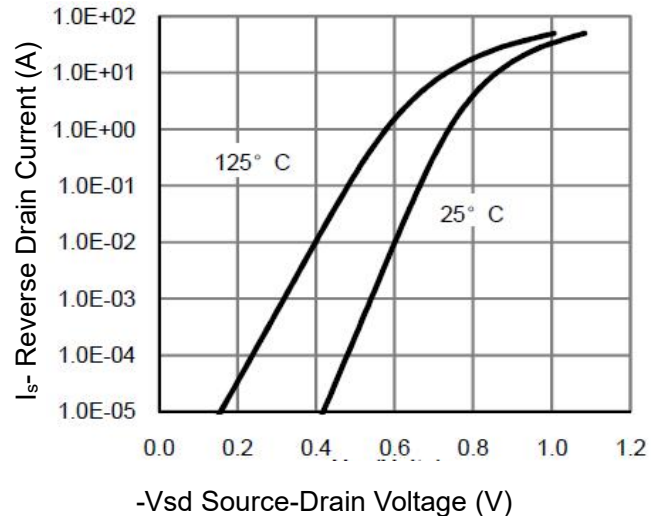
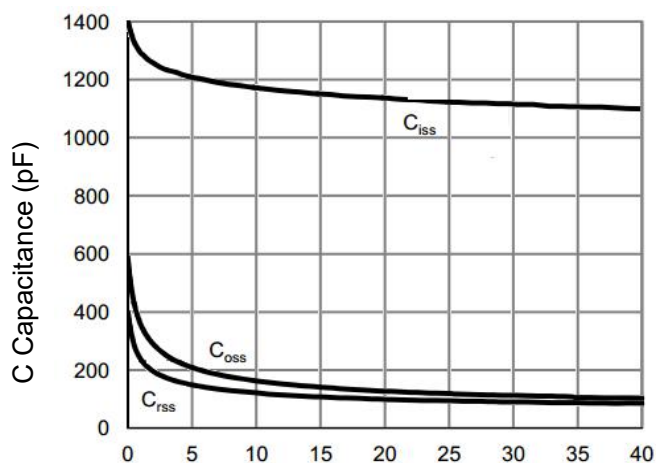
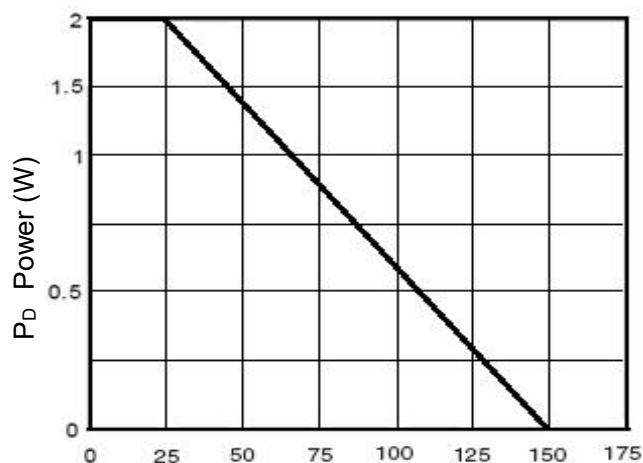


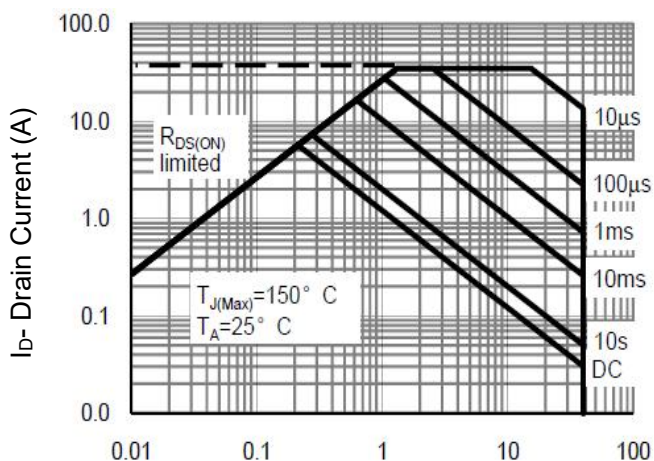
Figure 6 Source- Drain Diode Forward



-Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J -Junction Temperature($^{\circ}\text{C}$)
Figure 9 Power Dissipation



-Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area

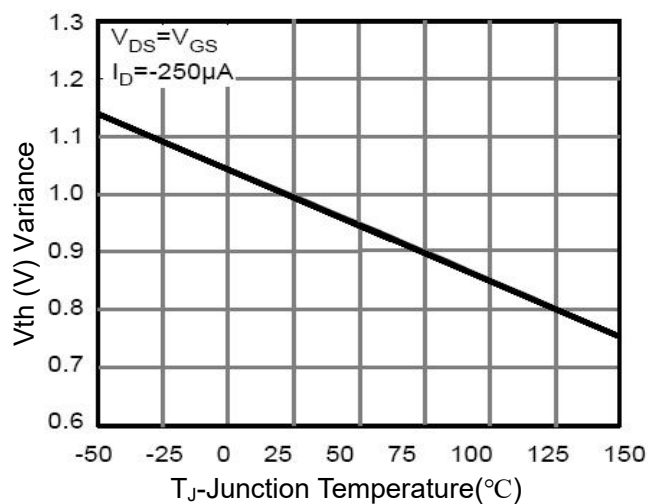


Figure 10 $V_{GS(th)}$ vs Junction Temperature

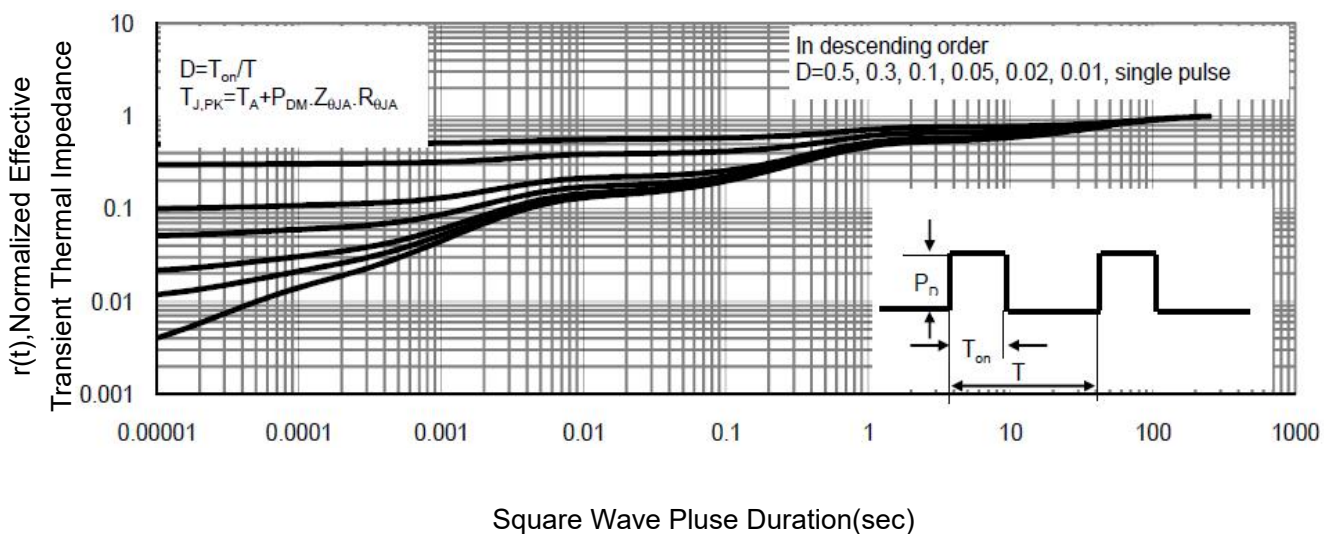


Figure 11 Normalized Maximum Transient Thermal Impedance